Ref. No.: Ex/PG/ETCE/T/1210B/2019

M.E Electronics and Tele-Communication Engineering, First Year Second Semester Examination, 2019

EMBEDDED SYSTEMS

Time:3 Hours. **Full Marks: 100**

Answer any FOUR questions.

1. Design an ASIC for the following state-machine. An output pulse z is to be coincident with the second of 2 consecutive x_2 pulses immediately following an x_1 pulse. [25]

2. Develop a state diagram, flow chart/algorithm, data-flow path and control logic of an Integrated Circuit (IC) to obtain the sum of first n terms of the series: $1 + 2x + 3x^2 + 4x^3 + \ldots + (n\text{-}1)x^n$. Presume that the proposed IC inputs the first two elements of the series. [25]

3. (a) Emphasize the importance of a Hierarchical state machine in the context of an elevator design. [10]

   (b) Construct a lattice automaton with 4 states: 0, 1, 2, 3 and two input symbols: a and b, such that the automaton can recognize the string: bbaa in at least 3 ways. Assign lattice beliefs: x, y and z for state transitions with input symbols a and b arbitrarily. Construct 2 arbitrary Hasse diagrams and compute the lattice beliefs to recognize the given string: bbaa using the Hasse diagrams. [15]

4. (a) Design a PLA to store the combinational logic - $A\bar{B}C, \bar{A}BC, A\bar{B}\bar{C}$ and $\bar{A}\bar{B}\bar{C}$. [10]

   (b)Construct a PAL to develop the following switching functions:

   $$y_1 = \bar{A}B\bar{C} + AB\bar{C},$$

   $$y_2 = \bar{A}C + A\bar{B}C.$$ [10]

   (c) Modify the above PAL into a PLD for the following switching function:

   $$y_1 = \bar{A}B\bar{C}y_1 + AB\bar{C}.$$ [5]

5. (a) Draw the schematic diagram of the basic FPGA module developed by Fairchild Corporation. [5]

   (b) Realize a Half Adder on this FPGA module. [10]

   (c) How optimal mapping of a logic function is done on an FPGA? [10]

6. (a) Explain with a schematic diagram, the interface of a Dot-Matrix Printer with a micro-computer. [10]

(b) Develop an assembly level program with appropriate remarks to transfer a block of data-bytes to the printer. [10]

(c) Justify the importance of the printer buffer and the character generation ROM in a DOT Matrix Printer. [5]

7. (a) Develop a scheme to transfer a 2 byte set-point to a process control program under online condition using RST 7.5 and RST 5.5 interrupt. [5]

(b) Also design an assembly level program to undertake the above scheme. [10]

(c) Explain the operation of the instruction: STR r_0,[r_1] with the help of a neat diagram of the ARM architecture. Show the data instruction-flow path by arrowheads along the appropriate buses. [10]

8. (a) Explain the importance of the Hardware-Software partitioning problem in Embedded Systems. [5]

(b) Write down the equations involved in the Ant Colony optimization. Also explain the equations. [10]

(c) State the main steps of the Ant colony optimization algorithm. [8]

(d) How will you use the above algorithm to solve the Hardware-Software partitioning problem? [2]

9. Write short notes on any **two** of the following:

(a) Task merging and splitting on a Task Graph.

(b) Principles used in Mind-driven position control of a 2-D robot arm using ERD/ERS and ErrP brain signals.

(c) Fuzzy Automation. 12 ½ ×2