Ref No . **Ex/PG/ETCE/T/129F/2019**

MASTER OF ENGINEERING IN
ELECTRONICS & TELE-COMMUNICATION ENGINEERING EXAM -2019

(First Year, 2nd Semester)

ELECTRONIC DESIGN AUTOMATION (ED)

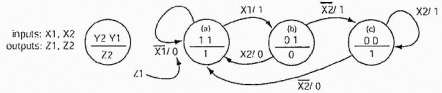
Time : Three Hours **Full Marks : 100**

Answer any four questions.

1.

a. What is test bench? Write test bench program to verify XOR gate . **2+8=10**

b. Write the VHDL code of following FSM **8**



c. Explain with example about multiple processes? **7**

2.

a. What is delta delay in VHDL? Explain the operation of transport and inertial delay on signal driver? **4+6= 10**

b. Design a 16:1 MUX using suitable MUX tree. Write the code using structural model. Use process for input sensitivity list. **8**

c. Write a program of Mod 5 counter by using structural model. **7**

3.

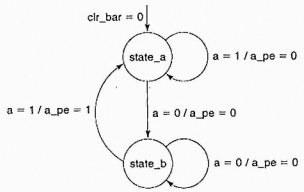
a. What is resolved signal? Write a short code to describe the resolution function **2+8=10**

b. Write a VHDL code to find out square root of a unsigned number **7**

c. Write a VHDL code for 8-bit bus that feeds and receives feedback from bidirectional pins. **8**

4.

a. Write the VHDL code of Mealy FSM state diagram for a positive edge detector. **12**



b. Write a program of D flip flop using behavioral model **6**

c. Write a program of single bit magnitude comparator in VHDL with proper circuit. Write proper syntax and there is no restriction on logic gate usage. **7**

5.

a. Explain the MOS small signal model and describe MOS capacitor. **8**

b. What is SPICE Level -1 model what are the primary net-list parameters? **4**

c. What is the requirement of scaling? What is constant field scaling and constant voltage scaling? **3+4=7**

d. Describe the condition of Cox, Id(linear), Id(Sat) , power dissipation, power density, gate delay for both constant field and constant voltage scaling **3+3=6**

6.

a. What is design for manufacturability? What is different process variation and how it changes the device, circuit and system? **10**

b. Define system level partitioning and board level partitioning **8**

c. Define RSM. Explain the factorial design of performance modeling procedure. **7**

7.

a.	What are the operational process in Floor planning and Placement?	**8**
b.	What are the differences between global and detailed routing?	**6**
c.	Why new trends in VLSI design providing complexities in design flow.	**8**
d.	Define physical design and its flowchart	**3**