EX/PG/ETCE/T/128D/179/2019

Master of Electronics and Tele-communication Engineering Examination, 2019 (1st year 2nd Semester)

Subject: VLSI Design

Time: Three hours Full Marks: 100

Answer any five questions

Q1. (a) Compare the merits and demerits of serial and parallel adders with reference to addition of two 4 bit numbers. Design a full adder using two 4:1 multiplexers. Draw the modified truth table of the final circuit.

(b) Design the control circuitry for a garage door opener. A single button controls the opening and closing of the door. Pressing the button opens a closed door or closes an opened door. For safety reasons, the direction of a moving door should be reversed immediately if the button is pressed. 8+12=20

Q2 (a) Describe the various types of power dissipation in CMOS inverter. How they can be controlled?

(b) "For reducing one type of power dissipation we require fast rising and fast falling signals at the input and slow rising & falling signals at output". What is that power dissipation? Explain the statement with proper justifications along with its absence condition.

(c) What is the philosophy behind the use of the pipelining technique to save power?

(d) In a pipelining scheme employed for low power logic architectures in VLSI Design , calculate the power savings when supply voltage is reduced from 1.8V to 1.2V (assume your required capacitor value suitably for your calculation). 5+ 5+ 2 + 8 = 20.

Q3 (a) Explain the following statements with proper justifications.

(i) "Minimize capacitance and wire length of nodes with high activities"

(ii) "Precharged logic always consume more power than static logic"

(b) Adapt supply voltage for performance needed: Explain with suitable examples.

(c) Consider a CMOS inverter. Assume that V_{DD}=1.8V, $W_n = 4\lambda$, $W_p = 20\lambda$, $L_n = L_p = 2\lambda$ .Using 180nm parameter: μ_n =287cm^2/V.s, μ_p = 88cm^2/V.s , $V_{thn} = |V_{thp}| = 0.35V$. Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th} and Noise Margins. 6+4+10=20

Q4(a) What are high and low-skewed logic gates? Explain GDI logic with an example. Implement two-input XOR gate with GDI logic. Explain their operations. Explain pseudo and Ganged CMOS logic with an example for each.

(b) For a CMOS inverter, consider the following parameters: V_{DD} = 5V, V_{THn} = 0.5V. A saturation current of 2.2 mA results when $V_{DS} \geq 4.5V$. Assume a step pulse signal at the input which switches instantaneously from 0 - 5V. Find the delay time necessary for the output to fall from its initial value 5V to 2.5V. Take C_L = 300pF. 12+8=20

Q5 (a) Why low power has become an important issue in the present day VLSI circuit realization? List the differences and similarities between constant field scaling and constant voltage scaling and give justifications.

(b) Calculate the threshold voltage of a MOSFET based NAND gate converted to inverter when V_{DD}=1.2V, μ_n =570cm^2/V.s , μ_p = 190 cm^2/V.s $W_p = 2W_n$, $L_n = L_p$, $V_{thn} = |V_{thp}| = 0.35V$

13+7=20

Q6. (a) How is a CMOS inverter different from a resistive load inverter? Which is preferred and why?

(b) What is pass transistor? Write its advantages and disadvantages. Realize a XOR Gate using pass transistors and explain its operation.

(c) Referring to the pseudo-nMOS inverter, show analytically that :

(i) The low-level input voltage VIL is : $V_{IL} = V_{thn} + \frac{V_{DD} - |V_{thp}|}{\sqrt{k_R(k_R + 1)}}$ and

(ii)The high level input voltage VIH is: $V_{IH} = V_{thn} + \frac{2(V_{DD} - |V_{thp}|)}{\sqrt{3k_R}}$ Symbols have the usual meanings. 3+5+12=20

Q7. (a) Lost performance compensated by parallelism is a technique for low power VLSI design: Explain with suitable examples.

(d) No lower limit to power consumption: Explain with suitable examples and circuit if possible.

(c) Design a combinational lock with three buttons 1, 2 and R. The numerical buttons are used to enter a code and the R button is used to reset the lock. To open the lock, a user would first push the reset button R and then enter a code of 3 digits. If a mistake is made in the process, the R button can be used to start over again. Your circuit should produce an output of 0 to open the lock after the correct code has been entered. Show the design process and the schematic circuit diagram of this lock for the code 1 -2 -1.

4+4+12=20

Q8. (a) What are DPL and its features? How would you implement a switching function using DPL style? Distinguish between CPL and DPL.

(b) How is the transfer characteristics of a CMOS NAND gate affected with increase in fan-in ?

(c) Use a minimum number of inverters and nMOS transistors to design a CMOS positive-edge-triggered "toggle" flip-flop with an asynchronous reset (R). A toggle flip-flop is a storage device with a control input T. If T=1 when the clock ticks, the state of the flip-flop changes; otherwise, it remains the same as the previous state. 5+3+12=20