M. E. ELECTRICAL ENGINEERING 1ST YEAR 2ND SEMESTER EXAMINATION, 2019
(2nd Semester)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEMS (MS)

Full Marks 100

Time: **Three hours**

No. of Questions		Marks
	Answer any five.	
1.	a) What are the different types of model for calculating gate delay of CMOS logic gates using parameters as W/L ratio, VDD, VSS, channel resistance RP, RN, load capacitance CL.	6
	b) Discuss how speed power product decides the operating frequency of CMOS gate.	4
	c) What are the advantages of variable threshold –CMOS gate?	4
	d) What is cross talk? Explain how it affects the performance of wire in VLSI fabrication. Show appropriate characteristic plot for delay vs W/H ratio, where W is the width of wire and H is the height of the wire from the plane of substrate.	6
2.	a) Illustrate different methods of routing in programmable interconnect systems. Explain the basic difference between SRAM based and CMOS logic gate based Look-up table. Explain "Antifuse" and "Flash" element which can be used for configuring logic elements in FPGA.	8
	b) Compare the performances of Carry-look ahead and Carry-skip Adders showing their functional diagram and Boolean expression.	6
	c) Show the functional diagram of array multiplier.	2
	d) Explain the Booth algorithm for binary multiplication, giving example.	4

3.	a) Explain the terms: i) Event driven simulation , ii) Simulation time wheel	5
	b) Distinguish between structural and behavioural modeling.	5
	c) What is meant by path delay and critical path delay? Give examples.	5
	d) What is meant by logic optimization phases in logic synthesis process? Give suitable examples.	5
4.	a) Describe the elevator unit control state machine using FSMD model definition <S, I, O, V, H, S_o>, where S, I, O, V, H, S_0 are the states, inputs, outputs, variables, action function and initial state. Also draw the state diagram also.	8
	b) State the advantage of adding hierarchy, concurrency to the state machine model showing state diagram.	6
	c) Write the sequential programming language pseudo code for elevator unit control system.	6
5.	Compare: a) Timer and watchdog timer. b) Controller and datapath for processors. c) Synchronous and asynchronous communication. d) Development processor and target processor.	4x5
6.	a) What are the basic functional units available in a generalized microcontroller? State the role of two such units that are used in	3+2

	communicating and controlling external devices.	
	b) What are the different constraints the programmer has to handle while fitting a functional model on an FPGA IC?	5
	c) Explain the process of CAD design flow with suitable diagram to create and implement a complete functional model on a configurable IC.	10
7.	Write short notes on any ***two***:	10+10
	i) Implementation of programmable matrix using diode-arrays.	
	ii) Configurable PAL.	
	iii) Sub-operations in instruction cycles.	
8.	a) Describe with suitable diagram the working principle of antifuse. What are the advantages of using antifuse over SRAM cell?	7+3
	b) What is locality of reference? How is the concept of locality of reference utilized to optimize the functioning of memory management hardware?	5+5