Modelling and Simulation Based Analysis of Random Dopant Fluctuation in DG JLFET under Quantum Confinement

Submitted in partial fulfilment of the

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By

RAUNAK ROY

Class Roll No: 002110702003

Exam Roll No: M4ETC23001

University Registration No. : 160203 of **2021-2022**

Under the Guidance of

Prof. Chayanika Bose

Jadavpur University

2023

DECLARATION

I hereby declare that the thesis entitled "**Modelling and Simulation Based Analysis of Random Dopant Fluctuation in DG JLFET under Quantum Confinement**" submitted by me, for the award of the degree of **Master of Engineering in Electronics & Tele-Communication Enguneering** of Jadavpur University is a record of bonafide work carried out by me under the supervision of **Prof. Chayanika Bose**.

I further declare that the work reported in this thesis has not been submitted and will not be submitted, either in part or in full, for the award of any other degree or diploma in this institute or any other institute or university.

Raunak Roy

Signature of the Candidate

Place: Jadavpur

Date: 11/09/2023

CERTIFICATE

This is to certify that the thesis entitled "Modelling and Simulation Based Analysis of Random Dopant Fluctuation in DG JLFET under Quantum Confinement" submitted by Raunak Roy having Reg. No. 160203, Class Roll No. 002110702003 and Exam Roll No. M4ETC23001 of Jadavpur University for the award of the degree of MASTER OF ENGINEERING in ELECTRONICS & TELE-COMMUNICATION , is a record of bonafide work carried out by him under my supervision, as per the code of academic and research ethics.

The contents of this report have not been submitted and will not be submitted either in part or in full, for the award of any other degree or diploma in this institute or any other institute of university. The thesis fulfils the requirements and regulations of the University and in my opinion meets the necessary standards for submission.

CBose 11.09.23.

Prof. Chayanika Bose

Professor (Retd.)
Electronics & Tele-communication
Engineering Department
Jadavpur University
Kolkata-700 032

The thesis is satisfactory / unsatisfactory

Internal Examiner

External Examiner

Approved by

Manotosh Biswas 12/09/23

HOD

Department of Electronics & Tele-Communication Engineering

MANOTOSH BISWAS
Professor and Head
Electronics and Telecommunication Engineering
Jadavpur University, Kolkata - 32

Saswati Majumder 12/9/23

DEAN

Jadavpur University, Faculty of Engineering & Technology

DEAN
Faculty of Engineering & Technology
JADAVPUR UNIVERSITY
KOLKATA-700 032

ABSTRACT

Moore's Law has been observed in the Microelectronics and Semiconductor Industries since 1970. Trend of downscaling transistors smaller and smaller to make processors work faster than before with implementation of VLSI (Very Large Scale Integration), ULSI (Ultra Large Scale Integration), GLSI (Giga Large Scale Integration) techniques require fabrication of nano-scale transistors. This presents significant challenges in term of developing new device structures and manufacturing processes. Because of the laws of diffusion and the statistical nature of the distribution of the dopant atoms in the semiconductor and rise of other Short Channel Effects, formation of ultra shallow junctions with high doping concentration gradients in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has become an increasingly difficult challenge for the semiconductor industry.

J.P. Collinge proposed an idea of using Junctionless transistors (also called gated resistor) for fabrication of nanoscale transistors. Junctionless transistors commonly known as JLFET (Junctionless Field Effect Transistor) have no junctions since a homogeneous highly doped substrate is used with Gate Oxide deposition over JLFET to control the current flow. These devices have full CMOS functionality and are made using silicon nanowires.
Since inception of JLFET in Semiconductor Industries, numerous researches and simulations on its fabrication techniques, device characteristics, etc. have been performed by Researchers.. But analytical models of JLFET under various short channel effects like Quantum Confinement and Random Dopant Fluctuations (RDF) needs more emphasis.

In our project, we have proposed an analytical model regarding impact of Quantum Confinement and RDF in Threshold Voltage and other parameters of an ultra short channel DG (Dual Gate) SMG (Single Material Gate) JLFET. We have incorporated Quantum Confinement effects on 3D JLFET into our model and derived threshold voltage for short channel JLFET. In addition, we have introduced a new approach that would give insights regarding impact of dopant atoms on threshold voltage in terms of their lattice site occupancies, and thus, RDF has been included in our model. The dependence of threshold voltage on different physical parameters of JLFET has also been investigated.

We have also simulated ultra short channel DG SMG JLFET using Silvaco TCAD Atlas with inclusion of Quantum Confinement Effects and compared simulation results obtained with the results predicted by our model, providing plausible explanations for any deviation from simulation results. The influence of RDF on the threshold voltage has been investigated through model simulation, where randomization of number has been included to account for the random factor regarding positional occupancy of dopant atoms.

Finally we incorporate both RDF and Quantum Confinement effects simultaneously in our model and observe fluctuations in threshold voltage for different channel lengths, and also provide statistical interpretation of its behavior.

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This is a great opportunity to express my gratitude and respect to all the persons who have supported me in their own way , during my thesis work.

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Raunak Roy 11/09/2023

Raunak Roy

Class Roll: 002110702003
Exam roll: M4ETC23001
Electronics And Tele-Communication Engg. Dept.
Jadavpur University
Kolkata

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Chapter 1

Introduction

Trends in the microelectronics industry require the fabrication of smaller and smaller components, resulting in transistor sizes down to the nano-scale. This presents significant challenges in term of developing new device architectures and manufacturing processes. Over the past decades, the size of MOSFETs has continually been scaled down leading to MOSFET with effective channel length less than ten nanometers. A classical MOS transistor comprises two PN junctions called the source junction and the drain junction. The effective channel length is the distance that separates these two junctions, and the source and drain junctions are separated by a region with opposite doping type. The formation of such junctions involves extremely high doping concentration gradients, and very low thermal budget processing must be used. Flash annealing techniques are currently used to heat silicon for a very short time period in order to minimize diffusion; but even in total absence of diffusion, ion implantation and other doping techniques do not achieve perfectly abrupt junctions with infinite concentration gradients. Therefore it would be suitable to use a transistor device structure that overcomes the above-mentioned problems .

Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms in the semiconductor, the formation of ultra shallow junctions with high doping concentration gradients has become an increasingly difficult challenge for the semiconductor industry. Junctionless transistors (also called gated resistor) have no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires. The key to fabricating a Junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned OFF. The semiconductor alsoneeds to be heavily doped to allow for a decent amount of current flow when the device is turned ON.Incorporating these two together imposes the use of nanoscale dimensions and high doping concentration.

JLFETs contain the same doping concentration of a single doping species across the semiconductor region, and thus have been proposed as one of the promising alternatives over

conventional fin field-effect transistors (FinFET), which are more complicated to process and costlier to manufacture. Moreover, it is expected that the JLFETs can maintain scaling down of complementary metal-oxide-semiconductor (CMOS) technology owing to restrained short channel effects (SCEs) by increased effective channel length. In addition, to improve device characteristics like ON-state current, adopting new channel materials is a favorable technique.

1.1 **Thesis Objective**

In this thesis,we study device physics of DG JLFET and impact of Random Dopant Fluctuations in its Threshold Voltage. Our main objective is to model threshold voltage of a short channel DG JLFET with inclusion of RDF and Quantum Confinement Effects.Using this model,we would observe behavior of threshold voltage with change in different physical parameters of DG JLFET and we could also make a comparison with Simulation results for verification and validation of our model. Observing fluctuations in Threshold Voltage due to RDF and understanding RDF in terms of lattice occupancy of dopant atoms is also a priority in this thesis.

1.2. Organization of the Thesis

The present thesis has been organized as follows:

- Chapter 2 gives a vividexplanationof device physics of JLFET. Device fabrication and different types of JLFET have also been explained. Concept of RDF along with recent findings and work progress of JLFET have been described in this chapter.
- Chapter 3 includes simulation of DG JLFET and analysis of JLFET under different modes of operation based on the simulation results.
- Chapter 4 focuses on classical approach for the derivation of threshold voltage of DG JLFET and influence of various physical parameters on it.
- Chapter 5 gives a section for current derivation in JLFET and also exhibits family of I-V curves for different physical parameters of JLFET and also gives explanation for their characteristic behavior.
- Chapter 6 proposes a new model for threshold voltage formulation based on the positional occupancy of dopant atoms and also makes a comparison with the simulation results.
- Chapter 7 incorporates Quantum Confinement effects in the proposed model and compares analytical resultswith respective simulation results.

- Chapter 8 includes the phenomenon of RDF in the proposed model to show the resulting fluctuationsin threshold voltage under consideration.
- Chapter 9 finally fulfills our thesis objective by incorporating RDF and Quantum Confinement Effects in our proposed model and observing fluctuations of threshold voltage.
- Chapter 10 provides Conclusions and future scopes for the present work.

Chapter 2

Literature Survey

2.1.Device Structure of JLFET

The Lilienfield transistor, like modern metal oxide semiconductor (MOS) devices, is a field-effect device. A thin semiconductor film is put on top of a narrow insulator layer, which is deposited on top of a metal electrode. The device's gate is made up of the latter metal electrode. Through operation, current can flow in the resistor between two contact electrodes, similar to how drain current flows in a conventional MOSFET between the source and drain. The Lilienfield device is a simple resistor in which the introduction of a gate voltage causes the carriers in the semiconductor layer to be depleted, changing its conductivity. In an ideal scenario, it should be feasible to deplete the semiconductor layer of carriers completely, resulting in a quasi-infinite resistance to the device. Unlike all other types of transistors, the Lilienfield transistor does not have a junction.

The Lilienfield transistor is a gated transistor with a gate that regulates carrier density and therefore current flow.

2.1.1.SINGLE GATE JLFET

the single gate JLT has two types of structures: bulk and SOI (Fig.2.1). Because the bulk structure can be doped and biased, it gives more control over the device's characteristics.

When compared to SOI, bulk junctionless transistors have a lower effective thickness and the bulk SGJLT has better analog performance than the SOI structure, with better output transconductance, output resistance, early voltage, and inherent gain.

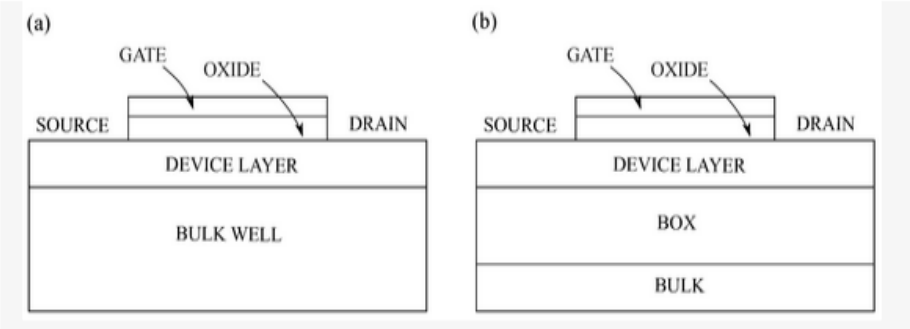

Fig2.1: Cross-sectional view of: (a) Single Gate junctionless transistor (SGJLT) (b) SGJLT with SOI structure.

2.1.2.DOUBLE GATE JLFET

The structure of a double gate junctionless transistor is shown in fig 2.2

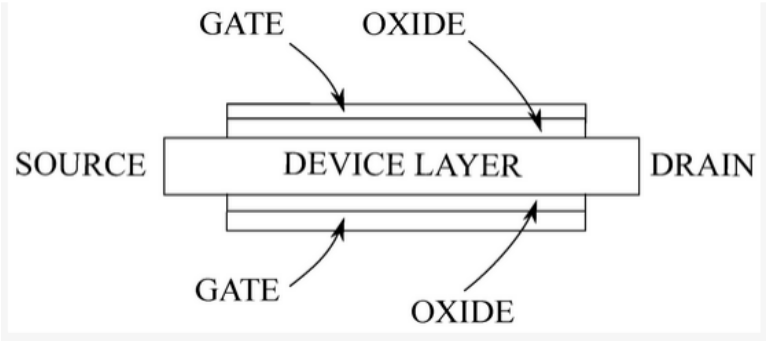

Fig2.2: Cross-sectional view of a double gate junctionless transistor.

Double Gate JLFET provides more control than SG-JLLFET on the mobility and conduction of electrons in N+ doped channel of JLFET under different modes of operation.

2.1.3.TRI-GATE JLFET

Bulk and SOI structures of Tri-gated JLFET is shown in fig 2.3.

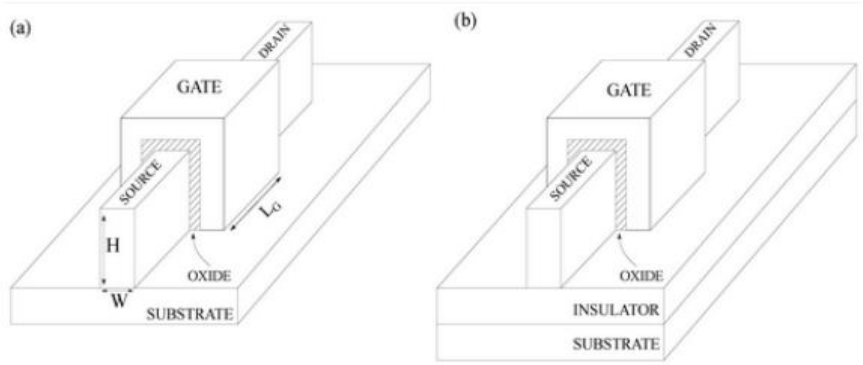

Fig.2.3: 3D TG JLFET structure: (a) bulk (b) SOI.

2.1.4.GATE-ALL-AROUND JLT or GAAFET

A model of a cylindrical junctionless Gate -All-Around transistor is shown in Fig 2.4.

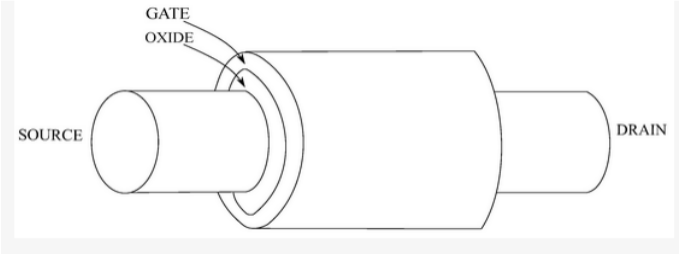

Fig.2.4: Three-dimensional (3D) structure of a cylindrical junctionless GAAFET.

2.2.Conduction Mechanism in JLFET

2.2.1.Physics of JLFET under different regions of operation

MOSFETs (including accumulation-mode FETs) are normally off devices, as the drain junction is reverse biased and blocks any current flow if no channel is created between source and drain. To turn the device on, the gate voltage is increased in order to create an inversion channel.

The junctionless transistor, on the other hand, is basically a normally on device where the work function difference between the gate electrode and the silicon nanowire shifts the flatband voltage and the threshold voltage to positive values. When the device is turned on and in flatband conditions, it basically behaves as a resistor and the electric field perpendicular to current flow is basically equal to zero in the ‘‘bulk’’ channel.

Figure 2.5 shows the drain current as a function of gate voltage in pi-gated SOI MOSFETs (Fig.2.6) in inversion-mode ‘‘N^+PN^+’’(fig 2.7.a), accumulation-mode ‘‘N^+NN^+’’ and heavily doped junctionless ‘‘$N^+N^+N^+$’’ transistor(fig 2.7.b).

• Below threshold the inversion-mode device is depleted (either fully or partially) and the flatband voltage is situated below the threshold voltage, at a gate voltage at which the device is off (Fig.2.5a). Below flatband , the body is p-type neutral. Above threshold, the body of the channel is depleted and a surface inversion layer is formed.

• Below threshold accumulation-mode devices are fully depleted. Threshold is reached when the gate voltage is increased in such a way that a portion of the channel region is no longer depleted. At that point, the channel region is technically partially depleted. As gate voltage is further increased, flat-band is reached: the channel region is now neutral (i.e. no longer depleted, even partially). Further increasing the gate voltage creates a surface accumulation channel (Fig.2.5b).

• The heavily doped junctionless transistor is fully depleted below threshold. As gate voltage is increased, the electron concentration in the channel increases, and threshold is reached when the peak electron concentration in the channel reaches the doping concentration N_D. Further increasing the gate voltage increases the ‘‘diameter’’ of the region where $n = N_D$, until the entire cross section of the device becomes neutral (i.e. no longer depleted, even partially), at which point flatband is reached (Fig.2.5c). It is possible to further increase the gate voltage

to create accumulation channels, but this is probably not desirable, as the high doping concentration in the channel already insures a large current drive.

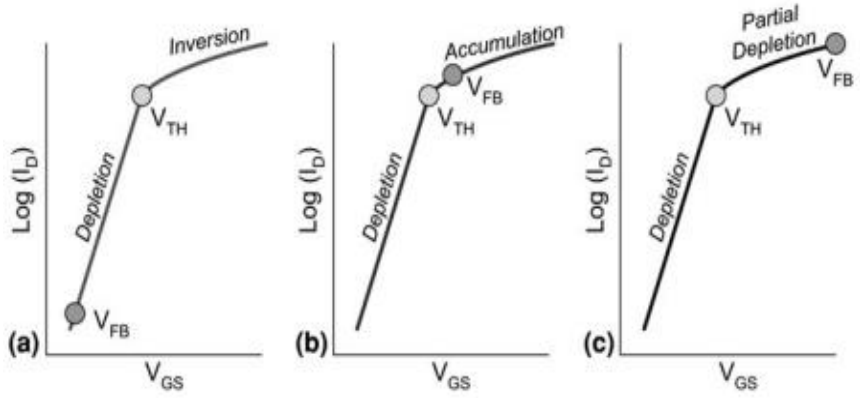

Fig.2.5: Drain current (log scale) as a function of gate voltage in (a) an inversion-mode MOSFET; (b) an accumulation-mode MOSFET and (c) a heavily-doped JLFET

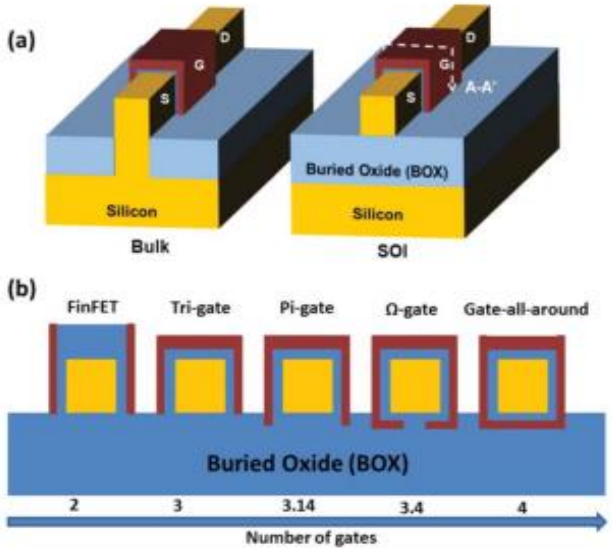

Fig.2.6: Schematic of (a) bulk and SOI multi-gate FETS, and (b) cross-section of different multi-gate FETS and their corresponding effective number of gates.

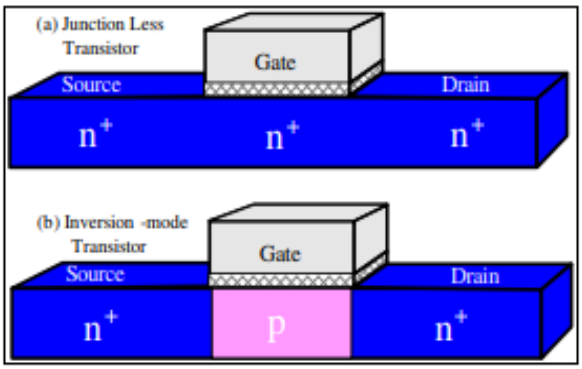

Fig.2.7: Longitudinal cross sections showing the doping profiles in: (a) a junctionless device, (b) an inversion-mode transistor.

Below threshold, the junctionless channel is depleted of electrons, and the current varies exponentially with gate voltage (Fig.2.8a). At threshold, a neutral silicon filament forms between source and drain (Fig.2.8b). The cross-section of filament increases when gate voltage is increased (Fig.2.8c) until depletion disappears and the device is in flatband condition (Fig.2.8d). Fig 2.9 shows band diagram of DG JLFET for different regions of operation.

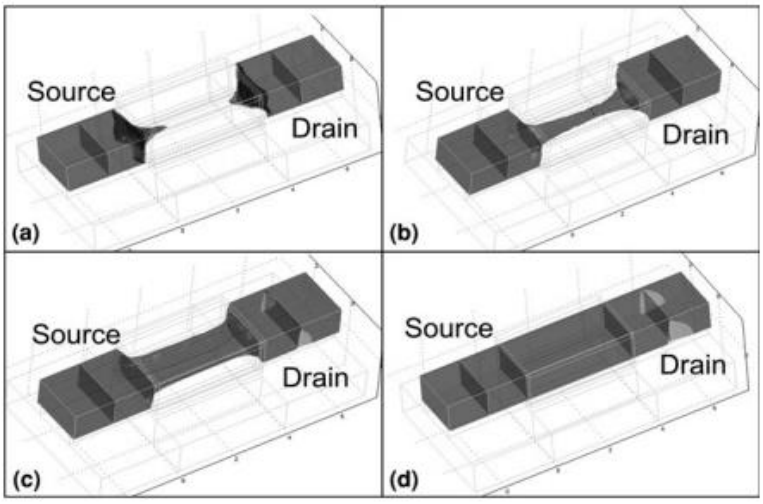

Fig.2.8: Electron concentration contour plots in an n-type junctionless transistor for V_{DS} = 50 mV. a)$V_G < V_{TH}$; b)$V_G = V_{TH}$ c)$V_G > V_{TH}$; d)$V_G = V_{FB} >> V_{TH}$.

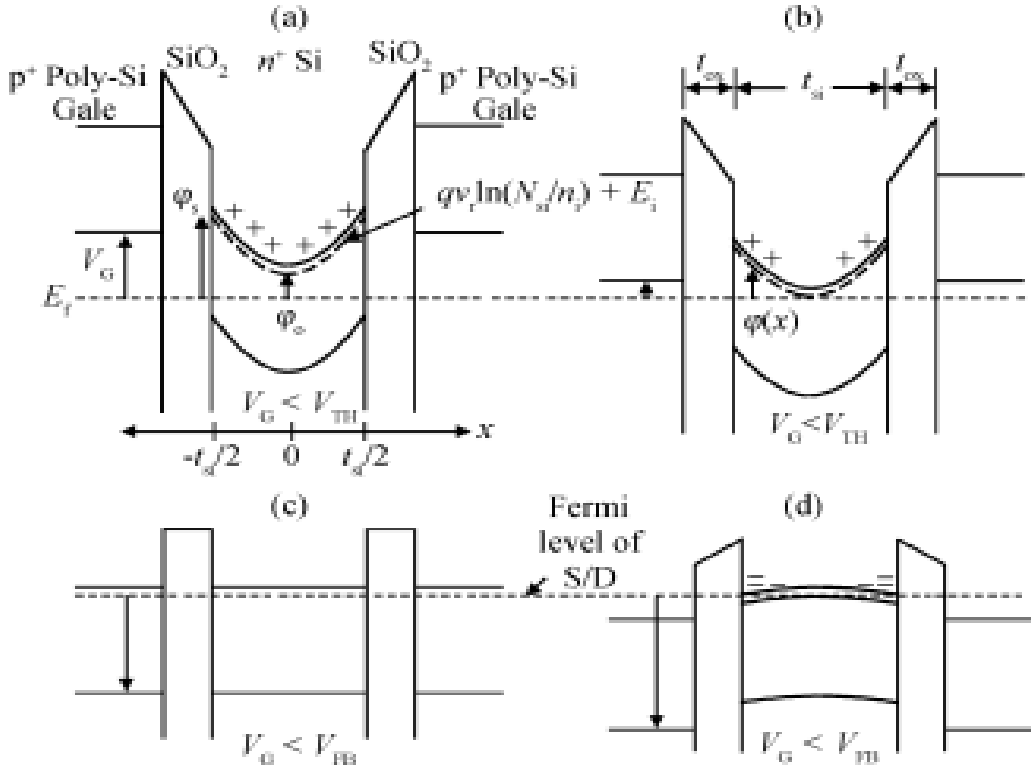

Fig.2.9: Schematic band diagrams for a symmetric DG-JLFET. (a) Fully depleted and downwardly bent channel in the sub threshold mode. Partially depleted and downwardly bent channel in the bulk current mode. (c) Flattened channel in the flat band mode. (d) Upwardly bent channel in the accumulation.

2.2.2.Subthreshold Conduction Path of JLFET

Unlike accumulation-mode and inversion-mode devices the channel of junctionless transistors is in the bulk of the nanowire (i.e. it is not a surface channel). As a result, carriers in the channel are exposed to a low electric field in the directions to current flow. This strongly reduces the degradation of mobility when gate voltage is increased in the on state [5] . Figure 2.10 shows the position of the channel in both subthreshold operation and above threshold. In an inversion-mode device, subthreshold conduction mainly takes place in the top corners of the device (Fig.2.10a). Above threshold, surface channels are formed on three sides of the nanowire, with carrier concentration peaks in the corners Fig. 10d). In an accumulation-mode transistor, the subthreshold current flows through the bulk of the device, near the center or the back of the nanowire (Fig.2.10b). When the device is turned on, a small current flows through the body of the nanowire, but this current typically amounts for less than ten percents of the overall current drive. Most of the current flows in surface and corner

accumulation channels, like in an inversionmode device (Fig.2.10e). In the junctionless device the subthreshold current flows in the center of the nanowire, as in the accumulation-mode device (Fig.2.10c). When threshold is reached, the channel leaves full depletion and a neutral (‘‘undepleted’’) channel forms between source and drain, in the center of the device (Fig.2.10f). Thus, the junctionless transistor is partially depleted when it is turned on.

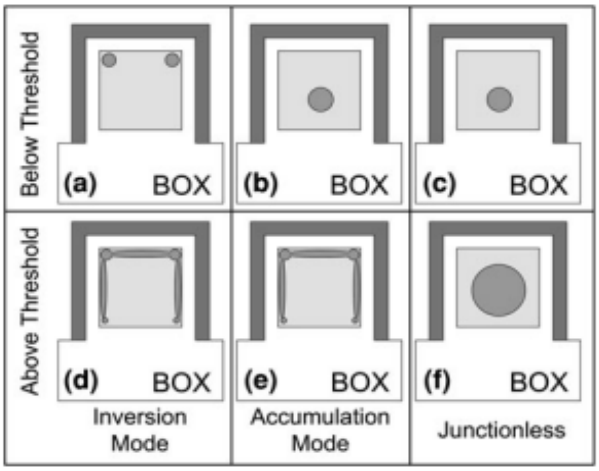

Fig.2.10: Location of conduction path in the different devices. Subthreshold conduction path in a) inversion-mode, b) accumulation-mode and c) junctionless devices. Conduction channels above threshold in d)inversion-mode, e) accumulation-mode and f) junctionless devices.

2.3.Threshold Voltage of JLFET

2.3.1.Variation of Threshold Voltage

The threshold voltage of junctionless devices depends on silicon film thickness, width of the nanowire, doping concentration and gate oxide thickness (Fig.2.11). One can easily obtain different threshold voltages by varying the width of the nanowires, if doping concentration is kept constant, which may be useful for producing devices with multiple values of V_{TH} on a chip. Figure 2.11 shows the variation of threshold voltage in a long-channel junctionless device as a function of silicon width (W_{si}) and thickness (T_{si}). The EOT is 0.5 nm and the doping concentration is 2×10^{19} cm^{-3} . Threshold voltage can be varied from 1 to -0.2 V by varying W_{si} from 5 to 20 nm and T_{si} from 5 to 15 nm.

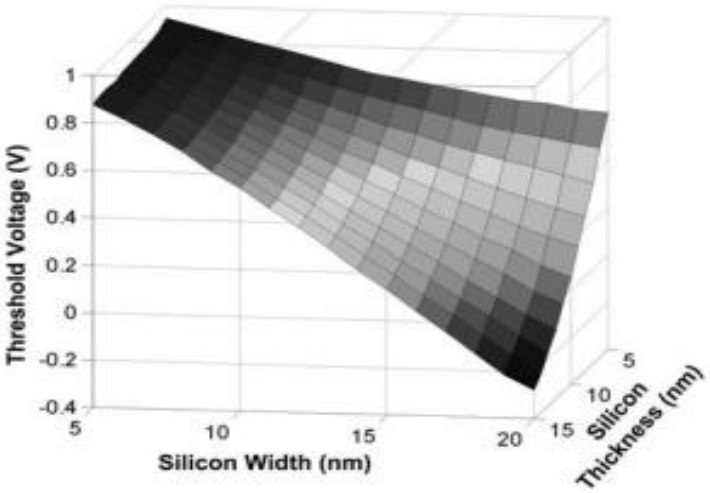

Fig.2.11: Long-channel V_{TH} defined as peak in $\frac{dg_m}{dV_G}$ for T_{ox} = 0.5 nm and $N_D = 2 \times 10^{19}$ cm^{-3}

2.3.2.Sensitivity of Threshold Voltage with fabrication parameters

It is important to evaluate the sensitivity of V_{TH} variations with fabrication parameters. Figure 2.12 shows the results of such an analysis. If one of the dimensions (T_{si} or W_{si}) is small enough, the variations of the other dimension do not impact too much the threshold voltage. For example, if the silicon thickness is 5 nm, the variation $\Delta V_{TH}/\Delta W_{si}$ is equal to 25 mV/nm. At the same time, the variation of threshold voltage $\Delta V_{TH}/\Delta T_{si}$ is equal to 100 mV/nm. Since thin-film SOI wafers with a σT_{Si}<0.2 nm can nowadays be produced , threshold voltage variations on the order of σV_{TH}<35 mV can be expected at wafer level, provided a lithography width control of 0.5 nm. The use of a thinner EOT decreases the sensitivity of V_{TH} on dimensions.

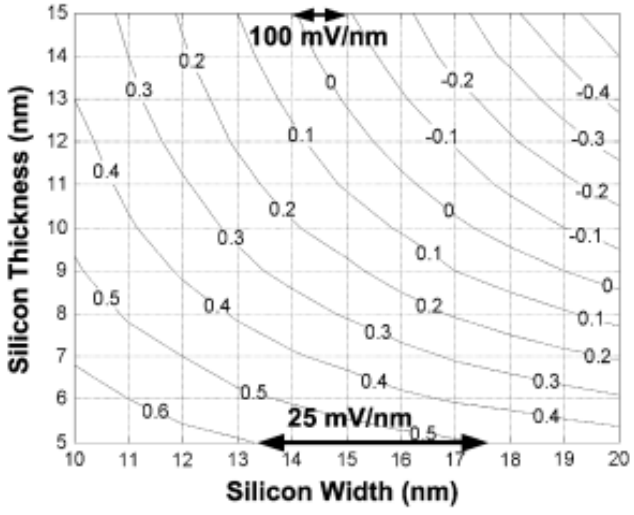

Fig.2.12: Contour plot of threshold voltage in an n-channel junctionless device with T_{ox} = 1 nm and $N_D = 2x\ 10^{19}$ cm^{-3} , as a function of nanowire thickness and width.

2.4.Fabrication of JLFET

Junctionless gated resistor devices were made using standard SOI wafers. The SOI layer was thinned down to 15 nm and patterned into nanoribbons using e-beam lithography. Using a combination of plasma lateral overetch and gate oxidation, the thickness of the nanowires was reduced to nm, and their width was reduced to dimensions as small as 5 nm. Ion implantation was used to dope the devices uniformly N^+ or P^+ with a concentration of 1 x 10^{19} – 5 x 10^{19} cm^{-3} , which is a typical LDD doping concentration, to realize N-channel and P-channel devices, respectively.

Figure 2.13 shows the TEM cross-section of a several devices with different widths. Due to processing parameters the cross-section of the devices is not a rectangle, but rather a trapezium or even a triangle. Devices with a silicon thickness of approximately 10 nm and a width ranging from 5 to 30 nm were made.

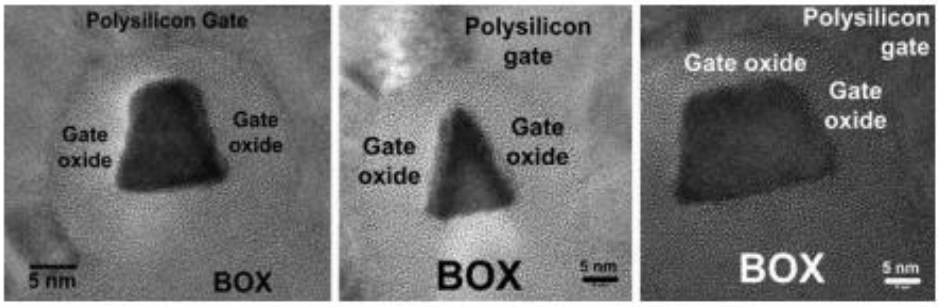

Fig.2.13: TEM cross section of a junctionless transistors with increasing width from left to right

2.5.I-V Characteristic Curve of JLFET

Junctionless transistors have excellent on–off switching behavior and an on/ off ratio larger than 10^5 for V_{DD}=0.5 V (Fig.2.14). The off current could not be measured as it is lower than 1 fA, which is the sensitivity limit of the measuring apparatus.

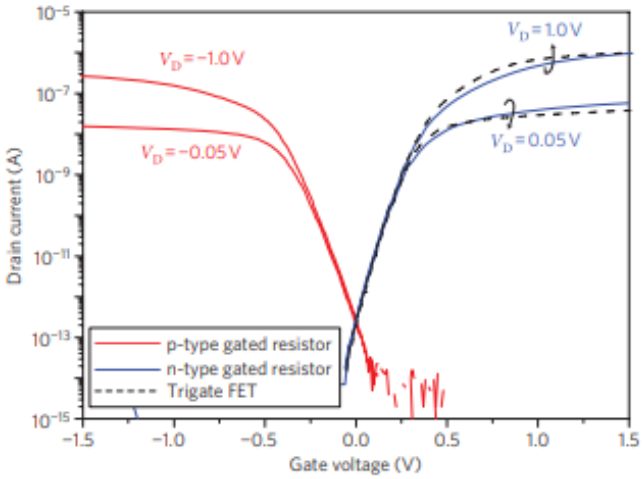

Fig.2.14: Drain current versus gate voltage for N - and P- type junctionless gated resistors and a trigate inversion-mode, N-channel MOSFET. N_D = 1 x 10^{19} cm^{-3} in the junctionless device. L = 1 µm.

2.6. Mobility of charge carriers in JLFET

Mobility in junctionless devices is largely dominated by ionized impurity scattering, and acoustic phonons seem to have little effect on mobility. Figure 2.15 shows the mobility, measured from the peak of transconductance as a function of gate voltage, in trigate SOI MOSFETs and in junctionless transistors. The inversion-mode trigate devices have either an undoped channel (N_A = 5x10^{15} cm^{-3}) or a doped channel (N_A =5x 10^{17} cm^{-3}). In the undoped devices the peak mobility is 350 cm^2 /Vs at room temperature, but drops by 36% as temperature is increased to 200C. The doped devices have a lower room-temperature mobility (220 cm^2 /Vs) which also drops by approximately 36% as temperature is increased to 200C. The heavily doped (N_D =2x10^{19} cm^{-3}) junctionless devices have a much lower room-temperature mobility: 80 cm^2 /Vs. However, the mobility decreases <7% as temperature is increased to 200C. This clearly illustrated the fact that mobility is limited by ionized impurity scattering and is relatively insensitive to phonon scattering in heavily doped junctionless transistors.

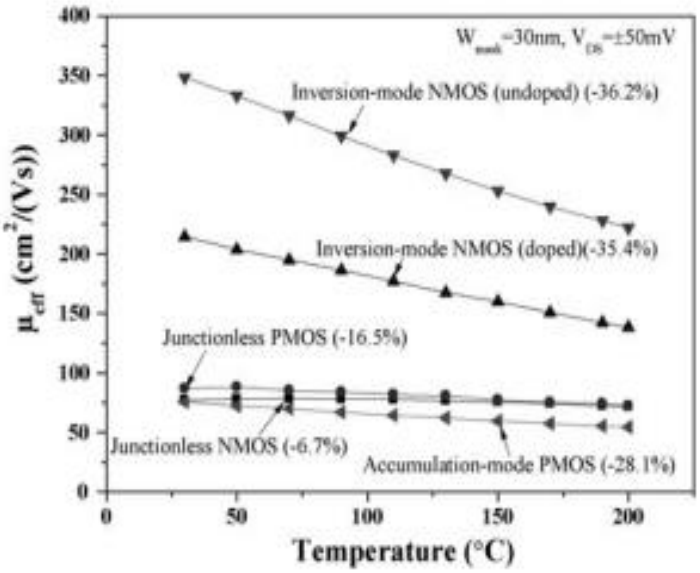

Fig.2.15: Mobility in heavily doped junctionless transistors and in regular trigate MOSFETs with doped and undoped channels, as a function of temperature.

2.7.Comparative study between JLFETs and MOSFETs

- **Current Drive**: In junctionless transistors, the electric field perpendicular to the current flow is substantially lower than in ordinary inversion - mode or accumulation-mode field-effect transistors. Because this electric field reduces inversion channel mobility in metal-oxide semiconductor transistors, junctionless transistors may have a benefit in terms of current drive for manometer-scale complementary metal-oxide semiconductor applications. When quantum confinement is present, this observation still holds true. A Junction transistor's large carriers in the channel region act as a barrier to carrier scattering, but a Junctionless transistor does not have this problem, resulting in a high current drive.
- **Structural Complexity at deep sub-micron level:**A classical MOS transistor comprises two PN junctions called the source junction and the drain junction.The formation of such junctions involves extremely high doping concentration gradients, and very low thermal budget processing must be used. Flash annealing techniques are currently used to heat silicon for a very short time period in order to minimize diffusion, but even in total absence of diffusion, ion implantation and other doping techniques do not achieve perfectly abrupt junctions with infinite concentration gradients. The formation of ultrashallow junctions with high doping concentration gradients has become an increasingly difficult challenge for the semiconductor industry. On the other hand ,Junctionless transistors (also called gated resistor) have

no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires.

- **Short Channel Effects(SCE):** . In a ‘‘regular’’, inversion-mode trigate device, assuming the distance between the source and drain junctions is exactly equal to the physical gate length (Fig.2.4a), the presence of PN+ junctions creates a reduction of the effective gate length, resulting in a shortchannel effect (SCE). This effect has been quantified using the voltage-doping transformation model (VDT). The VDT can be used to translate the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters. . The decrease of threshold voltage with decreased gate length is a well-known short-channel effect called the ‘‘threshold voltage roll-off’’. The SCE is illustrated in Fig.2.16 (a) for an inversion-mode transistor. In a junctionless device in the off state, the electrostatic squeezing effect causes the distance between the non-depleted source and drain regions to be larger than the physical gate length (Fig.2.16 b). This is a beneficial factor that reduces short-channel effects and can possibly reduce source-to drain direct tunneling in very short-channel devices.

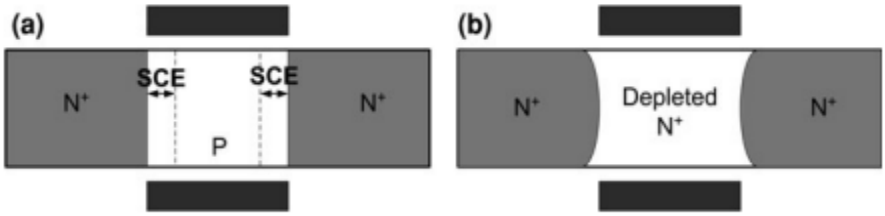

Fig.2.16: Illustration of effective channel length in an inversion-mode device (a) and (b) a junctionless transistor.

- **Robustness against doping fluctuations:** With the statistical distribution of doping impurities is the variation of effective channel length, L_{eff}, defined as the distance between the source junction and the drain junction . This is illustrated in Fig.2.17, the statistical nature of the doping atom distribution at the source and drain junctions causes the effective channel length to fluctuate from device to device. These fluctuations are inherent to the ion implant and diffusion processes. Furthermore, dopants from the source and drain can scatter in the channel region and influence the threshold voltage. In the junctionless device, there is no gradient of doping concentration between source, channel and drain. The effective channel length can no longer be

defined as the distance between two junctions. The effective gate length is basically equal to the physical gate length, although it may be somewhat longer when the device is turned off.

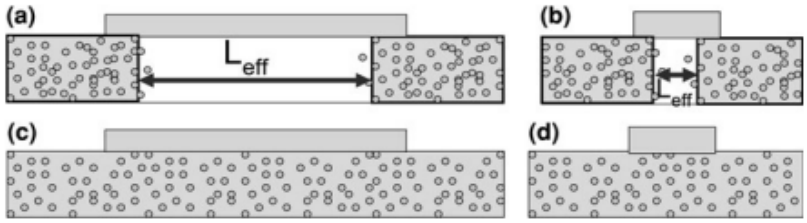

Fig.2.17: Scattering of source and drain doping impurities in the channel of (a) a long-channel and (b) a short-channel inversion-mode MOSFETs; (c) long-channel and (d) short-channel junctionless devices

- **Subthreshold Slope:** The subthreshold slope at room temperature JLFET is 64 mV/decade, and it remains very close to the "ideal" value of (kT/q) ln(10) over the temperature range 225–475 K. Figure 2.18 shows the evolution of subthreshold slope, SS (in mV/ decade) at V_{DS}=50 mV in a N-channel inversion-mode trigate MOSFET and a junctionless gated resistor. The subthreshold slope of both devices follows the following law: SS = n (kT/q) ln(10) with n = 1.066, which is very close to the lowest theoretical limit (n = 1).

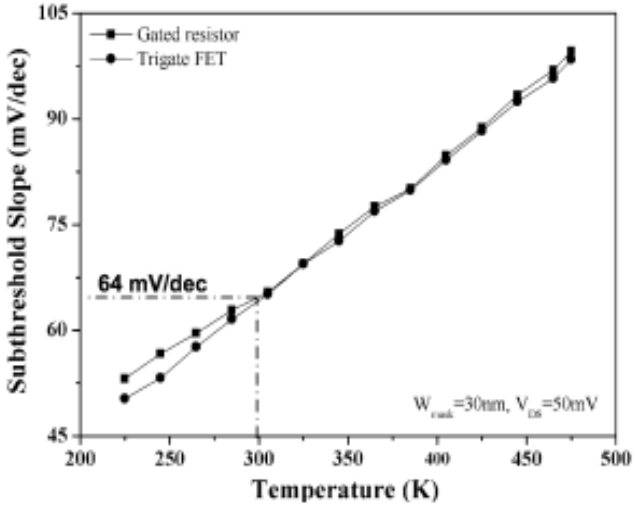

Fig.2.18: Measured subthreshold slope versus temperature in a junctionless gated resistor and an inversion-mode trigate MOSFET.

2.8.Adverse effects of high level doping in JLFET

2.8.1.Mobility Degradation:

The effect of the high channel doping concentration of junctionless gated resistors is on carrier mobility. It is well known that ionized impurity scattering degrades carrier mobility. The electron mobility in silicon is shown in Fig.2.19 as a function of donor atom concentration, N_D. The mobility drops from 1,400 cm^2 /Vs in lightly doped silicon to 80 cm^2 /Vs for $N_D=10^{19}$ cm^{-3} .

Channel mobility in inversion-mode devices is affected by the (vertical) electric field in the channel, E_{eff}. Since E_{eff} increases when the effective oxide thickness, EOT, is reduced, surface channel mobility has steadily decreased in successive technology nodes and would now be well below 100 cm^2 /Vs at the 45-nm node, if it wasn't for the introduction of strained silicon technology.

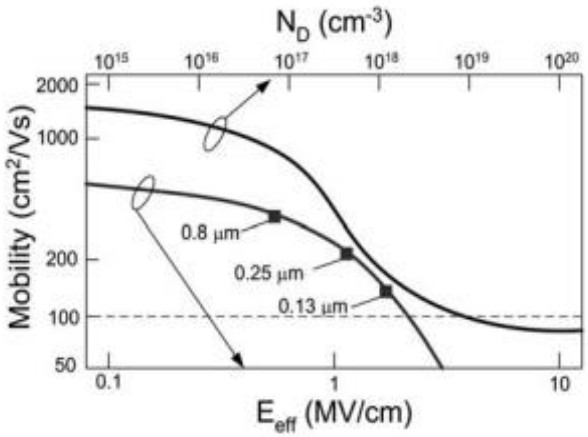

Fig.2.19: Electron mobility in silicon as a function of donor doping atom concentration and as a function of electric field in the channel. The latter curve shows the mobility/ field for several key technology nodes.

2.8.2.Random Dopant Fluctuations(RDF):

Doping fluctuations are a serious problem in nanoscale devices. Even in the so called ''undoped'' channels the doping concentration is not equal to zero but to a value of a few 10^{15} cm^{-3} . This means that there a chance of approximately one in a thousand to find a (boron) doping atom in a device with a channel volume of 10 x 10 x 10 nm^3 .

Random dopant fluctuation (RDF) is a type of process variation caused by changes in the concentration of implanted impurities. RDF in the channel region of MOSFET transistors can change the transistor's characteristics, particularly the threshold voltage. Because the total amount of dopants in contemporary process methods is lower, and the insertion or removal of a few impurity atoms can drastically modify transistor's electrical characteristics, and thus RDF has a stronger effect. RDF is a type of local process variation in which two identical transistors on a same silicon die with similar dopant concentrations may have considerably different dopant concentrations. Fig 2.20 depicts the variations in the structure of a scaled device.

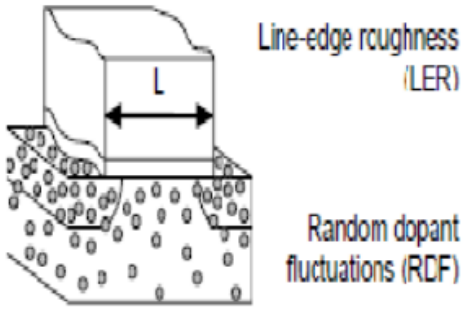

Fig.2.20: Primary sources of variation in a nanoscale device

These variations interact with one another, affecting every aspect of circuit performance. The RDF effect is primarily a random effect. The uncertainty in charge location and numbers, such as the discrete placement of dopant atoms in the channel region that follow a Poisson distribution, causes this well-known phenomenon. The overall number of channel dopants reduces as the device size shrinks, resulting in a wider fluctuation in dopant quantities and a considerable impact on threshold voltage shown in the Fig 2.21 .

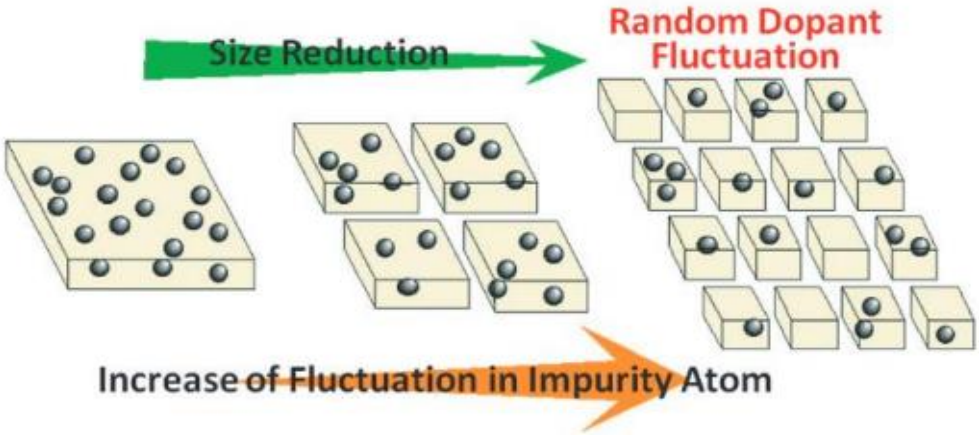

Fig.2.21: Appearance of RDF increases with reduction in size of semiconductor bulk.

Variability of junctionless field-effect transistor (JL-FET) performance due to random dopant fluctuation (RDF) is projected to be a serious problem when scaled to nanoscale dimensions as the total number of dopant atoms becomes increasingly discretized. While line edge roughness (LER)-induced variability was already shown to be significant for junctionlessFinFETs(JL-FinFETs) at even small rootmean-square amplitudes (LER) , there has not been an equivalent study on the effect of RDF for such devices.

2.9.Work Progress in JLFET:

Few of the extensive research reports on JLFET are mentioned in the following list:

- The idea of JLFET was first published in a patent filled by Polish-American physicist and inventor Julius E. Lilienfeld in, "Method and Apparatus for Controlling Electric Currents," in 1926 in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Lilienfeld Transistor is the basic structure of the evolved JLFET.[69]
- First physical design of JLFET was patented in 2009 by Prof. J.P. Colinge in the paper entitled “Junctionless Transistor” communicated about the proposed novel device and all the limitations that are associated with FET structures when they are scaled sown to 10nm. The proposed device named as Junctionless FET or gate resistor, has simpler fabrication and involves fewer steps as compared to that of MOSFET.[2]
- Lee et. al. in 2010 studied the junctionless transistor for deep submicron technology node. They have simulated both inversion mode ($N\text{-}P^{+}\text{-}N$) and accumulated mode junctionless ($N^{+}\text{-}N^{+}\text{-}N^{+}$) transistor and concluded that junctionless FET have improved short channel characteristics.[1]
- In the 2010 papers by Colinge et al and Lee et al. , first reports of electrically measured JNTs(Junctionless Nanowire Transistors) in Si channel were shown, including both n-type and p-type transfer and output characteristics for L = 1 µm, W= 20 nm.[6]
- Important early reports on the JNT in 2010 include the work by Colinge et al, where the electric field perpendicular to the current flow is found to be significantly lower in junctionless transistors which may be another advantage for this device type.In addition, the same group reported how the JNT can be fabricated to yield low subthreshold slopes in combination with impact ionization effects.[5]

- In the following year of 2010,many research reports were documented . Renan DoriaTrevisoli et al . presented a physically based analytical model for the threshold voltage in junctionless nanowire transistors (JNTs). The model was based on the solution of the two-dimensional Poisson equation and included the dependence on JNT width, height and doping concentration. The quantum confinement was also taken into consideration in the model formulation.[62]
- In 2012, Park,Chan-Hoon et al. fabricated n-channel junctionless nanowire transistors with gate lengths in the range of 20–250 nm, and have compared their electrical performances with conventional inversion-mode nanowire transistors. The junctionless tri-gate transistor with a gate length of 20 nm showed excellent electrical characteristics with a high I_{on}/I_{off} ratio (>106), good subthreshold slope (∼79 mV/dec), and low drain-induced barrier lowering (∼10 mV/V). The simpler fabrication process without junction formation results in improved short-channel characteristics compared to the inversion-mode devices, and also makes the junctionless nanowire transistor a promising candidate for sub 22-nm technology nodes.[63]
- In the same year of 2012, Razavi et al investigated two important device metrics, intrinsic gate-delay and energy-delay product of triple-gate junctionless nanowire transistors (JNTs) with gate lengths from 22 nm down to 15 nm, for different channel doping concentrations and compare them with those of triple-gate inversion-mode (EVI) nanowire field-effect transistors. Our study shows although intrinsic gate-delay is larger in junctionless devices compared to those of EVI devices, since the 16 switching energy is smaller in JNTs, energy-delay product is almost identical for both junctionless and IM devices.[64]
- In the same year, Ting-Kuo Kang investigated the piezoresistive effect in n-type silicon nanowires on silicon-on-insulator wafers, also called junctionless nanowire transistors (JNTs). A marked change in the subthreshold drain current for strained JNTs was observed that could be attributed to strain-induced interface state modification, due to an increase in the interface state for tensile strain or a decrease in the trap activation energy for compressive strain. Through many long-time cycles of compressive and released strain, the electromechanical response of subthreshold IDS with time was found, supporting piezo-resistance effect. [65]

- Duarte et al. formulated a compact model of quantum electron density at the subthreshold region is derived for junctionless (JL) double-gate (DG) FETs. The proposed quantum model is obtained under two different quantum confinement conditions. One is for a case of a thick channel and a heavily doped channel, where quantum confinement effects (QCEs) are modeled by a 1-D quantum harmonic oscillator. The other is for a case of a thin channel, where QCEs are modeled by the use of a 1-D quantum well surrounded by high potential barriers and an energy correction term coming from the depletion charge. It is shown that, regardless of the channel thickness, the quantum confinement is higher in JL than in inversion-mode (IM) DG FETs.[66]
- In the following year,Razavi and Fagas evaluated the performance of III-V inversionmode and junctionless nanowire field-effect transistors using quantum simulations. Specifically they modelled InAs, GaSb, and GaAs devices. One of the main conclusions of that modelling work was that III-V junctionless nanowire transistors are more immune to short-channel effects than conventional inversion-mode III-V nanowire field-effect transistors.[15]
- In the year of 2014, Yu et al. reported p-type JNT with a Ge channel fabricated by a CMOS compatible top-down process . At that time the transistors exhibited the lowest Subthreshold Slope to date for Ge junctionless devices. The devices with a gate length of 3 μm exhibited a subthreshold slope of 216 mV/dec with an I_{on}/I_{off} current ratio of 1.2×103 at V_D = -1V and DIBL of 87 mV.The process consisted of electron beam lithography and reactive ion etch for patterning, a GeO_2 passivation step, ALD-based Al_2O_3 deposition, and gate formation and metallization thereafter.[11]
- In 2014 Song et al. reported the first experimental demonstration of III-V based JNTs using a gate-all-around architecture based on GaAs. The fabricated devices were scaled down to nanowire widths of 9 nm and gate lengths of 80 nm. The authors stressed that the electrical performance of the devices was particularly promising for low power RF applications.[16]
- In 2015,Sun et al. fabricated JNTs on ultra-thin-body germanium-on-insulator substrates using a simple Si-compatible top-down process. The devices with gate lengths and widths less than 100 nm, exhibited I_{on}/I_{off} ratios of ~ 105 with a 1 V supply voltage .[12]

- In parallel to the development of the Ge JNTs, many groups worked on the evaluation and demonstration of III-V based JNTs.In 2015 Leung et al. performed a very extensive device performance analysis based on TCAD, of $In_{0.53}Ga_{0.47}As$ channel JNTs. For example, n-type $In_{0.53}Ga_{0.47}As$ has some advantages over p-type $In_{0.53}Ga_{0.47}As$and Si in terms of JNT sensitivity to process variations. They also studied the impact of random dopant variation on it.[17]
- In the same year of 2015, Asthana Pranav Kumar et al. presented a GaSb/InAsjunctionless tunnel FET and investigate its static device characteristics. The proposed structure presents tremendous performance at a very low supply voltage of 0.4 V ,at a 17 temperature of 300 K, gate length of 20 nm, HfO_2 gate dielectric thickness of 2 nm, film thickness of 10 nm, low-k spacer thickness of 10 nm. The key idea was to the present device architecture, which can be exploited as a digital switching device for sub 20 nm technology. Numerical simulations resulted in an I_{OFF} of $\sim 8 \times 10^{-17}$ A/μm, I_{ON} of ∼9 μA/μm, I_{ON}/I_{OFF} of $\sim 1 \times 10^{11}$, subthreshold slope of 9.33 mV/dec and DIBL of ∼87 mV/V.[67]
- Djara et al. reported device performance of a tri-gate $In_{0.53}Ga_{0.47}As$-on-insulator (InGaAs-OI) JNT architecture. The fabricated devices had a 20-nm-thick $In_{0.53}Ga_{0.47}Asn$ channel doped to $10^{18}/cm^3$. The authors of that work highlighted that the tri-gate InGaAs-OI JNT showed the best compromise in terms of threshold voltage, SS and DIBL compared to the other III–V JNTs architectures reported to date.[18]
- In the following years, S. Sahay and M. J. Kumar proposed a double gate junctionless FET (DGJLFET) with an extended back gate (EBG) architecture for significantly improved performance in the sub-10-nm regime also demonstrated the quantum confinement-induced bandgap widening diminishes the parasitic bipolar junction transistor (BJT) action and, therefore, facilitates the scaling of the conventional DGJLFETs to the sub-5-nm channel regime where the quantization effects are significant.[19]
- In the year of 2017, Thirunavukkarasu et al. experimentally demonstrateda silicon junctionless (JL) trench gate-all-around (GAA) nanowire field-effecttransistor with an atomically thin channel thickness of 0.65 nm and a very thin oxidewith a thickness of 12.3 nm. Experimental results indicated that this device with achannel thickness of 0.65 nm achieves a sub-threshold slope (SS) of 43

mV/decade, which is the best yet achieved by any reported JLFET. Owing to the atomically thinchannel, this device has an extremely high I_{ON}/I_{OFF} current ratio of >108.Furthermore, the atomically thin channel GAA JLFET exhibits a low thresholdvoltage (V_{TH}) variation and negligible drain-induced barrier lowering(DIBL < 0.4 mV/V). [20]

- In the same year, DehdashtiAkhavan et al studied the influence of random dopantfluctuations (RDF) on the statistical variability of the electrical characteristics ofn-channel silicon junctionless nanowire transistor (JNT) using three dimensionalquantum simulations based on the non-equilibrium Green's function (NEGF)formalism.[21]
- In the following years,S. Berrada et al. used the Non-Equilibrium Green's Functionformalism to study the dependence of the threshold voltage variability on the cross-section shape and the gate length in Junction Less Field Effect Transistors.[22]
- M.K.A Titu et al., In their work, by employing self-consistent solver studiedCapacitance-Voltage (C-V) characteristics and the threshold voltage variation ofp-type Rectangular Gate Junctionless Field Effect Transistor (RG-JLFET) andDouble Gate Junctionless Field Effect Transistor (DG-JLFET). The self consistentsolver solves Schrodinger-Poisson equations with appropriate boundary conditionsand takes wave function penetration and other quantum mechanical effects intoaccount.[61]
- Recent years include work of Bora ,N. et al. presented an analytical model for ultrascaled symmetric double gate (SDG) nanowire junctionless field effect transistor(JLFET), which includes charge quantization in all the regions of operation. Thismodel was based on a first-order correction for the confined energies obtained bysolving the Schrodinger's equation. The model predicted the quantum mechanicaleffects (QME) on the surface potential, drain current and transconductance for ahighly doped and extremely thin silicon layer of thickness down to 4nm.[68]
- Bora ,N. et al. presents the effects of quantum confinements on the surfacepotential, threshold voltage, drain current, transconductance, and drain conductanceof a Dual Material Double Gate Junctionless Field Effect Nanowire Transistor(DMDG-JLFENT). The carrier energy quantization on the threshold

voltage of aDMDG-JLFENT is modeled, and subsequently, other parameters like drain currentwere analytically presented. The QME considered here is obtained under thequantum confinement condition for an ultra-thin channel, i.e., below 10 nm of Sithickness.[23]

- In our current year,Bolokian, M. et al. suggested a junctionless field effect transistorwith an embedded p-type layer (EPL-JLT) near the drain channel side, employingcalibrated structure simulations to obtain a complete depletion region in a 6 nmchannel length. The incorporation of a p-type layer improves leakage current (I_{OFF})and subthreshold swing (SS) for a 6 nm regime structure at 5.9 eV work function(WF) while the ON current (I_{ON}) diminishes a little. This considerable achievementin the leakage current enables obtaining multiple threshold voltages (V_{TH}) byadjusting the gate WF. The proposed device has a leakage current of 1 nA μm^{-1} evenat a 5.1 eV WF. The scaling of the EPL-JLT for different channel lengths isinvestigated.[24]

2.10. Work Ahead

From the chronological literature survey on Junctionless transistors(JLFET) since its birth on 2009,numerous investigations and simulations were performed to explore the physical properties and characteristics of the new born novel device,JLFET.After vast researches on JLFET, we precisely modeled I-V Characteristics of JLFET and also diminished Sub-threshold Slope well below 60mV/dec at deep sub-micron level.In addition to that,short channel effects on JLFET were also extensively studied and alleviated problems of SCE to a large extent with significant reduction in DIBL.

But most of the proposed models lacked inclusion of Quantum Confinement Effects which is a quite significant factor in such deep submicron levels,Charge confinement due to Quantum Confinement effects strongly influence physical parameters of JLFET.Variation of Threshold Voltage,Subthreshold Slope and other parameters due to Quantum effects should be considered for evolving a more precise analytical model of JLFET.

Doping Fluctuation (RDF) has detrimental effects on the performance of JLFET at deep submicron levels.A few papers regarding effects of RDF on JLFET were studied without inclusion of quantum confinement effects.Thus work remains to be done regarding impact of RDF on variation of physical parameters of JLFET along with inclusion of Quantum Effects due to dimensions scaling.

Chapter 3

Device Simulation of JLFET

We have simulated short channel DG SMG JLFET using Silvaco TCAD Atlas and observed physical properties of JLFET under different modes of operation.

Following specifications of DG SMG JLFET are used in our simulation :

Device Parameters	Value
$t_{ox}(Gate\ Oxide\ Thickness)$	1nm
$\epsilon_0(Permittivity\ of\ Free\ Space)$	$8.854\text{x}10^{-12}\text{m}^{-3}\ \text{kg}^{-1}\text{s}^4\text{A}^2$
$\epsilon_{Si}(Permittivity\ of\ Si)$	$11.8\epsilon_0$
$\epsilon_{ox}(Permittivity\ of\ Oxide)$	$3.97\epsilon_0$
χ_m(Electron Affinity)	4.17 eV
$t_{Si}(Si\ Substrate\ Thickness)$	2nm
$L_G(Gate\ Length\ of\ JLFET)$	20nm
$N_D(Donor\ Concentration\ in\ Si)$	$5\text{x}10^{19}cm^{-3}$
$L_S(Source\ Length\ of\ JLFET)$	2.5nm
$L_D(Drain\ Length\ of\ JLFET)$	2.5nm
$W_{Si}(Width\ of\ Silicon\ Bulk)$	2nm
$L_{Si}(Length\ of\ Silicon\ Substrate)$	25nm
ϕ_m(Work Function of n^+ Poly Si Gate)	4.7eV
$V_{DS}\ (Drain\ to\ Source\ Voltage)$	0.05V
$a\ (Lattice\ Constant\ of\ Si)$	5.429Å
$m_0\ (Rest\ mass\ of\ e^-)$	$9.11\text{x}10^{-31}$kg
$m_l\ (Longitudinal\ Effective\ mass\ of\ e^-)$	$0.92m_0$
$m_t\ (Transverse\ Effective\ mass\ of\ e^-)$	$0.19m_0$

Table 3.1. Device Parameters for simulation of JLFET.

3.1 Results and Discussion

We have simulated a short channel Double Gate (DG) Single Material Gate(SMG) Junctionless Transistor presented in Figs. 3.1 and 3.2 using Silicon as bulk material with channel length $L_G\ as\ 20nm$, bulk thickness $t_{Si}\ as\ 2nm$, bulk width $W_{Si}\ as\ 2nm$, oxide thickness $t_{ox}\ as\ 1nm$ and Donor Dopant Density N_D of $5x10^{19}\ cm^{-3}$.

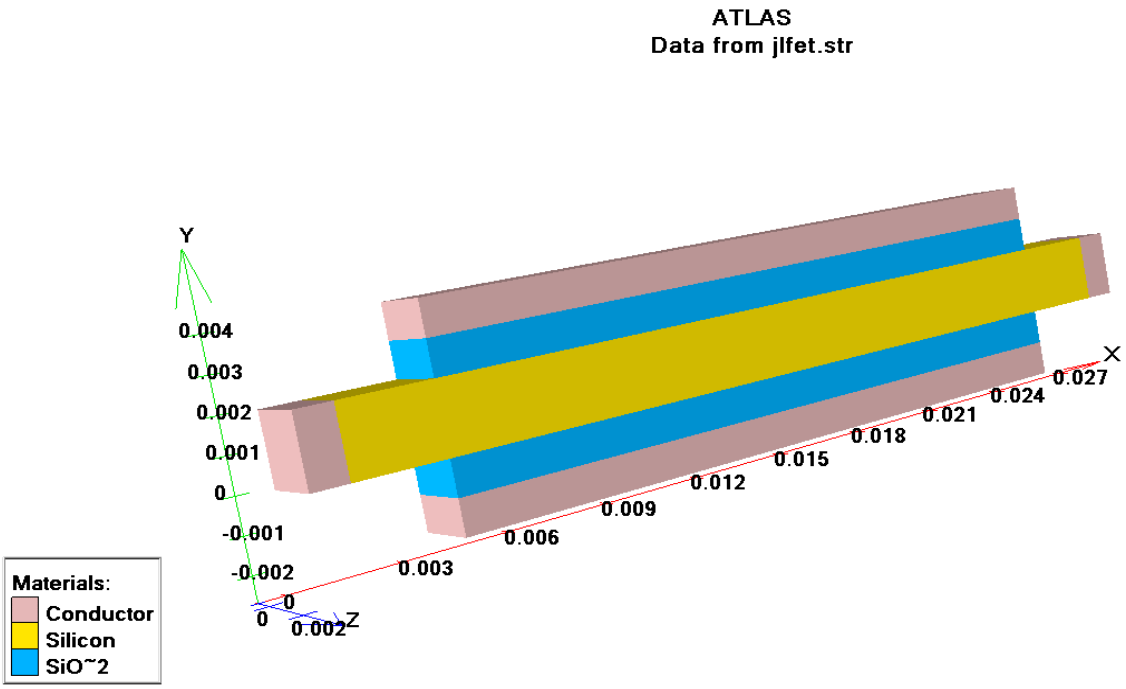

Fig. 3.1: 3D Device Structure of DG SMG JLFET.

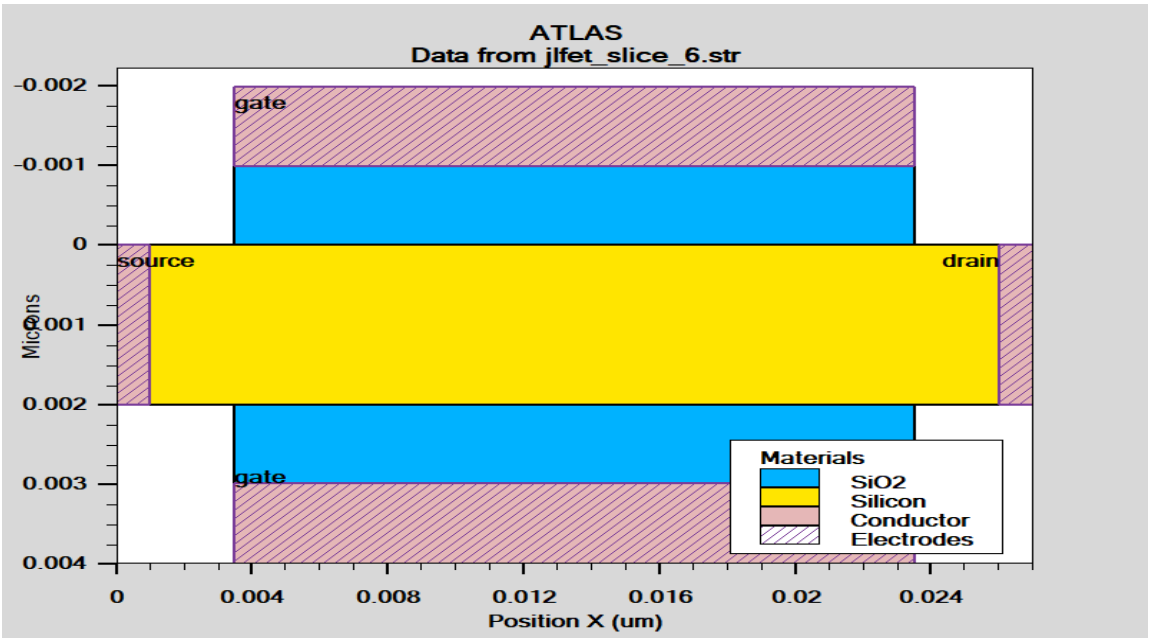

Fig.3.2: Cross Sectional View of DG SMG JLFET.

We would be using bulk conduction regime of JLFET for threshold voltage and sub threshold drain current calculations, so it is a good approximation to use bulk mobility of electrons ($\mu_n = 1350\ cm^2V^{-1}Sec^{-1}$)instead of surface mobility.

We would now analyze behavior of JLFET in different operation modes.

Depletion Mode:

We provided a negative bias Gate Voltage ($\boldsymbol{V_{GS} = -0.6V, V_{DS} = 0.5V}$) and observed changes in Physical Parameters of JLFET under Depletion Mode.

InFig.3.3 and Fig.3.4,we could observe symmetry in conduction band energy due to symmetric DG JLFET structure.

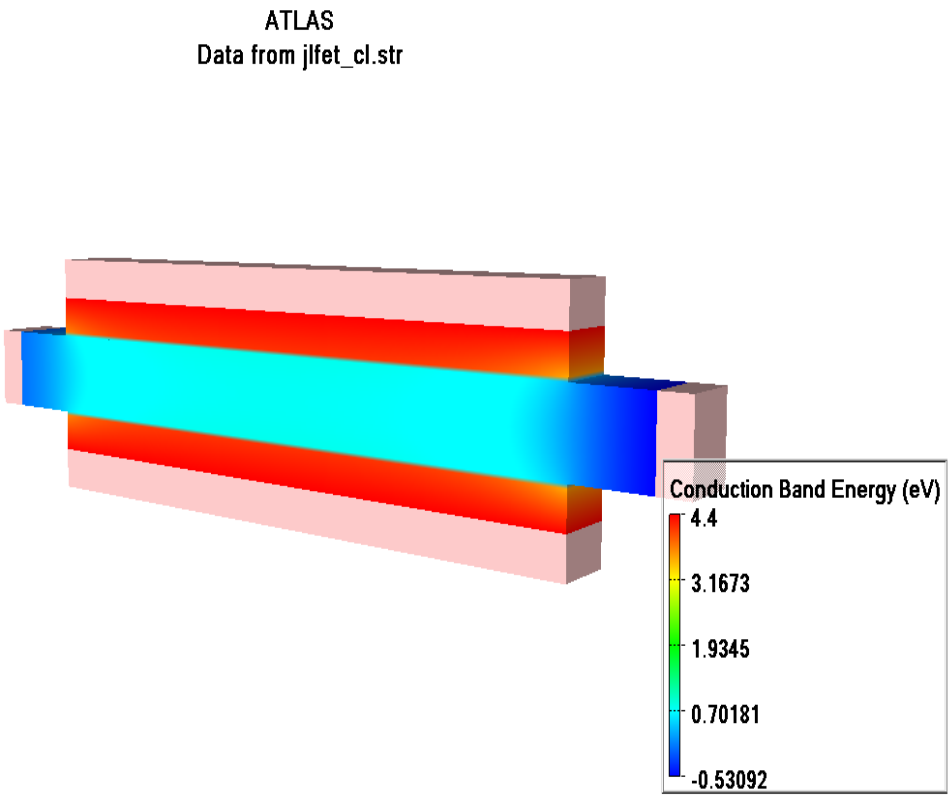

Fig.3.3: Conduction Band Energy in JLFET under Depletion Mode(3D View).

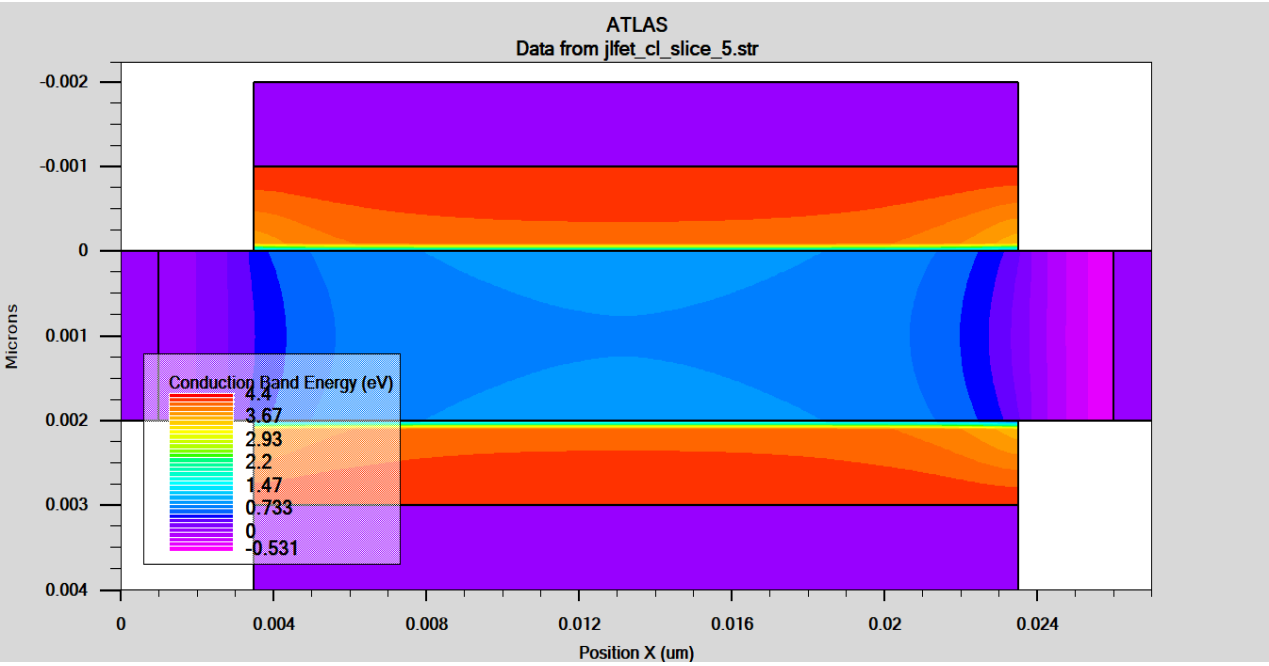

Fig.3.4: Conduction Band Energy in JLFET (Cross Sectional view) under Depletion Mode.

Figs.3.4. and 3.5. depict symmetric upward band bending of Conduction Band Energy near surface region throughout the channel length.

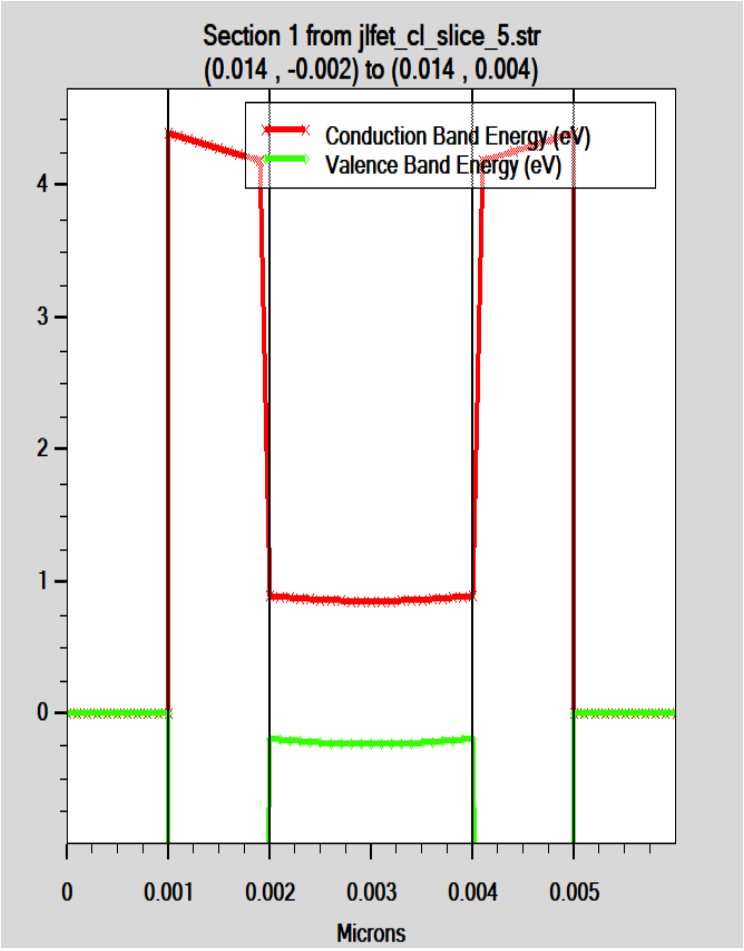

Fig.3.5: Energy Band Diagram of JLFET under Depletion Mode.

We could see from Fig 3.4. and 3.6, a considerable conduction band energy barrier around the bulk region would prevent drift flow of electrons from source to drain despite of having a considerable drain voltage.

Fig.3.6. shows Conduction Band Energy barrier is quite significant in the central line channel region that would prevent bulk conduction of current through drift mechanism. Diffusion mechanism is insignificant in JLFET because electrons are the majority charge carriers responsible for current conduction.

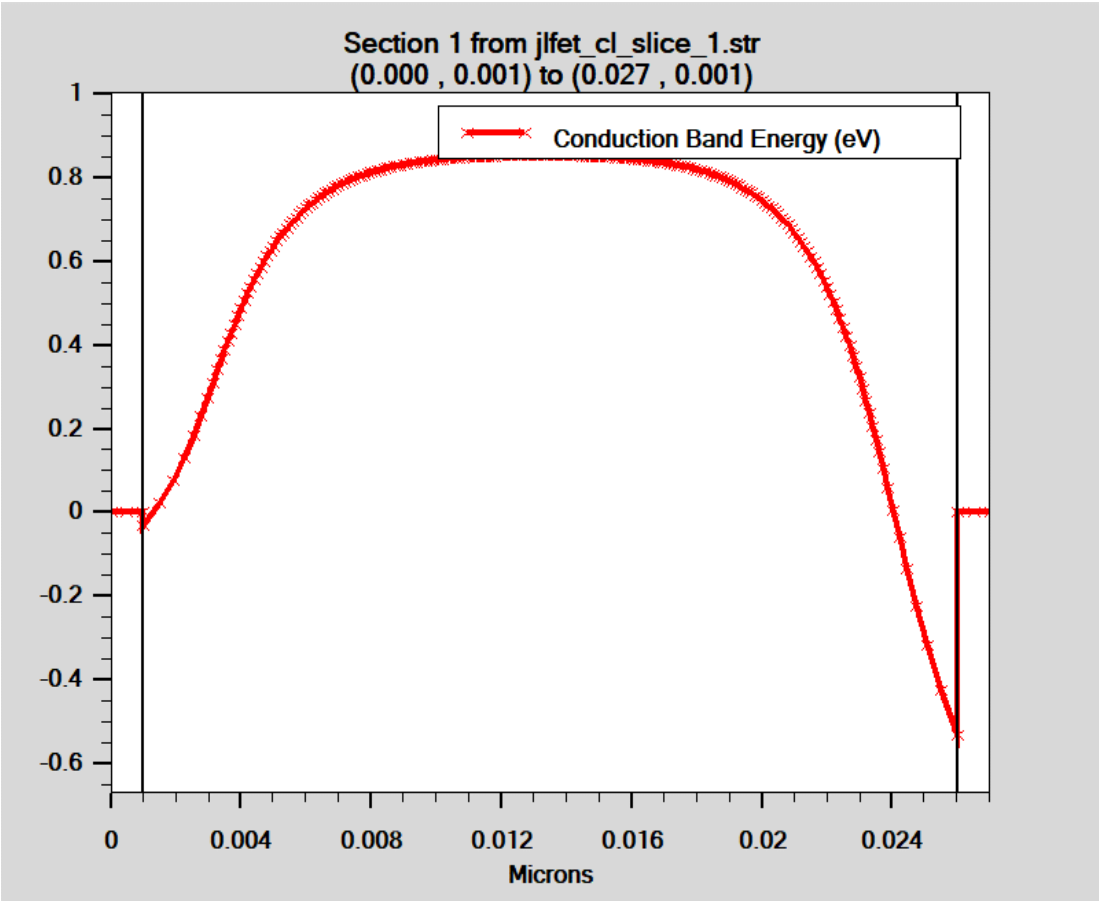

Fig.3.6: Variation of Conduction Band Energyacross the central line channel of JLFET under Depletion Mode.

If we observe conduction band energy distribution across oxide layers in Fig.3.4, a gradient in conduction band energy instead of a constant value is found. It is also shown by a gradual rise of conduction band energyin Fig.3.5 appearing for the space charge apprising from ionization of dopant atoms in Silicon bulk.On the contrary, the fixed oxide trap charges and interface charges depicted in the oxide regions of Fig.3.7 are responsible for the abrupt rise in conduction band energy in oxide regions.

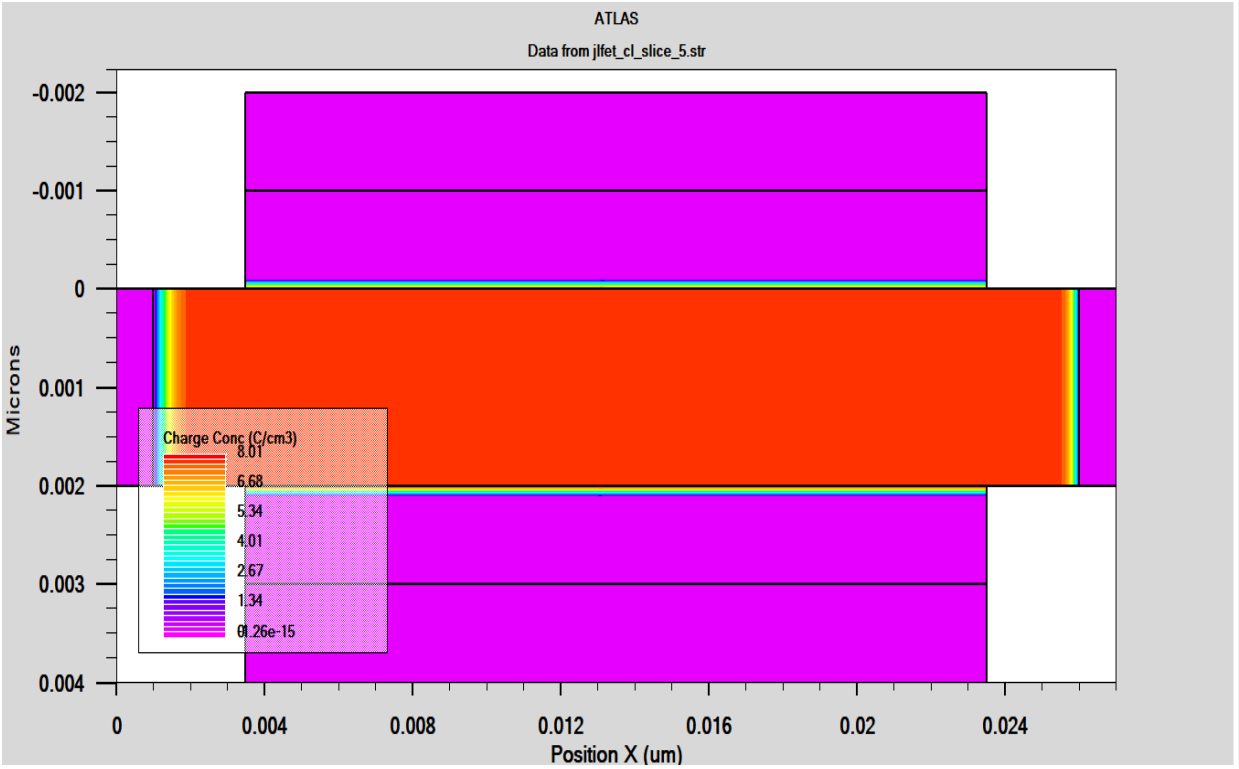

Fig.3.7: Charge Concentration in JLFET under Depletion Mode.

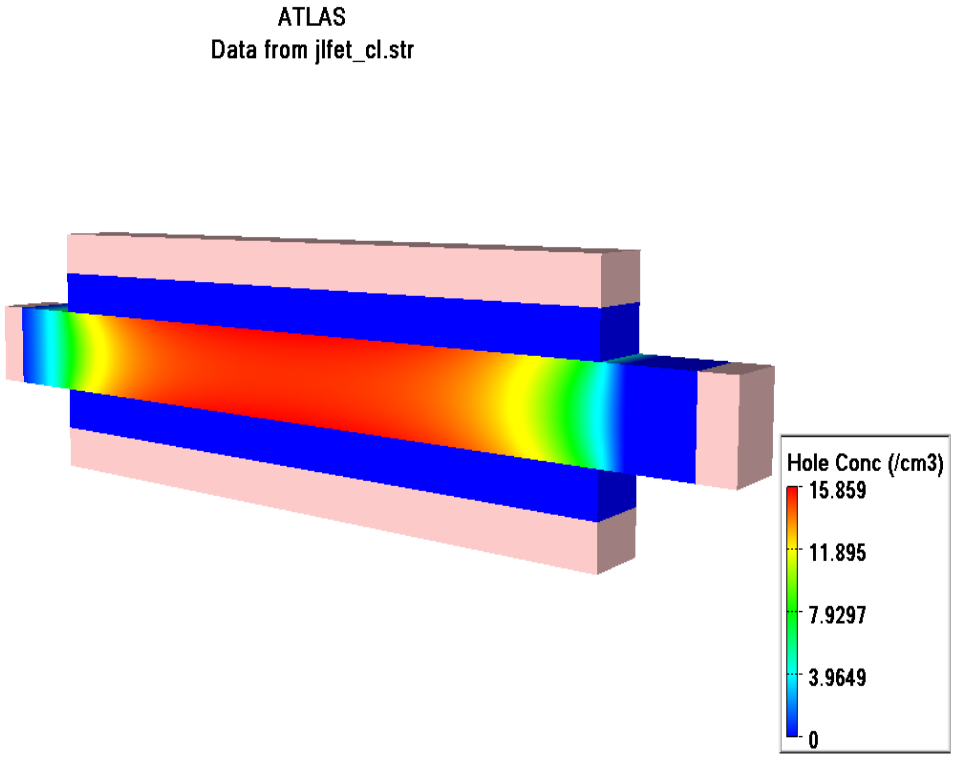

Fig.3.8: Hole Concentration in JLFET under Depletion Mode

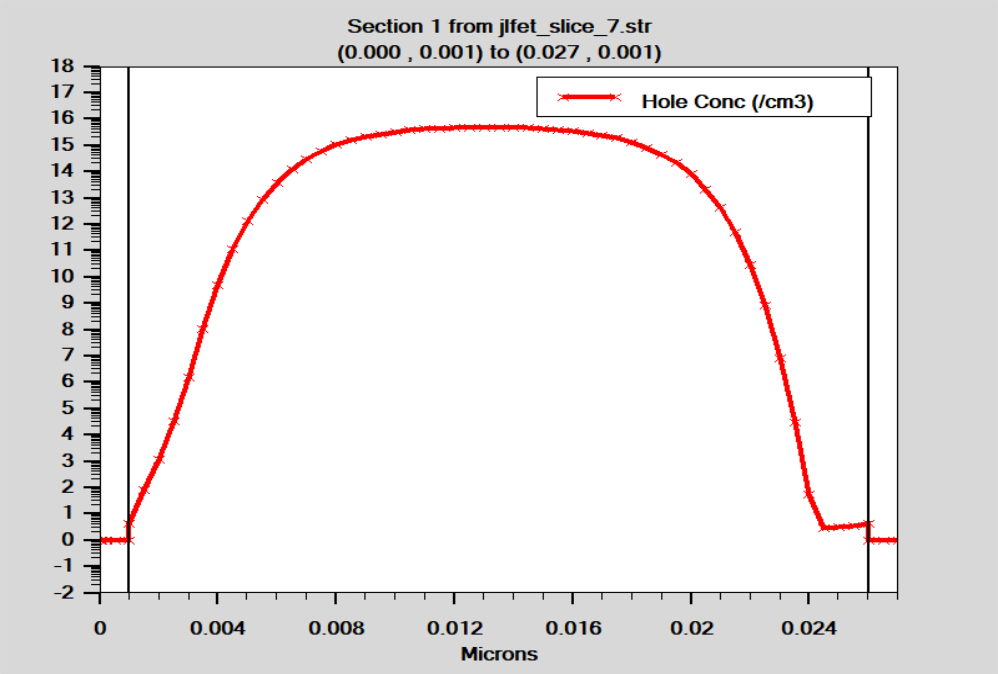

Fig.3.9: Hole Concentration in JLFET across the central line channel region of JLFET under Depletion Mode.

Under depletion mode,bulk region of JLFET is depleted of electrons as shown in Figs.3.10and 3.11rather accumulated by holes.There is a gradual increase in hole concentration as we move towards the channel region from either side due to symmetry in source and drain regions (symmetric for $V_{DS} = 0$). Hole concentration is minimum in source and drain regions and gradually rises to maximum value in the bulk region across the channel, as evident from Figs.3.8. and 3.9.

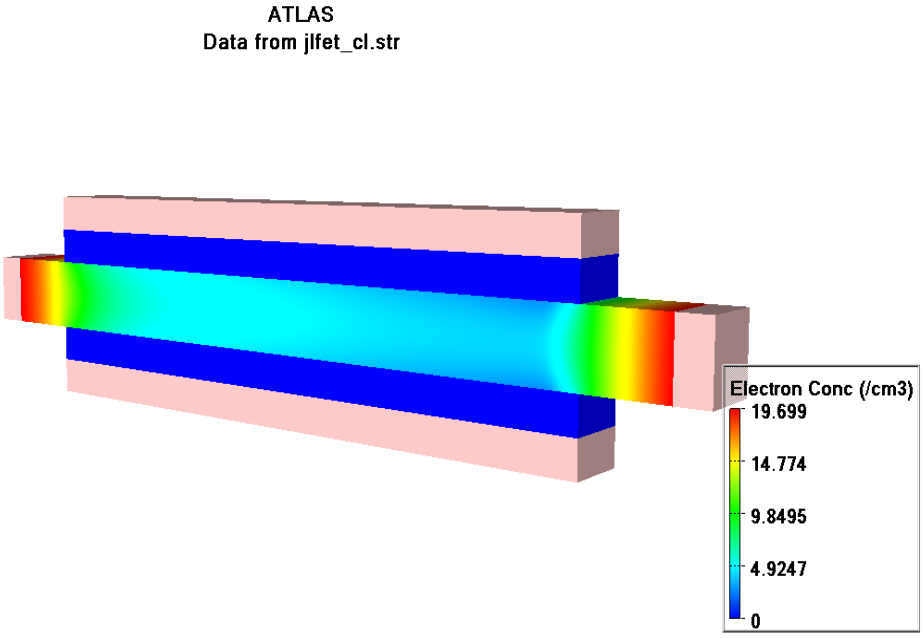

Fig.3.10: Electron Concentration in JLFET under Depletion Mode.

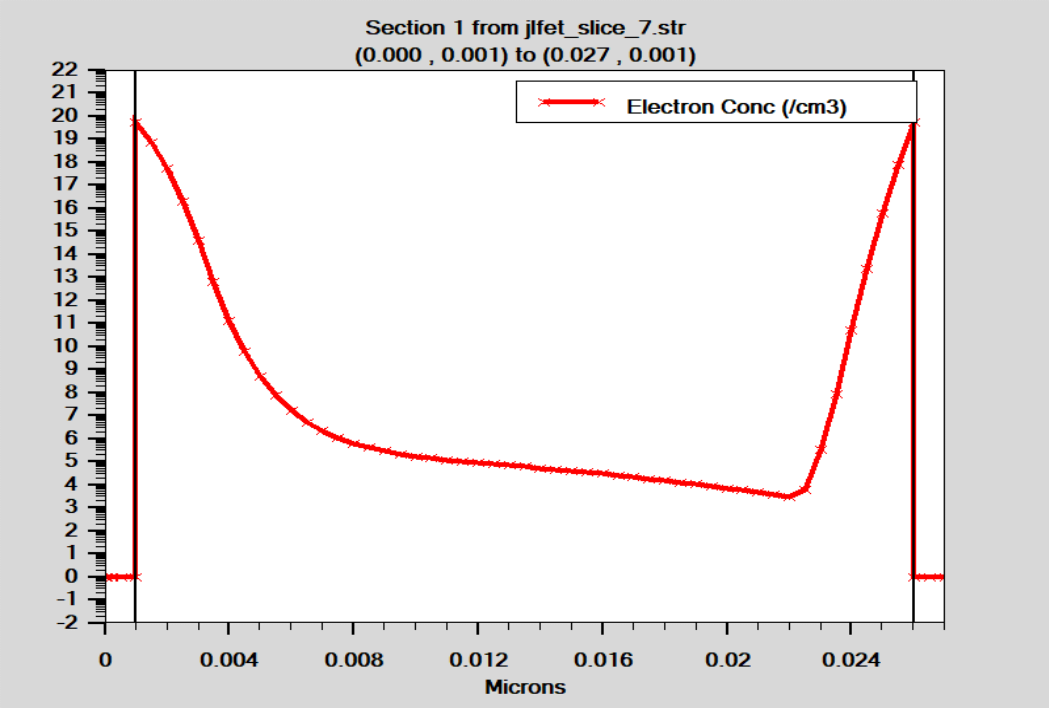

Fig.3.11:Electron Concentration across central line channel region of JLFET under Depletion Mode.

Under depletion mode,central line channel isvanished due to depletion of electrons in the bulk channel region resulting in discontinuity of flow from source to drain, as seen in Fig.3.12. Unlike MOSFETs, channel region tends to form around bulk instead ofoxide-semiconductor interface surfaces. Current Density around oxide-semiconductor interface regions is negligible due to accumulation of holes near the surface regionsas can be seen inFig.3.8. Hotspots in the current density are found to appear in the vicinity of drain and source regions and gradually spread into the bulk region.

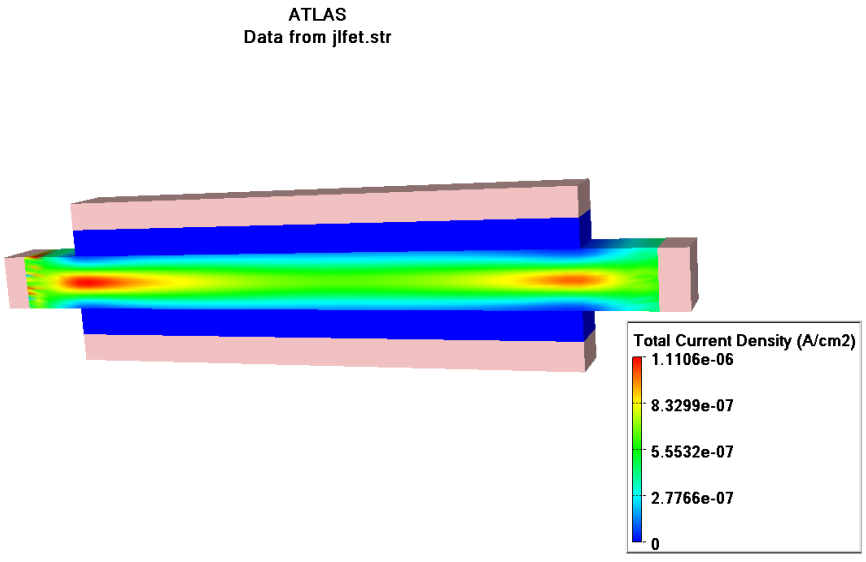

Fig.3.12: Current Density in JLFET under depletion mode.

Weak Depletion Mode :

We provided a positive Gate Bias Voltage ($\boldsymbol{V_{GS} = 0.1V, V_{DS} = 0.5V}$) and observed changes in Physical Parameters of JLFET under Weak Depletion Mode. The conduction band energies in JLFET under this mode are presented in Figs.3.13 (3D view) and 3.14 (cross-sectional view).

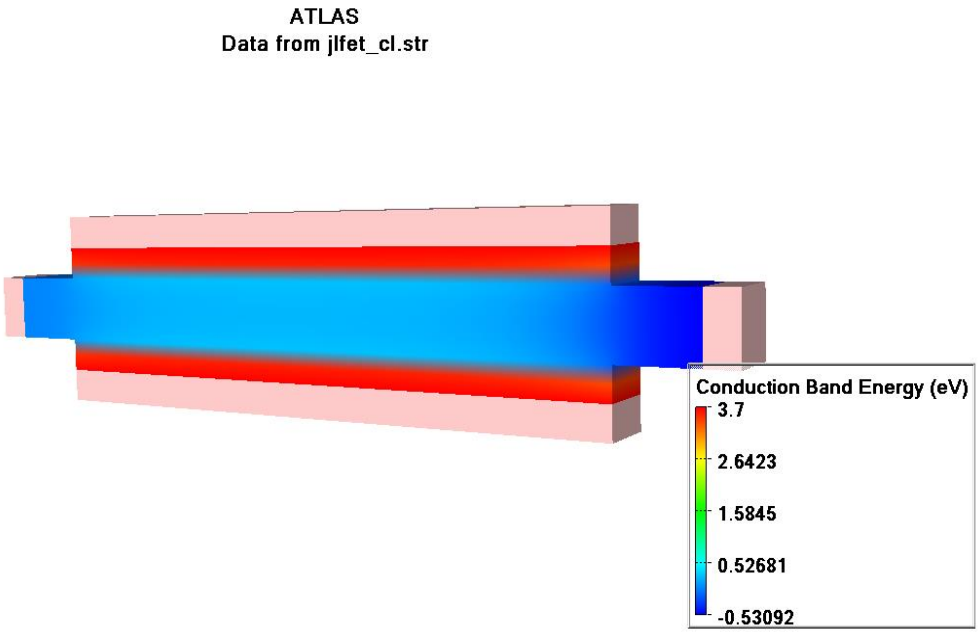

Fig.3.13: Conduction Band Energy in JLFET under Weak Depletion Mode.(3D View).

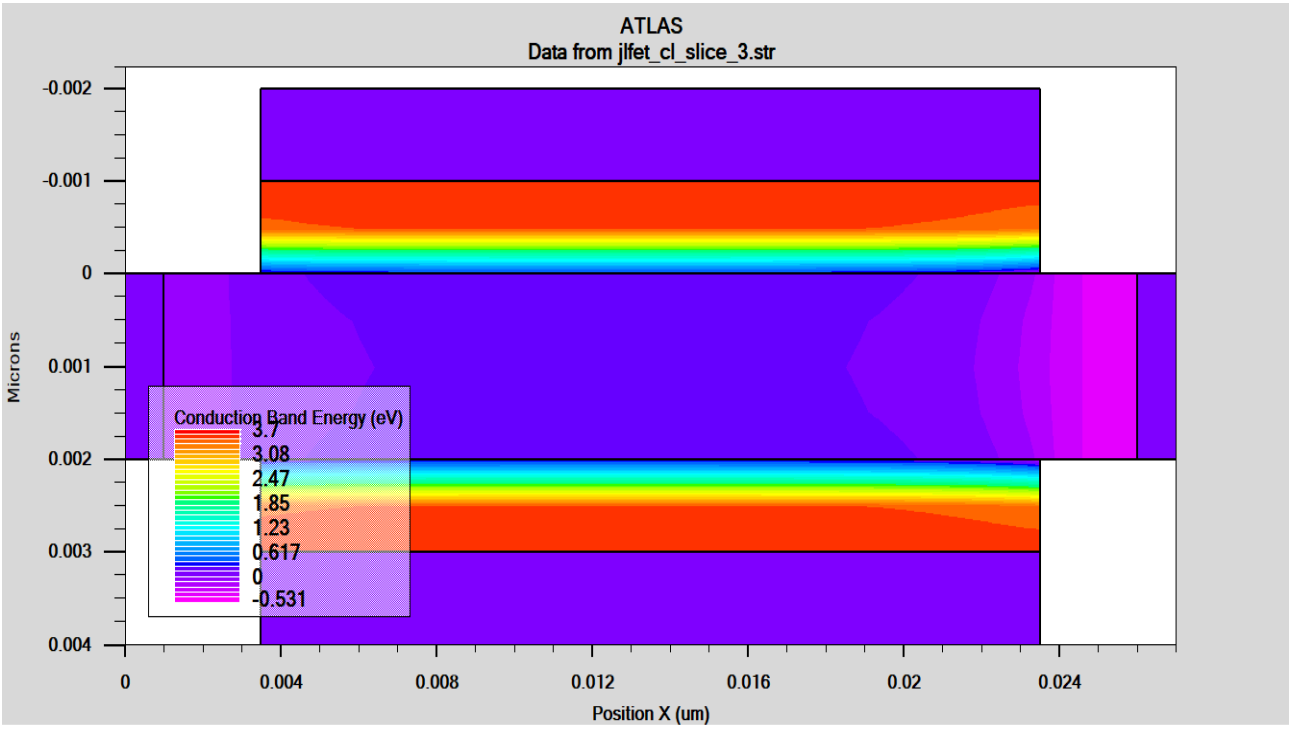

Fig.3.14: Conduction Band Energy in JLFET under Weak Depletion Mode(cross sectional view).

In Fig.3.13 and Fig.3.14,the upward band bending of Conduction Band Energy near surface region throughout the channel length is quite weaker compared to Fig.3.3 and Fig.3.4 in Weak Depletion Mode.We could see onset of Flat Band in the bulk region since Conduction Band Energy gradient is very less throughout the channel region in JLFET as depicted in Fig.3.15.

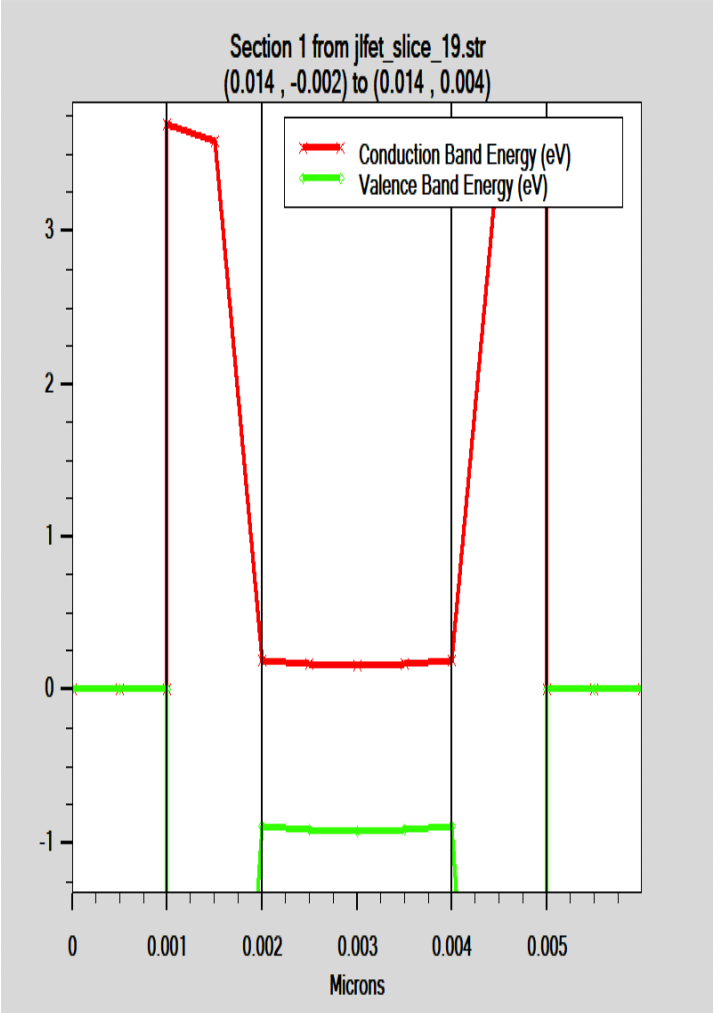

Fig.3.15: Energy Band Diagram of JLFET under Weak Depletion Mode

From Fig.3.16,we could infer conduction band energy barrier against electron flow from source to drain is significantly lowered in Weak Depletion Regionthat may lead to subthreshold current conduction through the central line channel region, provided significant electron concentration has been achieved in the bulk region.

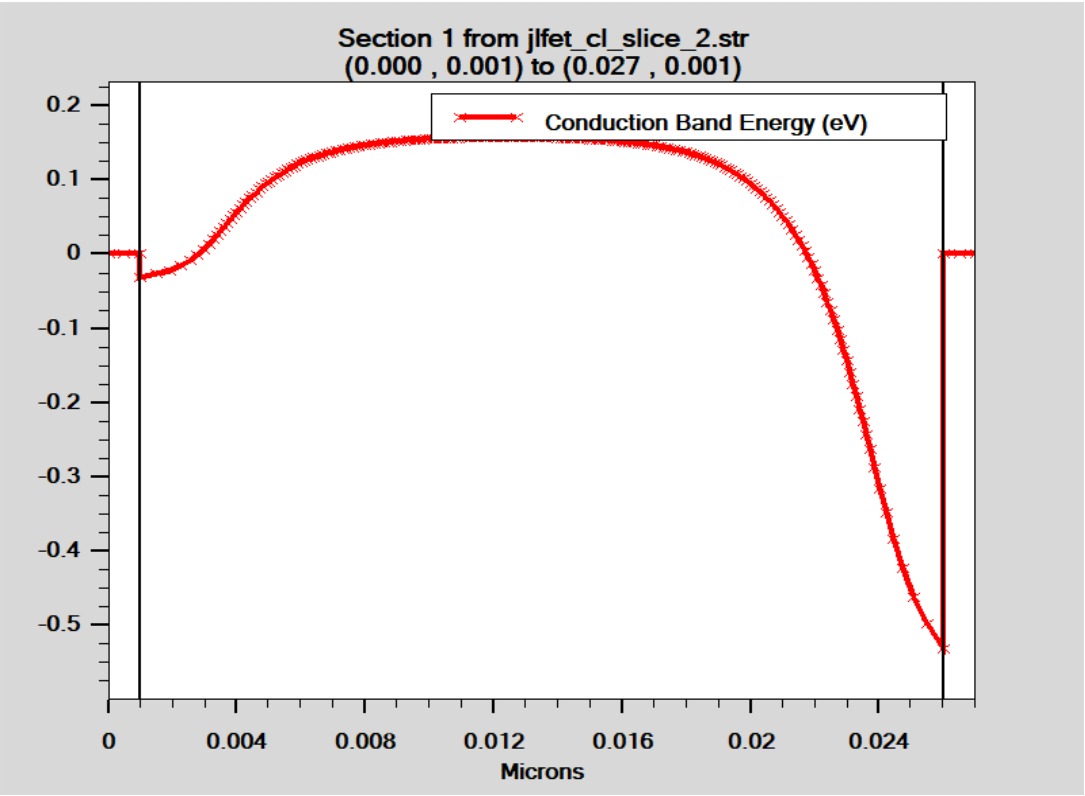

Fig.3.16: Variation of Conduction Band Energyacross the central line channel of JLFET under Weak Depletion Mode

From Fig.3.17 and Fig.3.18,it is apparent that the hole concentration has been significantly lowered throughout the effective gate channel length.The central line channel region experiences minimum hole concentration as in Fig.3.19.

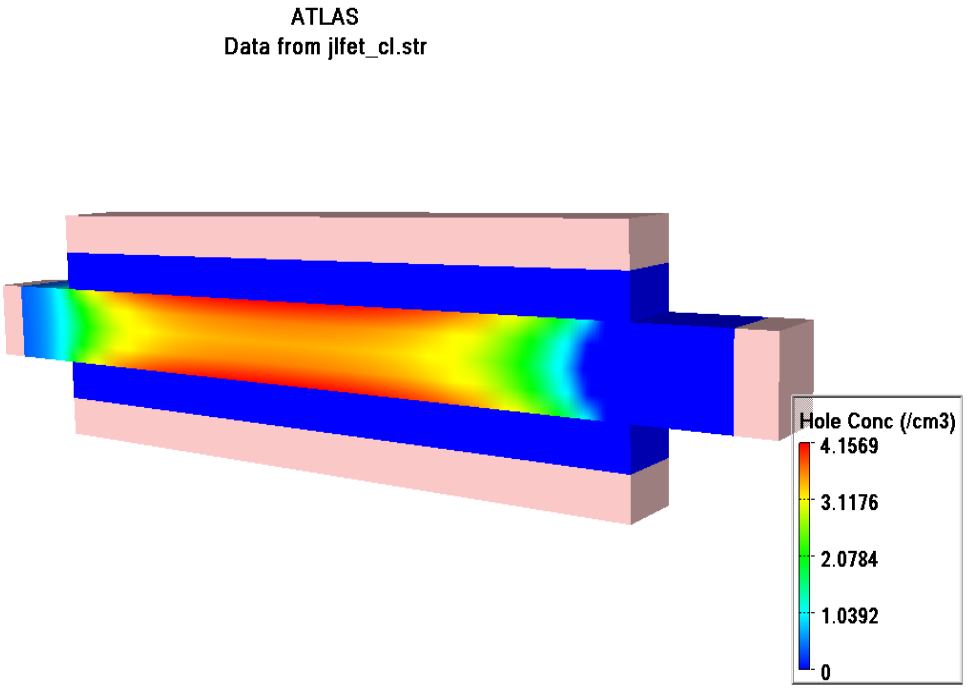

Fig.3.17: Hole Concentration in JLFET under Weak Depletion Mode.

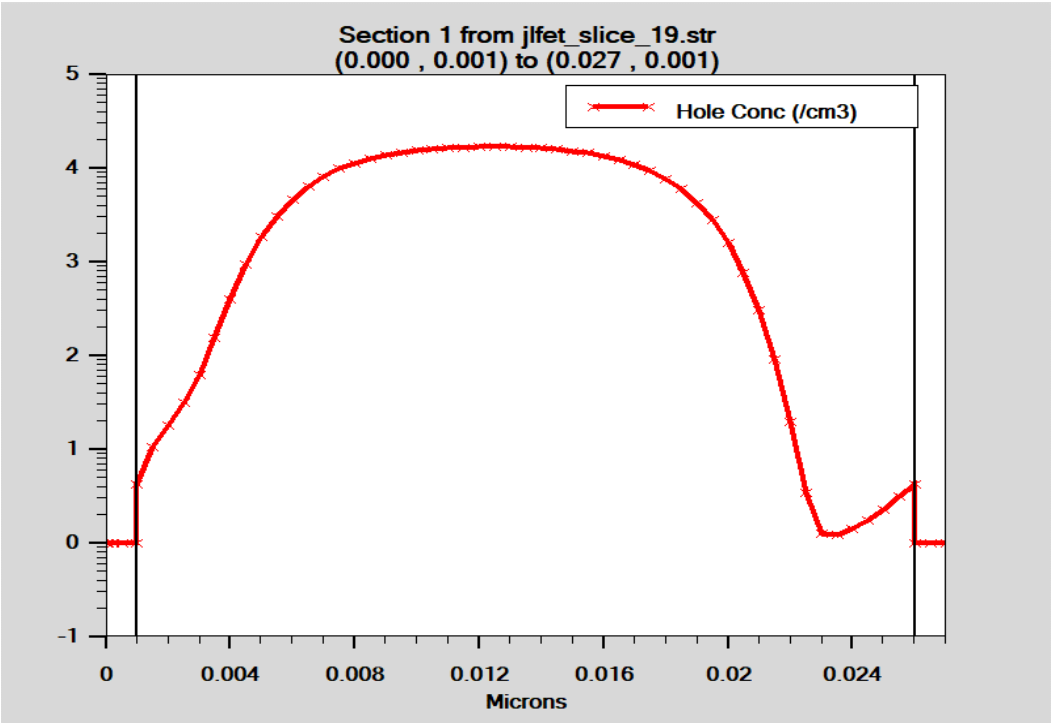

Fig.3.18:Hole Concentration across the central line channel region of JLFETunder Weak Depletion Mode (Horizontal Section)

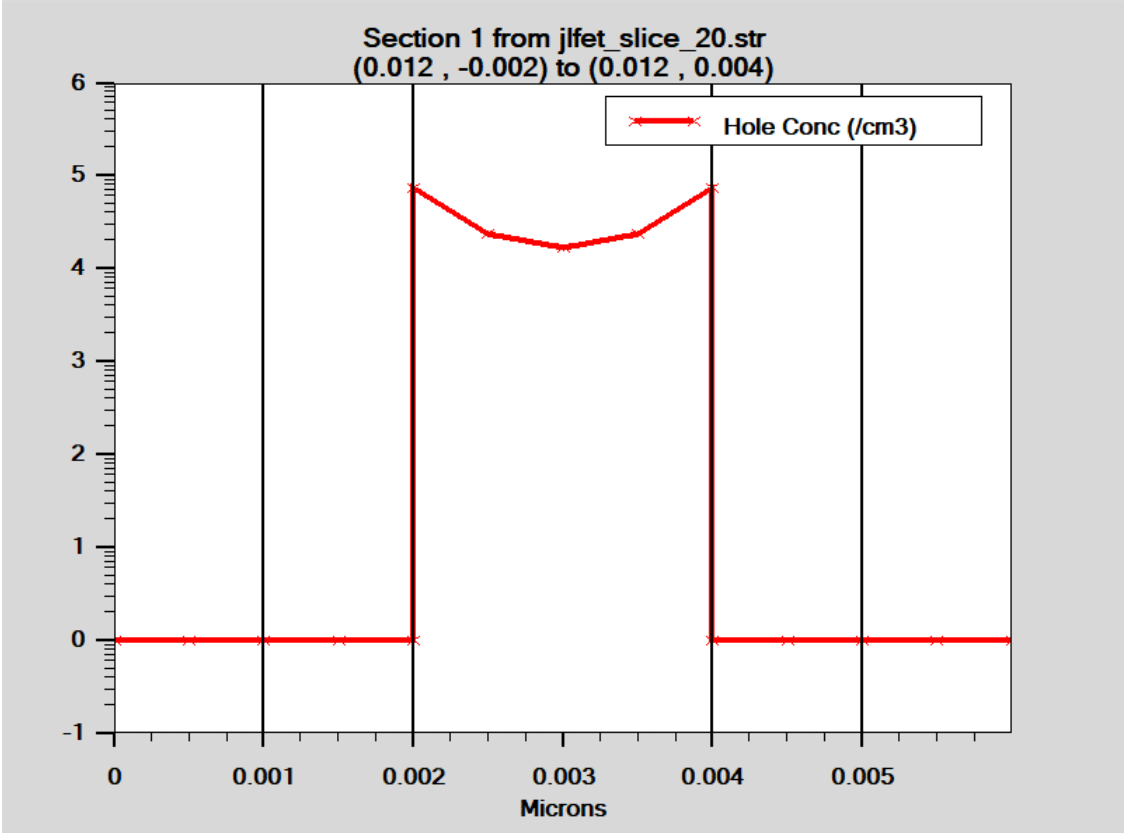

Fig.3.19: Hole Concentration in the central line channel region of JLFET under Weak Depletion Mode (Vertical Section).

On the contrary, electron concentration has been drastically increased throughout the bulk region and maximum electron concentration (due to complete ionization of Dopant atoms in Source and Drain) gradually spreading across the channel region from source to drain as shown inFig.3.20, with a maximum peak around the central line region inFig.3.21.

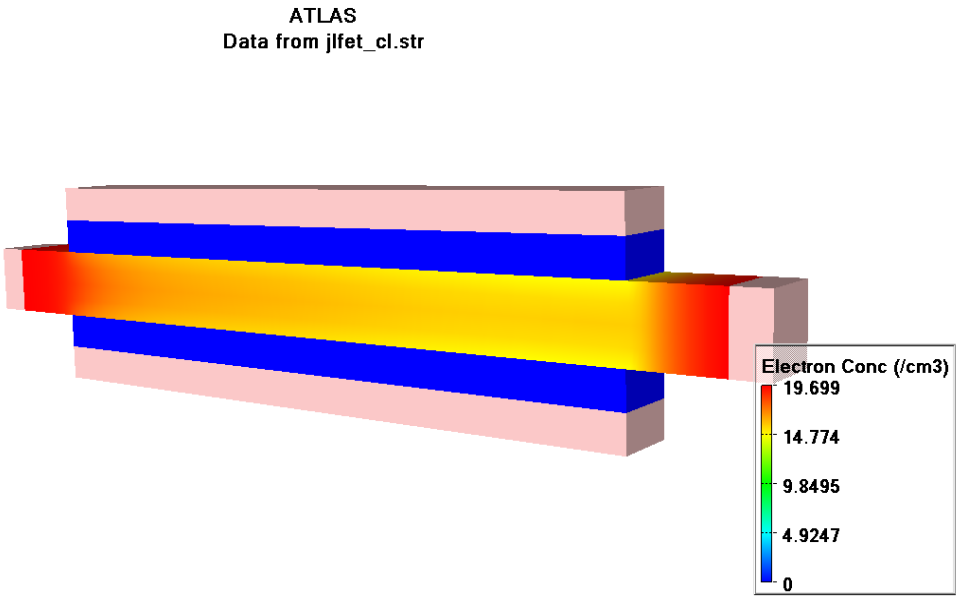

Fig.3.20: Electron Concentration in JLFET under Weak Depletion Mode.

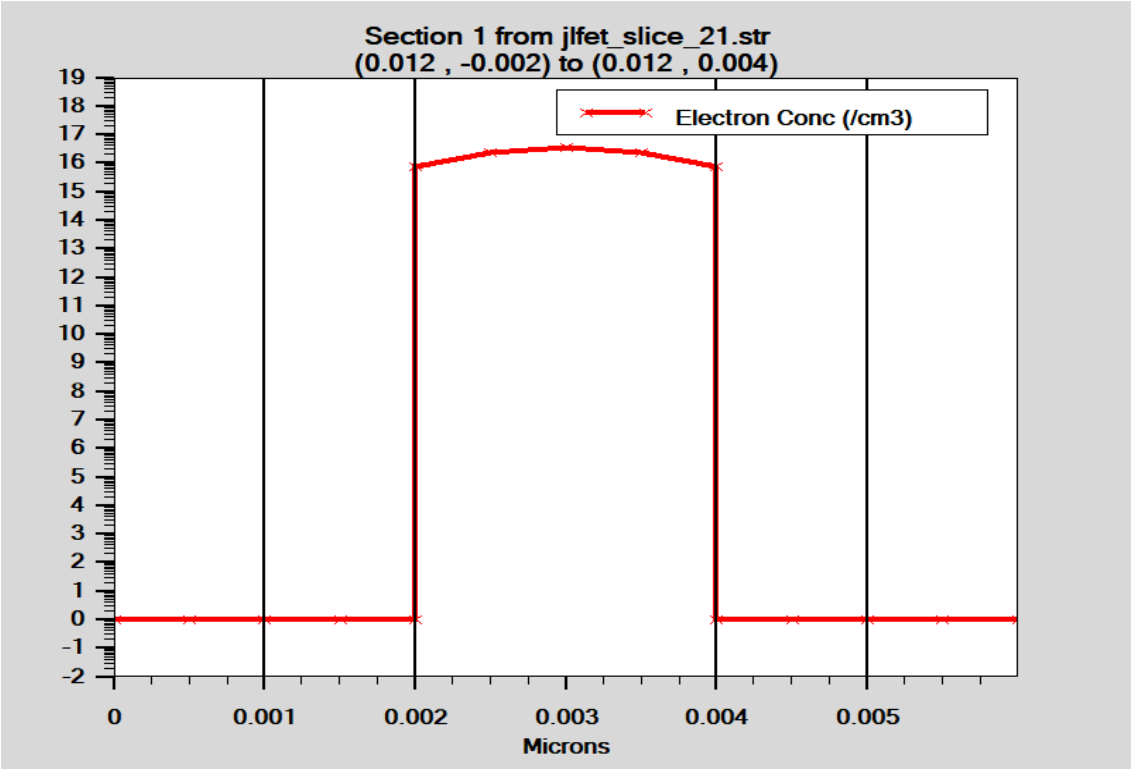

Fig.3.21: Electron Concentration across central line channel region of JLFET under Weak Depletion Mode.

As electron concentration is significant in bulk channel region with greatly lowered conduction band energy barrier across the central line channel region, quite a prominent central line channel region has been formed resulting in bulk current conduction, shown inFig.3.22.

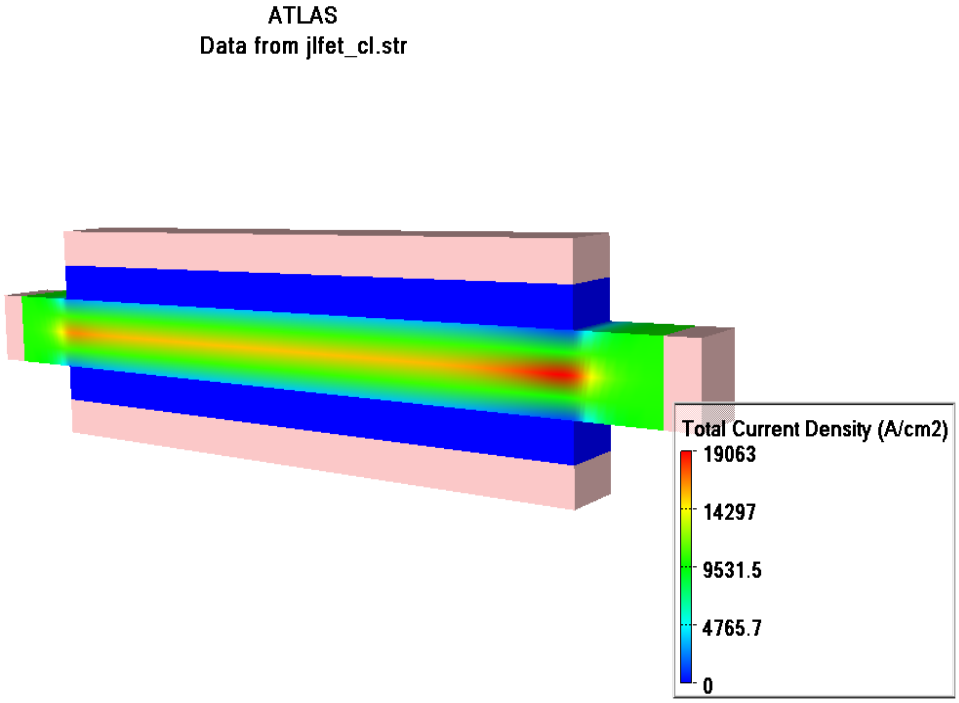

Fig.3.22: Current Density in JLFET under Weak Depletion Mode.

Weak Accumulation Mode:

We provided a positive Gate Bias Voltage ($\boldsymbol{V_{GS} = V_{TH} = 0.38V, V_{DS} = 0.5V}$) and observed changes in Physical Parameters of JLFET under Weak Accumulation Mode.

From Fig.3.23,we could see there is a visble downward band bending of Conduction Band Energy near surface region throughout the channel length that implies onset of accumulation of electrons at the surfaces in Weak Accumulation Mode.We could see Flat Band Condition in the bulk region in Fig.3.24 under this condition.

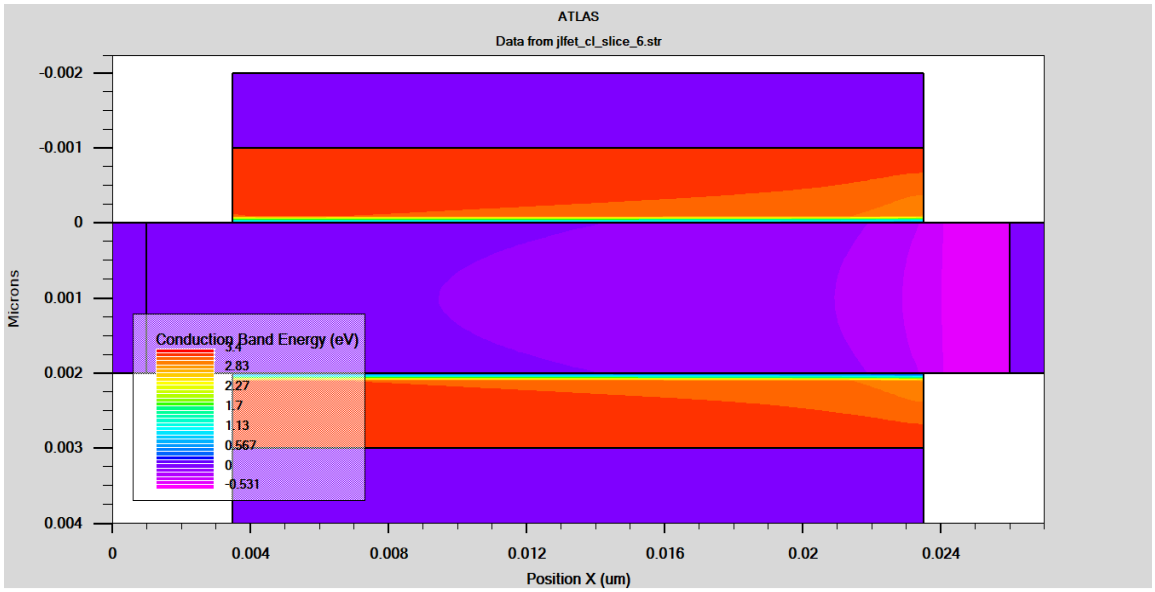

Fig.3.23: Conduction Band Energy in JLFET under Weak Accumulation Mode (Cross Sectional view)

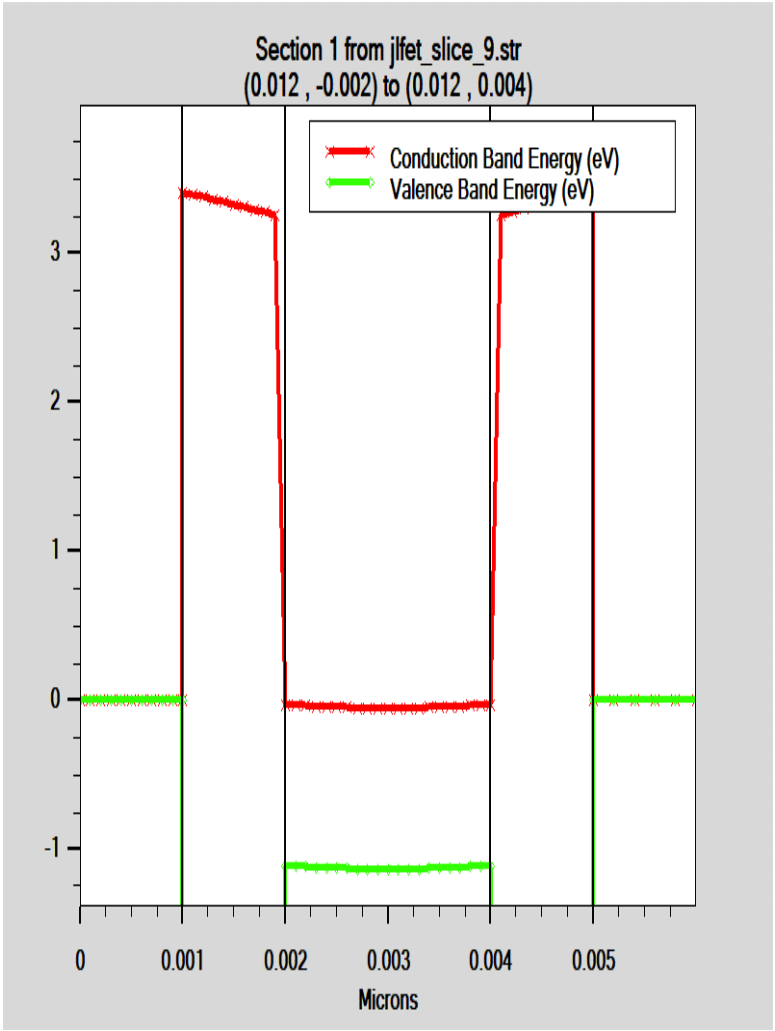

Fig.3.24: Energy Band Diagram of JLFET under Weak Accumulation Mode.

For Gate Voltage equal to Threshold Voltage ,thereis no conduction band energy barrier opposing electron flow from source to drain rather download slope of conduction band energy assists in drift current conduction through the central line channel region. Fig.3.25 supports this fact.

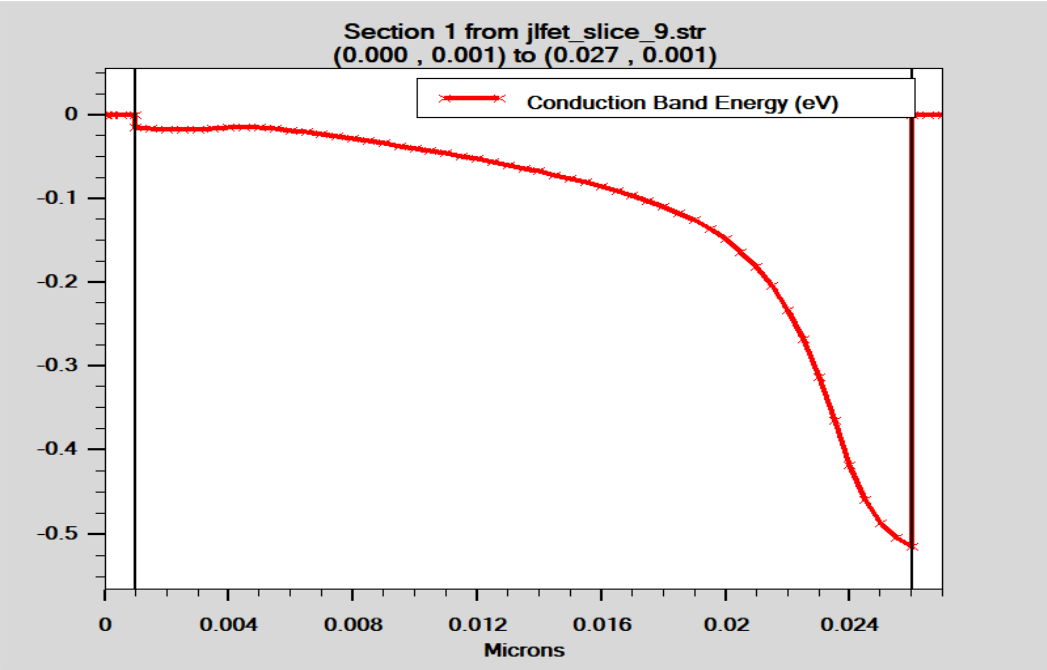

Fig.3.25: Variation of Conduction Band Energyacross the central line channel of JLFET under Weak Accumulation Mode.

With onset of accumulation region, hole concentration starts to diminish throughout the effective gate channel length gradually from drain to source, as shown in Fig.3.26.

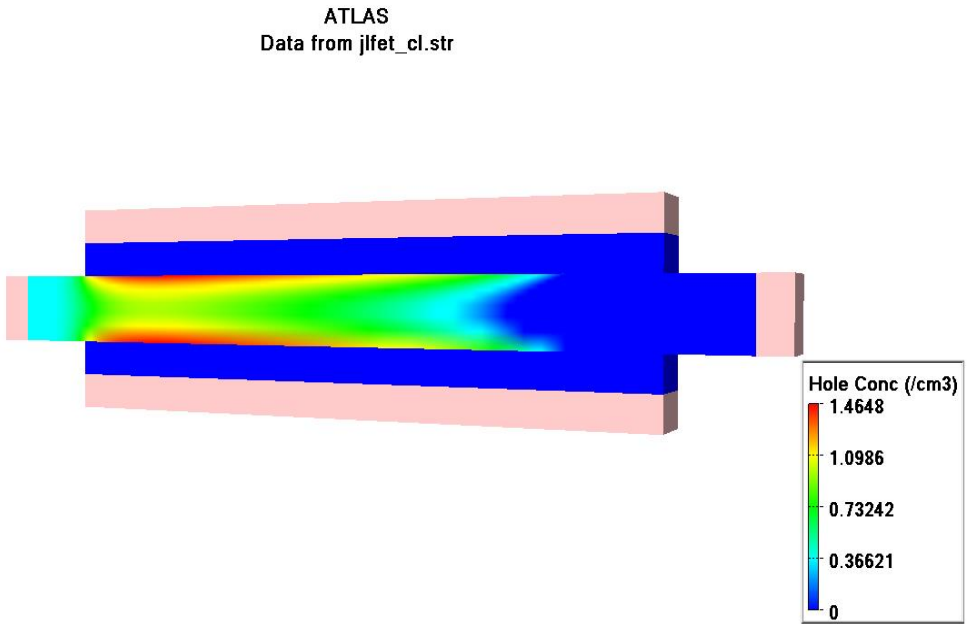

Fig.3.26:Hole Concentration in JLFET under Weak Accumulation Mode.

From Fig.3.27,we could see maximum electron concentration (due to complete ionization of dopant atoms in Source and Drain) throughout the bulk region in JLFET.

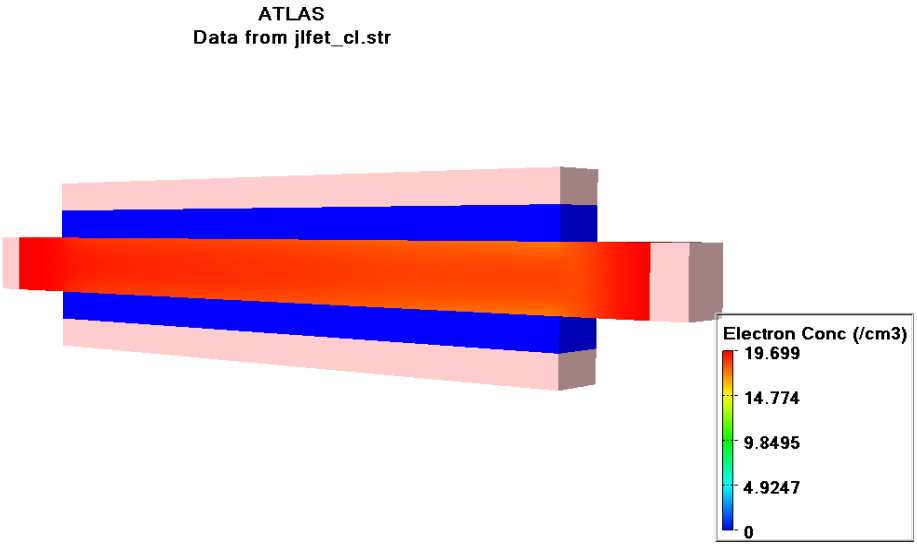

Fig.3.27:Electron Concentration in JLFET under Weak Accumulation Mode.

A Significant bulk channel as well as surface channel have been formed due to accumulation of electrons at the surfaces (seen in Fig.3.28),resulting in significant current flow both through bulk conduction regime as well as accumulation layer regime(inFig.3.29).

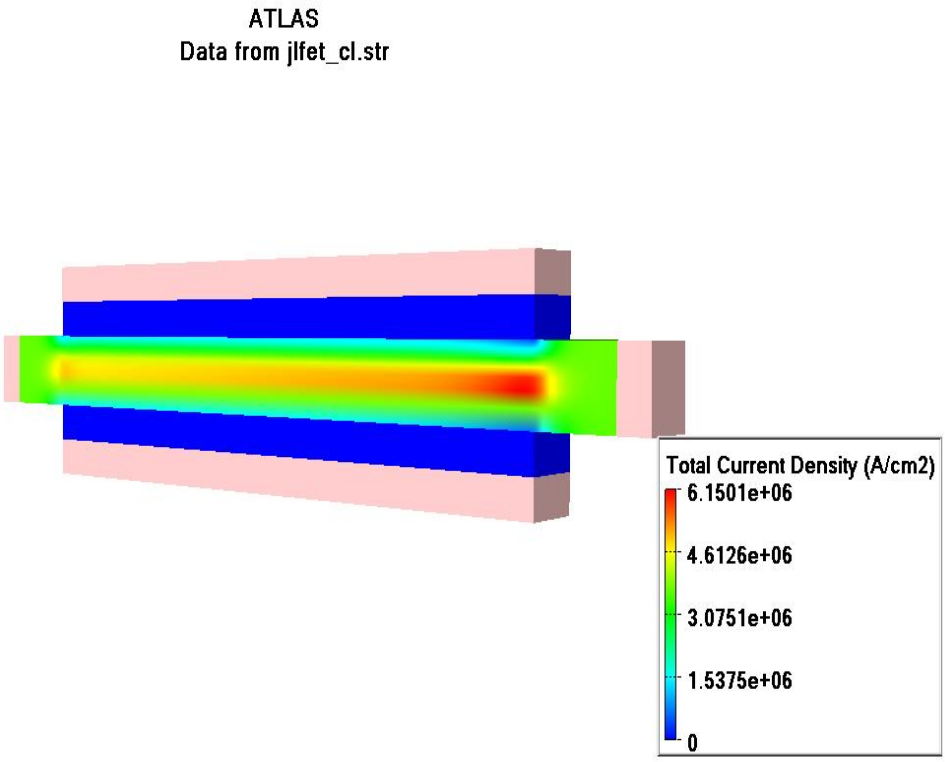

Fig.3.28:Current Density in JLFET under weak accumulation mode (3D View).

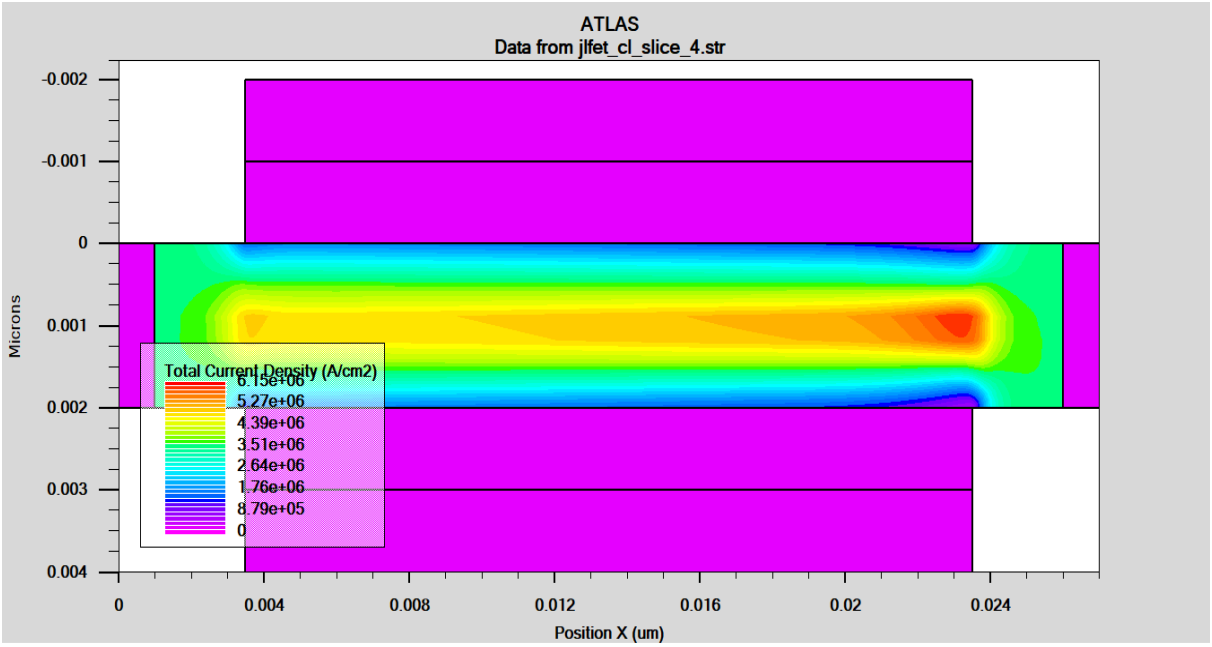

Fig.3.29:Current Density in JLFET under WeakAccumulation Mode (Cross Sectional View).

Accumulation Mode:

We provided a positive Gate Bias Voltage ($\boldsymbol{V_{GS} = 3.5V, V_{DS} = 0.5V}$) and observed changes in Physical Parameters of JLFET under Weak Accumulation Mode.

From Fig.3.30. and Fig.3.31.,we could see there is a downward band bending of Conduction Band Energy near surface in Accumulation Mode (as $V_{GS} > V_{TH}$) .

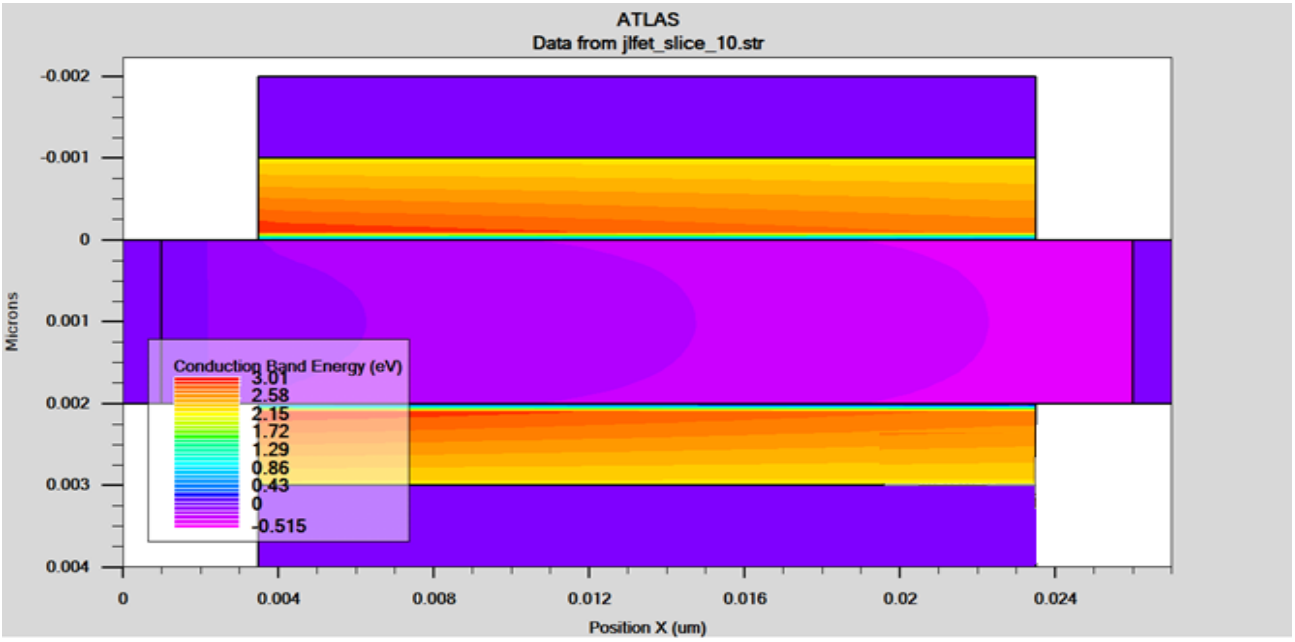

Fig.3.30: Conduction Band Energy in JLFET (Cross-sectional view) under Accumulation Mode.

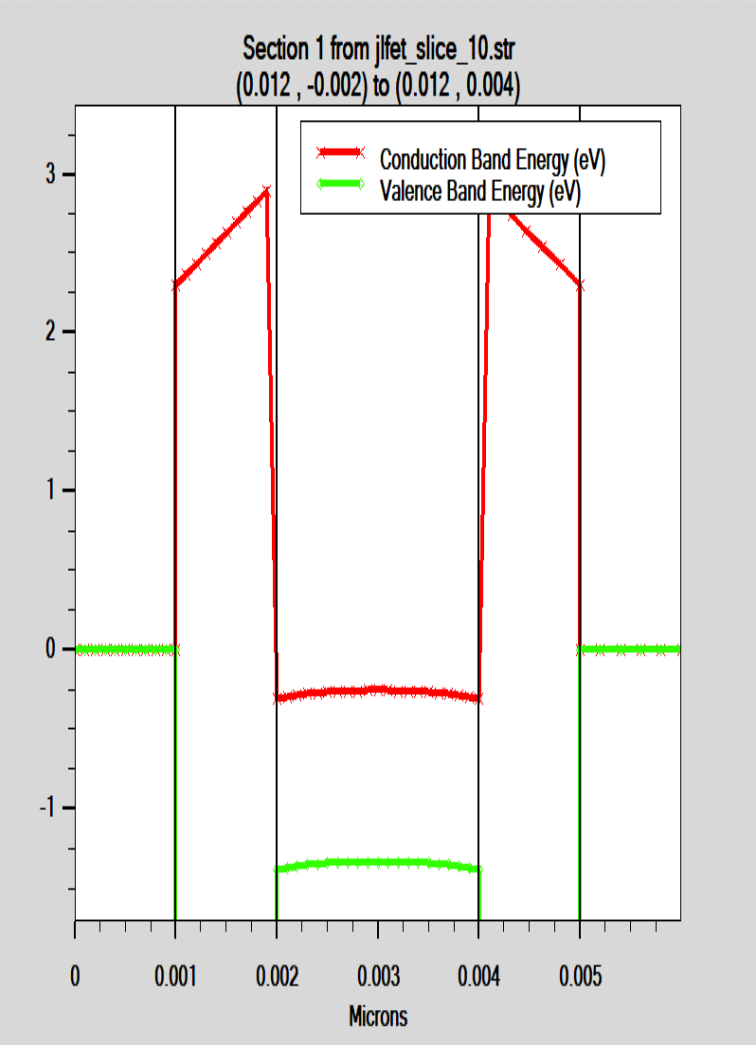

Fig.3.31: Conduction Band Energy of JLFET under Accumulation Mode.

Under Accumulation mode,due to MOS Capacitor action, prominent negative charge has been induced at the surface regions, and its density declines gradually towards the bulk.Also trapped positive mobile charges in the oxide layers disappear, as can be seen from Fig.3.32.

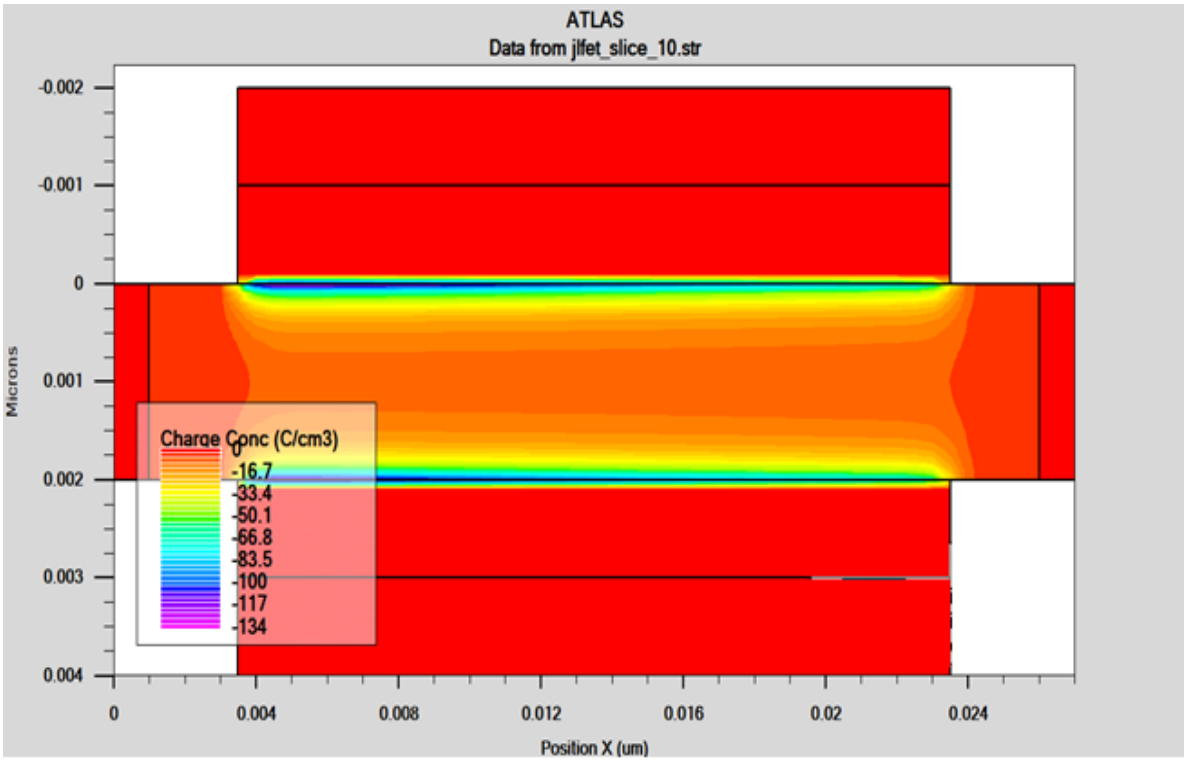

Fig.3.32: Charge Concentration in JLFET under Accumulation Mode.

Current Conduction now occurs though accumulation layer regime with a significant drop in current density through bulk conduction regime, as evident from Fig.3.33.

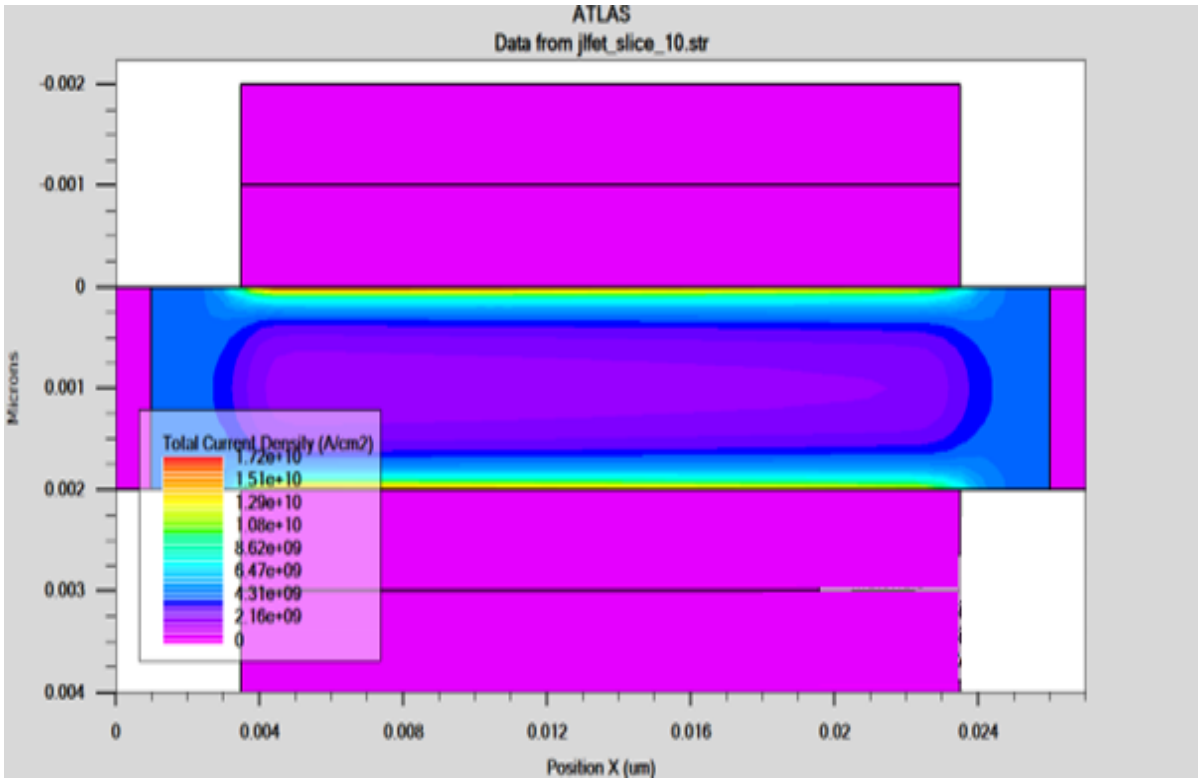

Fig.3.33: Current Density in JLFET under Accumulation Mode.

3.2 Conclusion

From the simulation results , we have investigated the device physics of short channel JLFET under different modes of operation. In depletion mode for negative V_{GS}, conduction band serves as energy barrier opposing electron flow from source to drain and hence no conduction channel is formed between drain and source regions.With increase in V_{GS} , JLFET attains weak accumulation mode, where electron concentration throughout the bulk starts to reach its maximum value (i.e. complete ionization of dopant atoms) and energy barrier of conduction band across the channel region is lowered. Thus a gradual bulk channel is formed between source and drain regions resulting in subthreshold current flow due to bulk conduction. With further increase in V_{GS}exceeding threshold voltage of JLFET, strong accumulation mode is attained. In strong accumulation mode, conduction band energy assists electron flow through its downward slope across the channel region; current conduction takes place due to accumulation layer of electrons at the oxide-semiconductor interface, instead of bulk channel. Hence with transition from depletion mode to accumulation mode, mechanism of current conduction is also changed from bulk conduction to accumulation layer surface conduction. All the simulation results presented here help to clearly follow the device physics under each mode of operation.

Chapter 4

Formulation of Threshold Voltage in a JLFET

In my research project, I have taken Single Material Double Gate Junctionless Field Effect Transistor(DG SMG JLFET) as a specimen to investigate upon threshold voltage of Junctionless FET.

In pursuit of deriving Threshold Voltage for JLFET,bulkpotential ,$\psi_B$is used instead of surface potential $\psi_S$because bulk conduction of charge carriers is responsible for current flow through JLFET.

4.1. Derivation of Classical Threshold Voltage

Let$\psi(x,y)$ be the spatial variation ofpotential in JLFET

By using Poisson's Equation,

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=-\frac{\rho}{\epsilon_{Si}} \tag{4.1}$$

Where, ρ is Charge Density in JLFET,$\epsilon_{Si}$is Permittivity of bulk Silicon

Now in order to resemble spatial variation of potential with simulation results we need to approximate parabolic variation of potential,

$$\psi(x,y)=\alpha_0(y)+\alpha_1(y)x+\alpha_2(y)x^2 \tag{4.2}$$

Where $\alpha_0,\alpha_1,\alpha_2$ are unknown coefficients

Finding $\boldsymbol{\alpha_0,\alpha_1,\alpha_2}$:

We assume continuity of electric flux through both top gate oxide-semiconductor interface as well as bottom gate oxide-semiconductor interface,

$$\psi(0,y)=\psi(t_{Si},y) \tag{4.3}$$

Charge Enclosed by Gaussian Surface across top gate oxide-semiconductor interface,

$$\mathrm{Q_{enclosed}}=C_{ox}((V_G-V_{FB})-\psi(0,y)) \tag{4.4}$$

Using Gauss's Theorem for top gate oxide-semiconductor interface,

$$E_{surface} - E_{center} = \frac{Q_{enclosed}}{\epsilon_{Si}} \tag{4.5}$$

$$=> \ -\frac{\partial\psi(0,y)}{\partial x} = \frac{C_{ox}(V_G - V_{FB} - \psi(0,y)}{\epsilon_{Si}} \tag{4.6}$$

$since\ E_{center} = 0, E = -\frac{\partial\psi}{\partial x}$

On differentiating Equation (4.2) with respect to x,

$$\frac{\partial\psi(x,y)}{\partial x} = \alpha_1(y) + 2\alpha_2(y)x \tag{4.7}$$

At top gate oxide-semiconductor interface, x=0

$$\frac{\partial\psi(0,y)}{\partial x} = \alpha_1(y) \tag{4.8}$$

Substituting value of $\frac{\partial\psi(0,y)}{\partial x}$ $from\ equ^n(4.8)\ into\ equ^n(4.6), we\ get$

$$\alpha_1(y) = -\frac{C_{ox}\big(V_G - V_{FB} - \alpha_0(y)\big)}{\epsilon_{Si}} \tag{4.9}$$

Due to Symmetric structure of DG JLFET,we can assume Electric Field at the center(E_{center}) to be zero,

$$E_{center} = -\frac{\partial\psi\left(\frac{t_{Si}}{2}, y\right)}{\partial x} = 0 \tag{4.10}$$

Putting x = $\frac{t_{Si}}{2}$ $in\ Equation\ (4.7), we\ get$

$$\alpha_1(y) = -\alpha_2(y)t_{Si} \tag{4.11}$$

$$\alpha_2(y) = \frac{C_{ox}\big(V_G - V_{FB} - \alpha_0(y)\big)}{\epsilon_{Si}t_{Si}} \tag{4.12}$$

$$\alpha_0(y) = \ \psi(0,y) = \psi_S \tag{4.13}$$

Relation between bulk potential ,ψ_B *and* surface potential ψ_S:

$From\ equ^n(4.2), (4.9), (4.12), (4.13)\ we\ get$

$$\psi(x,y) = \psi_S + \frac{C_{ox}(V_G - V_{FB} - \psi_S)(x^2 - xt_{Si})}{\epsilon_{Si}t_{Si}} \tag{4.14}$$

$$\psi_B = \psi\left(\frac{t_{Si}}{2}, y\right) \tag{4.15}$$

$Putting\ x = \frac{t_{Si}}{2}\ in\ equ^n(4.14), we\ get$

$$\psi_B = \psi\left(\frac{t_{Si}}{2}, y\right) = \psi_S\left(1 + \frac{C_{ox}t_{Si}}{4\epsilon_{Si}}\right) - \frac{C_{ox}t_{Si}(V_G - V_{FB})}{4\epsilon_{Si}} \tag{4.16}$$

After finding values of unknown coefficients in Equation (4.2) from Eq. (4.11), Eq. (4.12) and Eq. (4.13),

$$\frac{\partial^2\psi(x,y)}{\partial x^2} = \frac{2C_{ox}}{\epsilon_{Si}t_{Si}}(V_G - V_{FB} - \psi_S) \tag{4.17}$$

$$\frac{\partial^2\psi(x,y)}{\partial x^2} = 8C_{ox}\left(\frac{V_G - V_{FB} - \psi_B}{4\epsilon_{Si}t_{Si} + C_{ox}t_{Si}^2}\right) \tag{4.18}$$

Similarly,

$$\frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{\partial^2\psi_S}{\partial y^2}\left(1 + \frac{C_{ox}}{\epsilon_{Si}}x - \frac{C_{ox}}{\epsilon_{Si}t_{Si}}x^2\right) \tag{4.19}$$

Now From equation (4.16),

$$\frac{\partial^2\psi_S}{\partial y^2} = \frac{\partial^2\psi_B}{\partial y^2}\left(\frac{1}{1 + \frac{C_{ox}t_{Si}}{4\epsilon_{Si}}}\right) \tag{4.20}$$

Putting values of Equation (4.18),(4.20) in Equation (4.1), we get

$$\frac{\partial^2\psi_B}{\partial y^2} - \frac{8C_{ox}}{4\epsilon_{Si}t_{Si} + C_{ox}t_{Si}^2}\left[\psi_B - (V_G - V_{FB}) - \frac{\rho t_{Si}}{2C_{ox}} - \frac{\rho t_{Si}^2}{8\epsilon_{Si}}\right] = 0 \tag{4.21}$$

Let ξ_0 be bulk potential for long channel JLFET,

$$\xi_0 = V_G - \gamma \tag{4.22}$$

$$where\ \gamma = V_{FB} - \frac{\rho t_{Si}}{2C_{ox}} - \frac{\rho t_{Si}^2}{8\epsilon_{Si}}$$

Now, $\left[\frac{8C_{ox}}{4\epsilon_{Si}t_{Si} + C_{ox}t_{Si}^2}\right] \equiv L^{-2}$, $inverse\ square\ length\ dimension$

So ,we introduce L_0 to be natural length of DG JLFET such that,

$$\frac{1}{L_0^2} = \frac{8C_{ox}}{4\epsilon_{Si}t_{Si} + C_{ox}t_{Si}^2} \tag{4.23}$$

Putting values of Equation (4.22),(4.23) into (4.21), we get

$$\frac{\partial^2\psi_B}{\partial y^2} - \frac{1}{L_0^2}(\psi_B - \xi_0) = 0 \tag{4.24}$$

Since $\psi_B = \psi\left(\frac{t_{Si}}{2}, y\right)$ is a function of y only ,so

$$\frac{d^2\psi_B}{dy^2} - \frac{1}{L_0^2}(\psi_B - \xi_0) = 0 \tag{4.25}$$

Solving O.D.E (4.25),we get

$$\psi_B(y) = \xi_0 + a_1 e^{\frac{y}{L_0}} + a_2 e^{-\frac{y}{L_0}} \tag{4.26}$$

Finding a_1,a_2:

Using Boundary Conditions ,

$$\psi_B(0) = V_S + V_{bi} \ , V_S \ is \ Source \ Potential \ and \ V_{bi} \ is \ built - in \ Voltage$$

$$=> \xi_0 + a_1 + a_2 = V_S + V_{bi} \tag{4.27}$$

$$\psi_B(L_G) = V_D + V_{bi} \ , V_D \ is \ Drain \ Potential \ and \ L_G \ is \ channel \ length$$

$$=> \xi_0 + a_1 e^{\frac{L_G}{L_0}} + a_2 e^{-\frac{L_G}{L_0}} = V_D + V_{bi} \tag{4.28}$$

On subtracting equation (4.27) from (4.28),

$$a_1 \left(e^{\frac{L_G}{L_0}} - 1\right) + a_2 \left(e^{-\frac{L_G}{L_0}} - 1\right) = V_{DS}$$

$$=> a_1 = \frac{V_{DS}}{\left(e^{\frac{L_G}{L_0}} - 1\right)} - a_2 \frac{\left(e^{-\frac{L_G}{L_0}} - 1\right)}{\left(e^{\frac{L_G}{L_0}} - 1\right)} \tag{4.29}$$

Substituting value of a_1 from Equation (4.29) into (4.27),we get

$$a_2 = \frac{1 - e^{\frac{L_g}{L_0}}}{2sinh\left(L_g / L_0\right)} \xi_0 - \frac{V_D}{2sinh\left(L_g / L_0\right)} + \frac{e^{\frac{L_g}{L_0}} - 1}{2sinh\left(L_g / L_0\right)} V_{bi} \tag{4.30}$$

Substituting value of $a_2$from Equation (4.30) into (4.27), we get

$$a_1 = \frac{e^{-\frac{L_g}{L_0}} - 1}{2sinh\left(L_g / L_0\right)} \xi_0 + \frac{V_D}{2sinh\left(L_g / L_0\right)} - \frac{\left(e^{-\frac{L_g}{L_0}} - 1\right)}{2sinh\left(L_g / L_0\right)} V_{bi} \tag{4.31}$$

Finding ξ_0:

In order to find out ξ_0 we need to investigate on extrema of bulk potential $\psi_B(y)$

On differentiating Equation (4.26) with respect to y,

$$\frac{d\psi_B(y)}{dy} = \frac{a_1}{L_0} e^{y/L_0} - \frac{a_2}{L_0} e^{-\frac{y}{L_0}} \tag{4.32}$$

On differentiating Equation (4.32) with respect to y,

$$\frac{d^2\psi_B(y)}{dy^2} = \frac{a_1}{L_0^2}e^{y/L_0} + \frac{a_2}{L_0^2}e^{-y/L_0} \tag{4.33}$$

From Equation (4.32),we obtain critical point as :

$$\frac{d\psi_B(y)}{dy} = 0$$

$$=> \frac{a_1}{L_0}e^{y/L_0} - \frac{a_2}{L_0}e^{-y/L_0} = 0$$

$$=> y = \frac{L_0}{2}\ln(\frac{a_2}{a_1}) \tag{4.34}$$

Putting value of critical point from Equation (4.34) into (4.33),we get

$$\frac{d^2\psi_B(y)}{dy^2} = \frac{a_1}{L_0^2}\left(\frac{a_2}{a_1}\right)^{1/2} + \frac{a_2}{L_0^2}\left(\frac{a_2}{a_1}\right)^{-1/2}$$

$$=> \frac{d^2\psi_B(y)}{dy^2} = \frac{2(a_1a_2)^{\frac{1}{2}}}{L_0^2} > 0$$

$$Hence, \psi_B(y)\ has\ a\ minima\ at\ y_{min} = \frac{L_0}{2}\ln(\frac{a_2}{a_1}) \tag{4.35}$$

Putting value of y_{min} from Equation (4.35) into (4.26),

$$\psi_B(y_{min}) = \xi_0 + 2(a_1a_2)^{\frac{1}{2}} \tag{4.36}$$

For different values of Gate Voltage V_G we obtained minima of $\psi_B(y)$(as shown infig4.1)

And $\psi_B(y_{min}) = 0$ when$V_G = V_{TH}$, where V_{TH} is Threshold Voltage of JLFET.

Based on that inference , we equate $\psi_B(y_{min})$ to zero as :

$$\psi_B(y_{min}) = 0$$

$$=> \xi_0 + 2(a_1a_2)^{\frac{1}{2}} = 0$$

$$=> \xi_0^2 = 4(a_1a_2)$$

$$=> \xi_0^2 = 4(-\beta_2\xi_0 + \beta_1V_D + \beta_2V_{bi})(\beta_3\xi_0 - \beta_1V_D - \beta_3V_{bi}) \tag{4.37}$$

$$where\ \beta_1 = \frac{V_D}{2sinh\left(L_g/L_0\right)}, \beta_2 = \frac{1 - e^{-\frac{L_g}{L_0}}}{2sinh\left(L_g/L_0\right)}, \beta_3 = \frac{1 - e^{\frac{L_g}{L_0}}}{2sinh\left(L_g/L_0\right)}$$

On solving quadratic equation for ξ_0 in Equation (4.37), we get

$$\xi_0 = \frac{(8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4V_{bi}(\beta_1\beta_3 + \beta_2\beta_1 + V_{bi}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2}$$

(4.38)

Now , obtained value of ξ_0 from Equation (4.38) is applicable when $V_G = V_{TH}$

From Equation (4.22),

$$\xi_0 = V_{TH} - \gamma$$

$$=> V_{TH} = \xi_0 + \gamma \tag{4.39}$$

Putting values of ξ_0 and γ from Equation (4.38) and (4.22) into (4.39) ,we get

$$V_{TH} = \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{\rho t_{Si}}{2C_{ox}} - \frac{\rho t_{Si}^2}{8\epsilon_{Si}} \tag{4.40}$$

Thus , the Threshold Voltage (V_{TH}) of DG SMG JLFET is derived.

In our DG JLFET specimen, we assume the dopant density as $N_D$we added donor impurities with dopant density say N_D,

Threshold Voltage of JLFET is calculated under Bulk Conduction regime where onset of current conduction is controlled by depletion charge density.So total charge density in JLFET under depletion region is equal to depletion charge density,such that

$$\rho = qN_D \tag{4.41}$$

Putting value of ρ from Equation (4.41) into (4.40) , we get

$$V_{TH} = \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{qN_D t_{Si}}{2C_{ox}} - \frac{qN_D t_{Si}^2}{8\epsilon_{Si}} \tag{4.42}$$

Equation (4.40) gives the final expression for the Threshold Voltage (V_{TH}) of DG SMG JLFET considered here.

4.2Results and Discussion

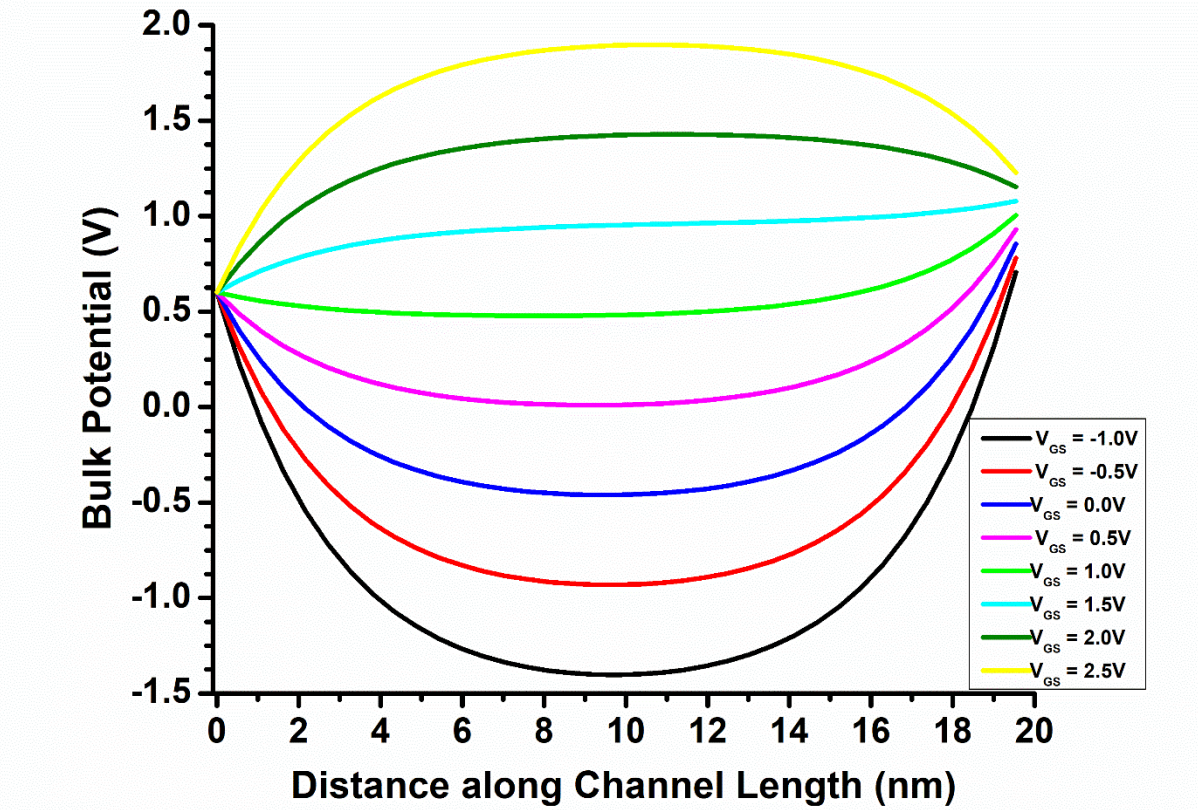

Fig. 4.1: Variation of $\psi_B(y)$ in Si bulk along channel length for different V_G

Based on the results derived above, plots of Bulk potential and mainly those of Threshold voltage for DG SMG JLFET are obtained using MATLAB and presented here. Fig.4.1 reveals that theCentral line bulk potential has a upward concavity with its variation along channel length of JLFET in depletion mode and gradually shifts to downward concavity in accumulation mode.(as indicated in Fig 4.1).Minima of the family curves gradually make a transition from negative critical point to positive with transition in mode of operation in JLFET from depletion to accumulation. Amidst the transition, there is a certain gate voltage for which minima of thecentral line potential becomes zero which is essentially the threshold voltage because the conduction band curve corresponding to threshold voltage would not have any positive barrier along the channel length opposing the current flow.

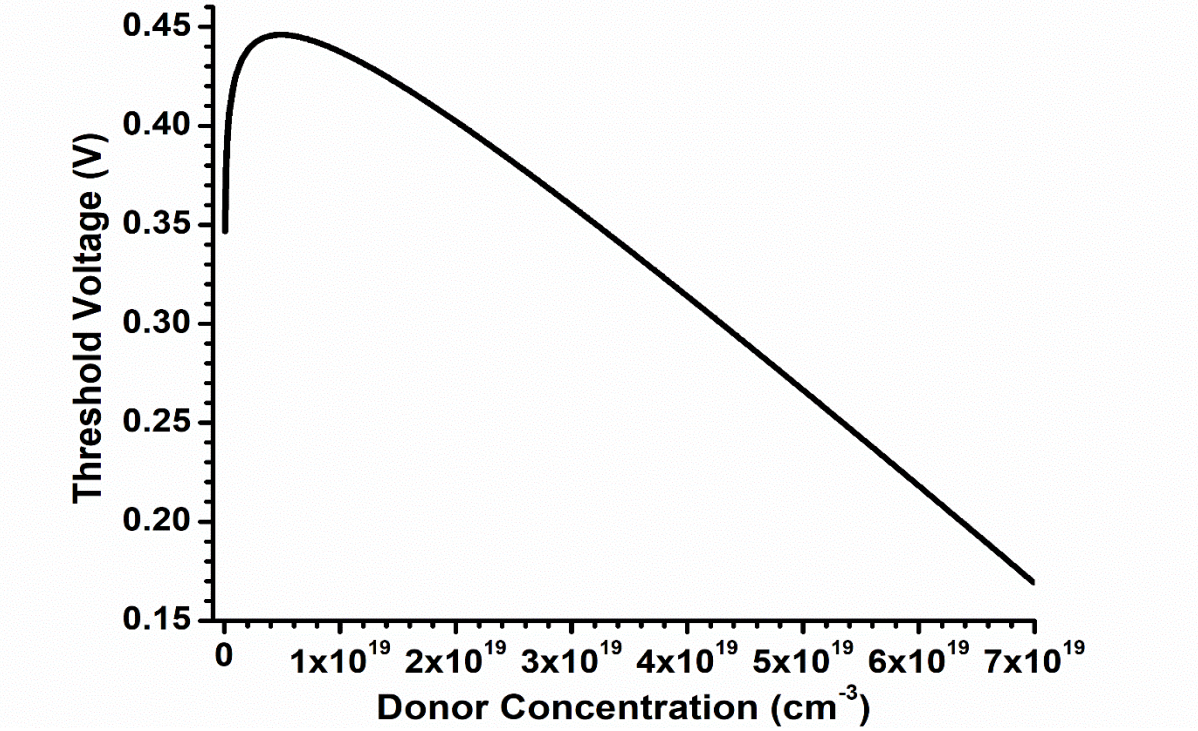

Fig. 4.2: V_{TH} variation with $N_D$for t_{ox} = 1nm , L_G= 20nm , t_{Si}= 2nm

Threshold Voltage of JLFET reaches to a maximum peak value rapidly (V_{TH} =0.446 V for N_D= 4.8x10^{18} cm^{-3}) with increase in Donor Concentration from the order to 10^{17} to 10^{18} cm^{-3} and declines gradually with further increase in Donor Concentration till the order of 10^{19} cm^{-3}as illustrated in Fig. 4.2.

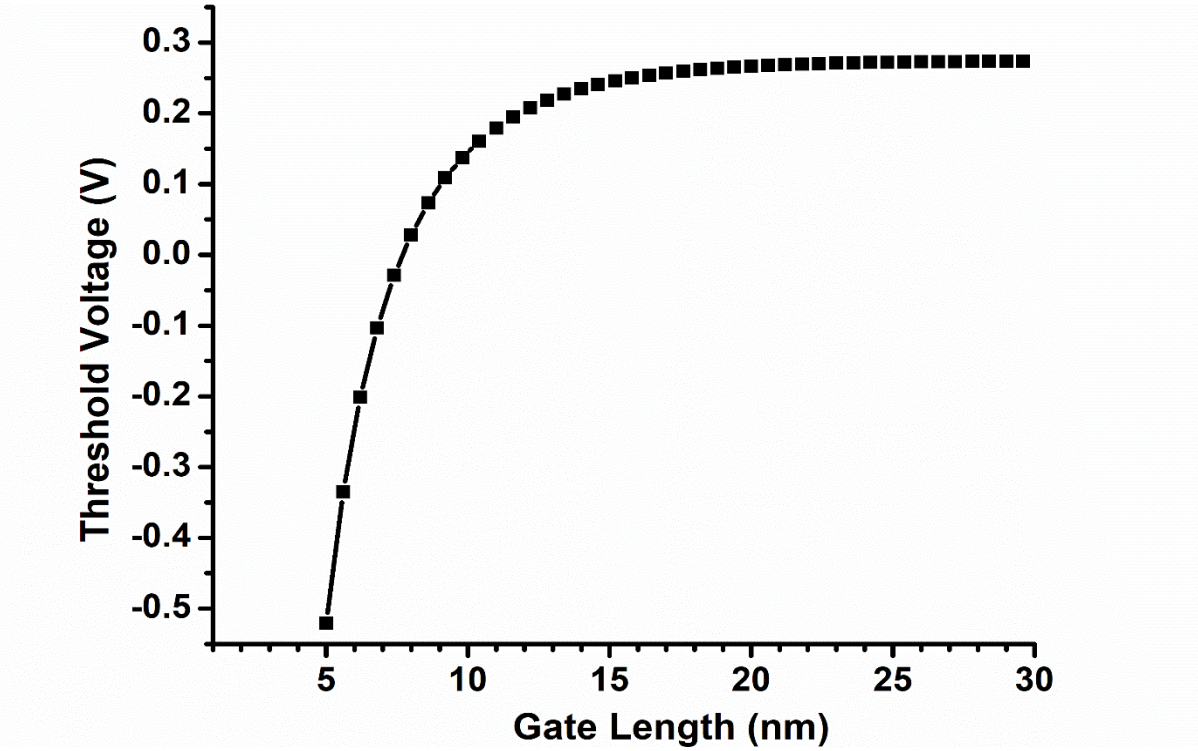

Fig 4.3: Variation of V_{TH} with $L_G$for t_{ox} = 1nm , N_D = 5x10^{19} cm^{-3} , t_{Si}= 2nm

For very short gate channels in JLFET below 10nm, threshold voltages drop down to negative values which require stronger gate control for current conduction. With increase in gate channel length ,threshold voltage gradually saturates to long channel threshold voltage as shown in Fig. 4.3.

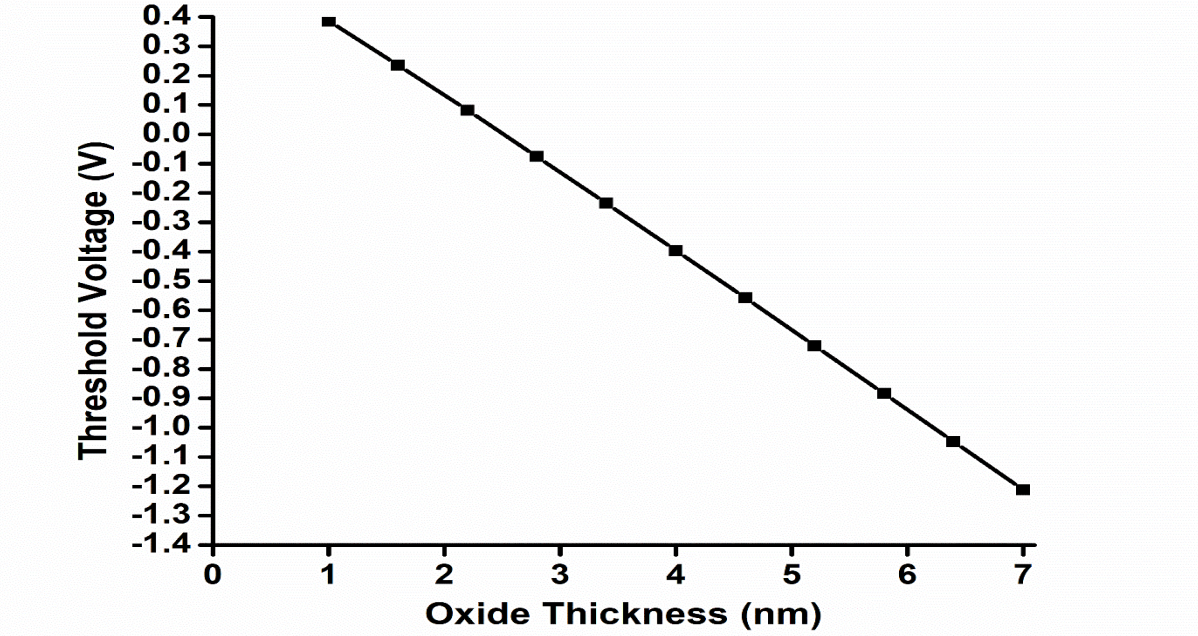

Fig. 4.4: V_{TH} variation with t_{ox} for N_D= 5x10^{19} cm^{-3} , L_G= 20nm , t_{Si}= 2nm

With increase in oxide thickness, gate capacitance gets weaker so gate control over conduction current gradually diminishes and eventually threshold voltage declines to negative values with a constant proportionality with oxide thickness as depicted in Fig 4.4 .

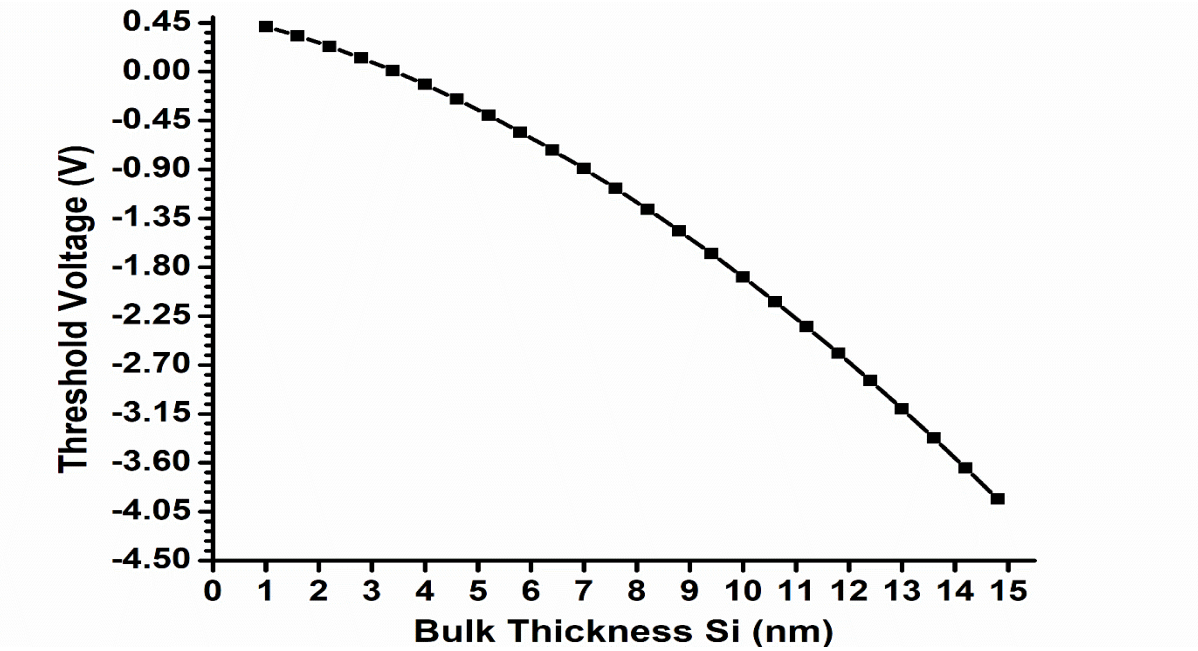

Fig. 4.5: V_{TH} variation with t_{ox} for N_D= 5x10^{19} cm^{-3} , L_G= 20nm , t_{ox}= 1nm

Since above threshold regimes, subthreshold current flow is governed by bulk conduction mechanism so higher the bulk thickness more is the separation of the central potential line from the oxide-semiconductor interface and hence lesser is the gate control over current flow. Thus threshold voltage drops to very high negative values with increase in bulk thickness of Si as evident from Fig. 4.5.

4.3 Conclusion

In this chapter we derived classical threshold voltage of JLFET with an assumption of uniform doping of dopant atoms. We plotted variation of V_{TH} with different parameters of JLFET namely Gate Length (L_G), Dopant Concentration (N_D), Oxide Thickness (t_{ox}) and Bulk Thickness (t_{Si}) and observed behavior of those plots and provided plausible explanation for respective plots.

Chapter 5

Formulation of Threshold Voltage for a Uniformly doped short channel JLFET

In this chapter we would be presenting our model for formulation of threshold voltage in a uniformly doped short channel JLFET. We would be introducing concept of lattice site occupancy of dopant atoms to account for uniform doping and extend this concept for derivation of threshold voltage.

5.1. Formulation of Threshold Voltage using a new Model

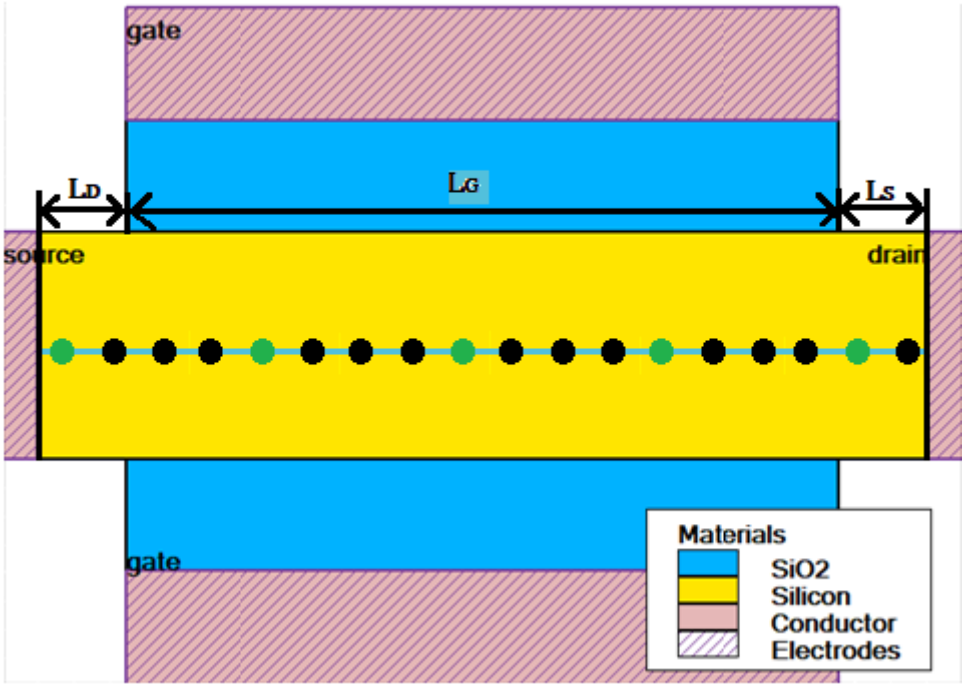

Fig.5.1: Model showing dopant atoms (green) spaced uniformly and occupying the lattice sites (black) along the central line of Si bulk in DG JLFET.

For uniform doping,donor atoms with dopant density (N_D) are uniformly distributed across the channel length.

Total number of donor dopant atoms in the bulk channel =$N_t = N_D V = N_D(W_{Si} t_{Si} L_g)$

We assume complete ionization of donors, so each donor atom contributes a free electron as charge carrier.

We would formulate threshold voltage under depletion regime,and therefore, assume that the bulk conduction of charge carriers is responsible for current flow.Thus the bulk channel is

formed along the central potential line.The assumption of uniform doping implies that the dopant atoms in the bulk channel would maintain uniform spacing between them.Also, each dopant atom is assumed to reside at lattice point in the lattice array spanning across the channel, as schematically shown in Fig.5.1.

We assume the first lattice site appearing at the metal-semiconductor interface on the source side.

Now,in counting of total lattice points occupied by donors, we take 2 lattice pointsfor the first lattice constantof Si bulk, say 'a_0', and additional single lattice pointsfor each subsequent lattice constants along the channel.

For any one dimensional lattice array of length 'L' with lattice constant 'a', the no. of lattice point simply taken as $\left\lfloor \frac{L}{a} \right\rfloor$ does not include the very first lattice point.

Thus, total number of lattice points should be $\left\lfloor \frac{L}{a} \right\rfloor + 1$

Or in other words,

Total number of lattice points should be $\left\lceil \frac{L}{a} \right\rceil$

Thus,
Total number of lattice points across the source and channel length along the central line $= \left\lceil \frac{L_S + L_G}{a_0} \right\rceil$

and Total number of lattice points in source side along the central line $= \left\lceil \frac{L_S}{a_0} \right\rceil$

Therefore, Total number of lattice points in the bulk channel $= \left\lceil \frac{L_S + L_G}{a_0} \right\rceil - \left\lceil \frac{L_S}{a_0} \right\rceil$

Now for uniform doping,the n^{th} dopant atom would occupy j^{th} lattice point such that

$$j = \left\lceil \frac{L_S}{a_0} \right\rceil + n \left\lfloor \frac{\left\lceil \frac{L_S + L_G}{a_0} \right\rceil - \left\lceil \frac{L_S}{a_0} \right\rceil}{N_D (W_{Si} t_{Si} L_g)} \right\rfloor \quad , n = 1,2 \ldots N_t \tag{5.1}$$

Now,we make an assumption that if the desired position for n^{th} dopant atom i.e. j^{th} lattice point has actually been occupied by a donor,the donor atom would be completely ionized and would contribute to the charge density of the device.

Theabove assumption is expressed mathematically as:

$$\rho' = \frac{q}{V}\sum_{n=1}^{N_t}\left(\sum_{k=\left\lceil\frac{L_S}{a_0}\right\rceil+1}^{k_{\max}=\left\lceil\frac{L_S+L_G}{a_0}\right\rceil-\left\lceil\frac{L_S}{a_0}\right\rceil} \delta[k-k']\,\delta\left[\left\lceil\frac{L_S}{a_0}\right\rceil + n\left\lfloor\frac{\left\lceil\frac{L_S+L_G}{a_0}\right\rceil-\left\lceil\frac{L_S}{a_0}\right\rceil}{N_D\left(W_{Si}t_{Si}L_g\right)}\right\rfloor - k'\right]\right)$$

$$where\ k' \in \left[\left\lceil\frac{L_S}{a_0}\right\rceil + 1, \left\lceil\frac{L_S+L_G}{a_0}\right\rceil - \left\lceil\frac{L_S}{a_0}\right\rceil\right] \qquad (5.2)$$

Equation (5.2) may seem obvious for uniform doping.

Thus, for threshold voltage calculation using the above approach, charge density ρ in Equation (4.40) obtained earlier, is replaced by ρ',leading to V_{TH}as:

$$V_{TH} = \frac{(8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1+4\beta_2\beta_3)(4V_{bi}(\beta_1\beta_3+\beta_2\beta_1 + V_{bi}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{\rho' t_{Si}}{2C_{ox}} - \frac{\rho' t_{Si}^2}{8\epsilon_{Si}} \qquad (5.3)$$

Relation between ρ' to ρ:

From Equation (4.41),

$$\rho = qN_D$$

We would now interpret equation (5.2) to find out its implication.

Having established jth lattice point for nth dopant atom occupancy in Uniform Doping using Eq.5.1,we need to verify if that jth lattice point been actually occupied by nth dopant atom in bulk channel across the central potential line.

For that,we introduce a Kronecker delta function as follows:

$$x_n = \sum_{k=\left\lceil\frac{L_S}{a_0}\right\rceil+1}^{k\_\max=\left\lceil\frac{L_S+L_G}{a_0}\right\rceil-\left\lceil\frac{L_S}{a_0}\right\rceil} \delta[k-k']\,\delta[\mathrm{j}-k'],\ n = 1,2..N_t \qquad (5.4)$$

Here x_n denotes the contribution of thenthdopant atom in depletion charge density in the semiconductor bulk.For particular nthdopant atom,we would calculate its desired jth lattice point as stated above.

Now,in the above equation (5.4), k' would give us the actual lattice point in bulk channel that has been occupied by the,n^{th}dopant atom, and $\sum_{k=\left\lceil\frac{L_S}{a_0}\right\rceil+1}^{k_\max=\left\lceil\frac{L_S+L_G}{a_0}\right\rceil-\left\lceil\frac{L_S}{a_0}\right\rceil}\delta[k-k']$would return 1 such that $\sum_{k=\left\lceil\frac{L_S}{a_0}\right\rceil+1}^{k\_\max=\left\lceil\frac{L_S+L_G}{a_0}\right\rceil-\left\lceil\frac{L_S}{a_0}\right\rceil}\delta[k-k']\,\delta[\mathrm{j}-k']$ becomes $\delta[\mathrm{j}-k']$.

Hence equation (5.4) gets simplified to

$$x_n = \delta[\mathrm{j}-k'] \tag{5.5}$$

Now if the lattice point actually occupied by n^{th}dopant atom matches with desired j^{th} lattice point, the Kronecker Delta Function would give 1,i.e$x_n = 1$, thenthdopant atom would contribute to the net charge density; otherwise $x_n$yields 0.

Similarly applying this approach for all the dopant atoms in bulk channel,we would get effective number of dopant atoms (n_{eff}) that would be contributing to charge density as:

$$n_{eff} = \sum_{n=1}^{N_t}\delta[\mathrm{j}-k'] \tag{5.6}$$

From equation (5.2),

$$\rho' = \frac{q}{V}n_{eff} \tag{5.7}$$

For uniform doping, n_{eff}=N_t,and equation (5.7) becomes

$$\rho' = \frac{q}{V}N_t$$

$$=> \rho' = \frac{q}{V}N_D(L_G W_{Si} t_{Si})$$

$$=> \rho' = \frac{q}{V}N_D(V)$$

$$=> \rho' = qN_D \tag{5.8}$$

So,for uniform doping,$\rho' = \rho$.

Hence the assumption that we have taken earlier is correct as the threshold voltage derived using ρ' is just the same as threshold voltage formulated earlier (Equation (4.40))using ρ .

We thus can also make a conclusion that threshold voltage that we have formulated earlier (Equation (4.40)) is just the corollary of Equation (5.3).

So Equation (5.3) gives the general expression for threshold voltage of JLFET.

As Equation (5.3) takes into account the occupancy of lattice points by donor dopants and their contribution to charge density, it would also explain variation of Threshold Voltage due to the phenomenon of Random Dopant Fluctuation (RDF), one of the SCEs appeared for significant shortening of channel length, which would be discussed later.

5.2Results and Discussion

Parameters used for MATLAB Simulation of our model are the same as given in Table 3.1.

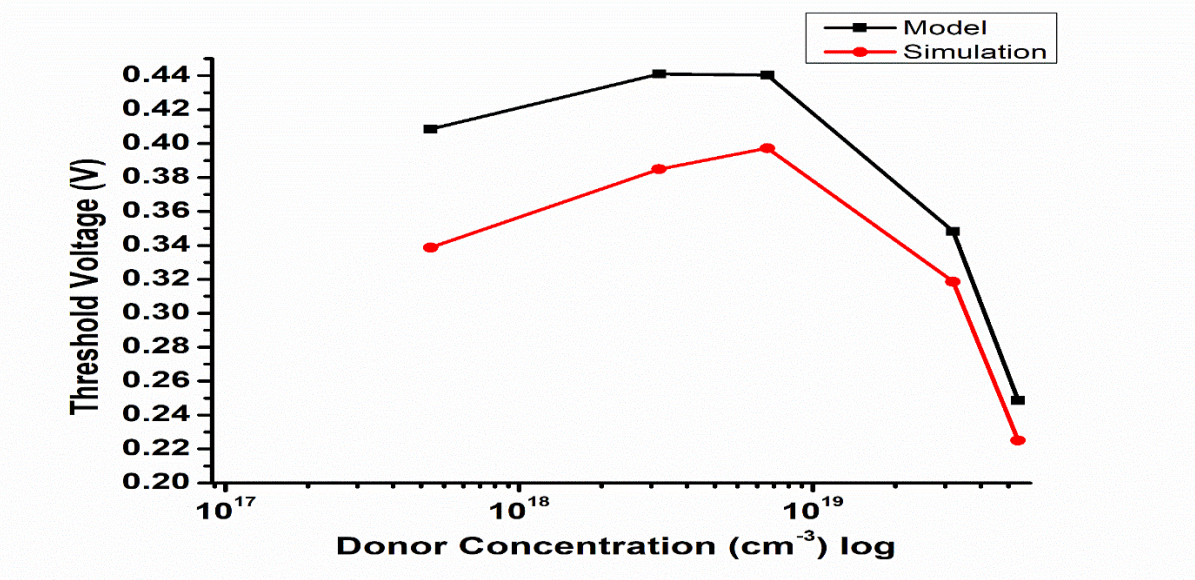

Fig.5.2. V_{TH} variation with $N_D$for t_{ox} = 1nm , L_G= 20nm , t_{Si}= 2nm

Fig.5.2. shows a comparison between the proposed model and simulation result for variation in threshold voltage (using Eq. 5.3) with different donor concentration. We could see although curves for both models follow the same nature described in Fig.4.2, difference of threshold voltage between model and simulation is largein lower donor concentration region (10^{17}-10^{18} cm^{-3}) in the range of (0.02 – 0.08) V and graduallydecreases beyond N_D= 2x10^{19} cm^{-3}.

Plausible explanation for such occurrence is due to the fact that the proposed model takes into account dopant atoms in the central line potential channel for threshold voltage calculations (using Eq. 5.7) and dopant atoms under gate channel get lower than smallest natural number i.e. 1 for low donor concentrations below the order of 10^{19} cm^{-3} (for particular physical parameters used in our JLFET). Since we consider dopant atoms mathematically to be natural numbers, for lower donor concentration, ρ' would be zero and threshold voltage would be having rather optimistic value(as described using Eq5.3).

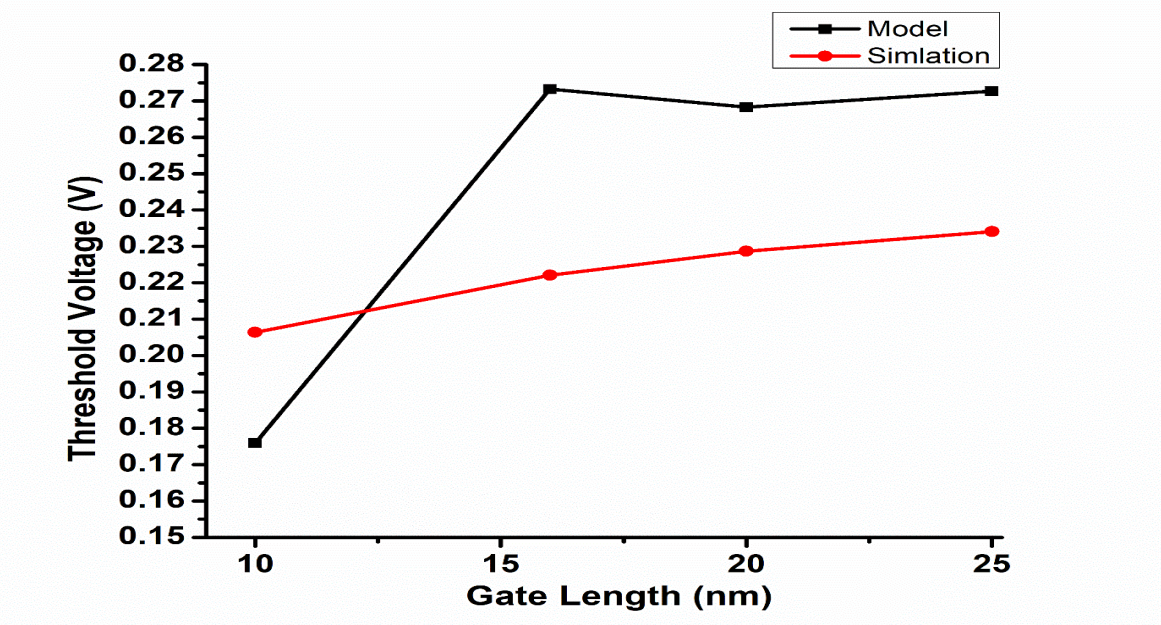

Fig.5.3. V_{TH} variation with L_G for t_{ox} = 1nm , N_D= 5x10^{19} cm^{-3} , t_{Si}= 2nm

From Fig.5.3, simulation provides a sort of piecewise linear variation of threshold voltage with gate length and variation is limited to around (0.204 - 0.225)V. On the other hand, proposed model shows greater threshold variation with a steeper slope compared to simulation when gate length is below 10 nm. Threshold voltage of the model differ from simulation by the range of $\pm$0.04 V.

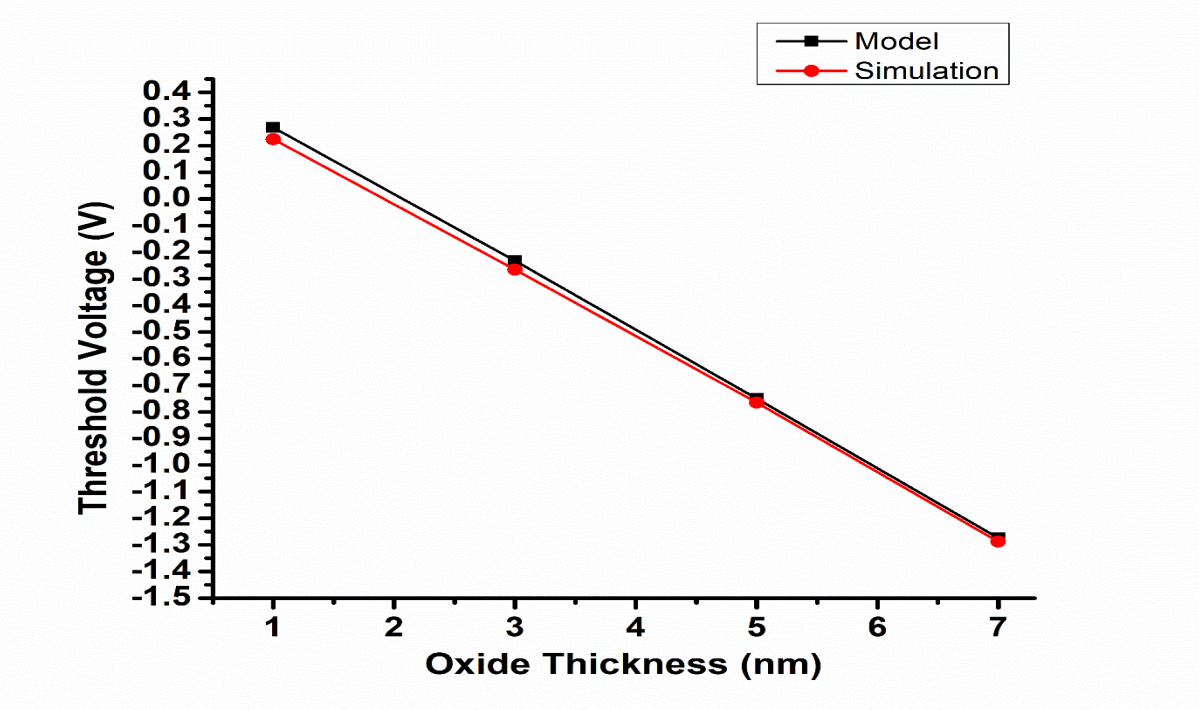

Fig.5.4. V_{TH} variation with t_{ox} for L_G = 20nm , N_D = 5x10^{19} cm^{-3} , t_{Si}= 2nm

Fig.5.4 reveals that the Threshold Voltages obtained from both simulation and proposed model are almost of the same valuespecifically for large values of t_{ox} , and with variation in the oxide thickness, the difference in two set of threshold voltages is nominal.

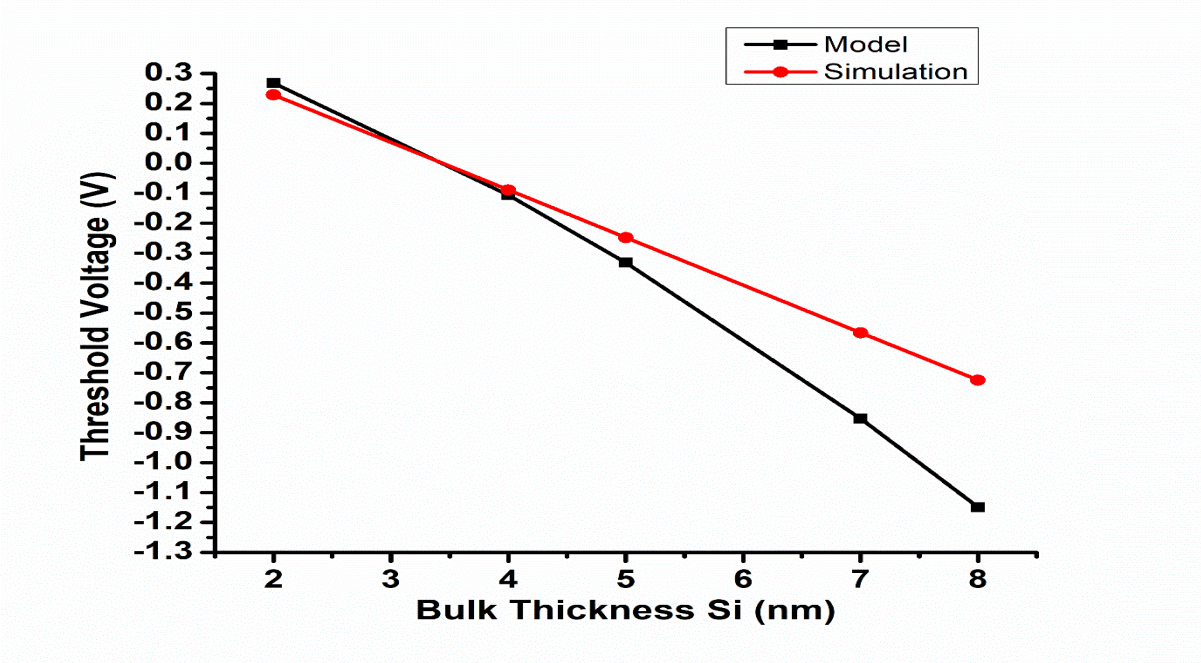

Fig.5.5. V_{TH} variation with $t_{Si}$for t_{ox} = 1nm , N_D = 5x10^{19} cm^{-3} , L_G = 20nm.

It is shown in Fig.5.5 that the Threshold voltage of the proposed model almost merges with that of the simulation model for bulk thickness of Si up to 4 nm, and starts gradually deviatingfor increasing bulk thicknesses (ranging till -0.5V).

5.3 Conclusion

In this chapter , we proposed a new model for derivation of threshold voltage of JLFET using the concept of lattice site occupancy by dopant atoms and compared with simulation results for variation of V_{TH} with different physical parameters of JLFET. We concluded a maximum deviation of 25% of V_{TH} with variation with $N_D$for N_D= 5x10^{17} cm^{-3}.While variation of V_{TH} with L_G,maximum deviation of 18% was obtained for L_G = 25nm .Whereas on variation of V_{TH} with t_{ox} and t_{Si},deviation was found to be 1% (for t_{ox} = 7nm) and -71% (for t_{Si} = 8nm) respectively.

Chapter 6

Formulation of Threshold Voltage of JLFET under Quantum Confinement

As the channel length of JLFET we have taken into account is very short and comparable to wavelength of electron,Quantum Effects would significantly influence physical parameters of our device.From the energy band diagram (shown in Fig. 2.9)of DG JLFET under subthreshold condition , we can infer that electrons in the conduction band are confined in a Quantum Well, which is of parabolic nature at the bottom and bounded by oxide layers offering infinitely high potential barrier.

6.1 Derivation of Threshold Voltage of Quantum Confined JLFET

Potential Energy in a parabolic potential well, $V(z) = \frac{1}{2}kz^2$which analogously describes the behavior of a harmonic oscillator.In other words,electrons occupying energy sub-bands in parabolic potential well would exhibit harmonic oscillations with natural frequency ω_0, such that:

$$z = z_0 cos\omega_0 t \, , z_0 \; is \; amplitude \; of \; oscillation \tag{6.1}$$

$$\text{where}, \omega_0 = \sqrt{\frac{k}{m_e^*}}, k \; is \; constant, m_e^* \; is \; effective \; mass \; of \; electron \tag{6.2}$$

We would now solve one dimensional Time Independent Schrodinger Equation with potential energy,$V(z) = \frac{1}{2}kz^2$to find out energy states of electron in a parabolic potential well.

$$\left(-\frac{\hbar^2}{2m_e^*}\frac{d^2}{dz^2} + V(z)\right)\psi(z) = \varepsilon_n\psi(z) \tag{6.3}$$

$$=> \left(-\frac{\hbar^2}{2m_e^*}\frac{d^2}{dz^2} + \frac{1}{2}kz^2\right)\psi(z) = \varepsilon_n\psi(z)$$

Substituting value of k from Equation (6.2),

$$=> \left(-\frac{\hbar^2}{2m_e^*}\frac{d^2}{dz^2} + \frac{m_e^*\omega_0^2 z^2}{2}\right)\psi(z) = \varepsilon_n\psi(z)$$

On multiplying both sides by $-\frac{2m_e^*}{\hbar^2}$,

$$=> \left(\frac{d^2}{dz^2} - \frac{m_e^{*2}\omega_0^2 z^2}{\hbar^2}\right)\psi(z) = -\frac{2m_e^*\varepsilon_n}{\hbar^2}\psi(z) \tag{6.4}$$

We would now transform physical parameters of equation (6.4) into dimensionless variables to make it as a mathematical problem and can be solved 2nd Order Ordinary Differential Equation.

We introduce a dimensionless variable $\bar{z}$ with a length scale factor z_0 such that $z = z_0\bar{z}$,

Substituting value of 'z' in Equation (6.4),we get

$$\left(\frac{d^2}{d\bar{z}^2} - \frac{m_e^{*2}\omega_0^2 z_0^4 \bar{z}^2}{\hbar^2}\right)\psi(\bar{z}) = -\frac{2z_0^2 m_e^*\varepsilon_n}{\hbar^2}\psi(\bar{z}) \tag{6.5}$$

We would now make each term dimensionless of equation (6.5),

$$\left[\frac{d^2}{d\bar{z}^2}\right] = 1$$

To make $\left[\frac{m_e^{*2}\omega_0^2 z_0^4}{\hbar^2}\right] = 1$, we substitute $z_0 = \sqrt{\frac{\hbar}{m_e^*\omega_0}}$

Similarly to make $\left[\frac{2z_0^2 m_e^*\varepsilon_n}{\hbar^2}\right] = 1$, we substitute $\varepsilon_n = \varepsilon_0\bar{\varepsilon}_n$,

where ε_0 is a energy scale factor such that $\varepsilon_0 = \hbar\omega_0$

Hence Equation (6.5) becomes :

$$\left(\frac{d^2}{d\bar{z}^2} - \bar{z}^2\right)\psi(\bar{z}) = -2\bar{\varepsilon}_n\psi(\bar{z})$$

$$=> \frac{d^2\psi(\bar{z})}{d\bar{z}^2} + (2\bar{\varepsilon}_n - \bar{z}^2)\psi(\bar{z}) = 0 \tag{6.6}$$

We now substitute $\psi(\bar{z}) = e^{-\frac{\bar{z}^2}{2}}u(\bar{z})$ to remove $\bar{z}^2$ term from equation (6.6),

After quite a long differential and algebraic simplification Equation (6.6) becomes:

$$\frac{d^2u(\bar{z})}{d\bar{z}^2}e^{-\frac{\bar{z}^2}{2}} - 2\bar{z}e^{-\frac{\bar{z}^2}{2}}\frac{du(\bar{z})}{d\bar{z}} + \bar{z}^2e^{-\frac{\bar{z}^2}{2}}u(\bar{z}) - e^{-\frac{\bar{z}^2}{2}}u(\bar{z}) + 2\bar{\varepsilon}_n e^{-\frac{\bar{z}^2}{2}}u(\bar{z}) - \bar{z}^2e^{-\frac{\bar{z}^2}{2}}u(\bar{z}) - e^{-\frac{\bar{z}^2}{2}} = 0$$

$$=> \frac{d^2u(\bar{z})}{d\bar{z}^2} - 2\bar{z}\frac{du(\bar{z})}{d\bar{z}} + 2\left(\frac{2\bar{\varepsilon}_n - 1}{2}\right)u(\bar{z}) = 0 \tag{6.7}$$

If Equation (6.7) takes the form of Hermite's Equation then $u(\bar{z})$ can be expressed in the form of Hermite's Polynomials.For that coefficient of $u(\bar{z})$ must be an non-negative even integer.

So,

$$2\left(\frac{2\bar{\varepsilon}_n - 1}{2}\right) = 2n\,, n = 0,1,2,3\ldots. \quad (6.8)$$

$$=> \bar{\varepsilon}_n = n + \frac{1}{2} (6.9)$$

$$=> \varepsilon_n = \left(n + \frac{1}{2}\right)\varepsilon_0$$

$$=> \varepsilon_n = \left(n + \frac{1}{2}\right)\hbar\omega_0\,, n = 0,1,2,3.. \quad (6.10)$$

Thus,energy levels of electron behaving as harmonic oscillator in a parabolic quantum well are equally spaced by $\hbar\omega_0$ above a zero point energy of $\frac{1}{2}\hbar\omega_0$.

Equation (6.10) can be rewritten as:

$$E_n = \left(n + \frac{1}{2}\right)\hbar\sqrt{\frac{k}{m_e^*}}\,, n = 0,1,2,3.. \quad (6.11)$$

Since we are operating under subthreshold region.so we can decouple Poisson's Equation and Schrodinger Equation.This advantage would help us in finding the unknown constant 'k'.

Using 1D Poisson's Equation:

$$\nabla^2\varphi = -\frac{\rho}{\epsilon_{Si}}$$

$$\frac{d^2\varphi}{dz^2} = -\frac{qN_D}{\epsilon_{Si}}\,, q = |e|,' e' is\ charge\ of\ electron \quad (6.12)$$

On integrating both sideswith integral limits from 0 to z,

$$\varphi(z) = -\frac{qN_D z^2}{2\epsilon_{Si}} \quad (6.13)$$

$$Now, V(z) = \frac{1}{2}kz^2$$

$$=> -|e|\varphi(z) = \frac{1}{2}kz^2$$

$$=> \frac{q^2 N_D z^2}{2\epsilon_{Si}} = \frac{1}{2}kz^2$$

$$or,\quad k = \frac{q^2 N_D}{\epsilon_{Si}} \quad (6.14)$$

Putting value of 'k' from Equation (6.14) into (6.11),we get:

$$E_n = \left(n + \frac{1}{2}\right) \hbar \sqrt{\frac{q^2 N_D}{\epsilon_{Si} m_e^*}}\ , n = 0,1,2,3.. \qquad (6.15)$$

We now need to find 3D Density of states that could be occupied by electrons in conduction band valley and accordingly find electron concentration across all the energy levels in the conduction band.

3D Density of States Derivation:

The state of electron is specified by its position vector $\vec{r} = x\hat{\imath} + y\hat{\jmath} + z\hat{k}$ and momentum vector $\vec{p} = p_x\hat{\imath} + p_y\hat{\jmath} + p_z\hat{k}$ in phase space.In classical mechanics,both position and momentum states can be precisely determined by a point in the phase space.

But state of electron under quantum regime is non-deterministic rather probabilistic in the phase space . According to Heisenberg's Uncertainty Principle,

$$\Delta x \Delta p_x \sim h, \Delta y \Delta p_y \sim h, \Delta z \Delta p_z \sim h$$

Hence , state of an electron cannot be determined by a point in the phase space rather by a cell of finite phase space volume $(\Delta x \Delta p_x).\left(\Delta y \Delta p_y\right).(\Delta z \Delta p_z) \sim h^3)$ in the phase space. Thus only a single electron can be accommodated in a cell of phase space volume h^3.

$$\text{Number of available states for electron} = \frac{\text{Volume of phase space}}{h^3} \qquad (6.16)$$

Volume of phase space for a single electron $=h^3$

Thus,from equation (6.16) ,we can conclude only one state is possible for a single electron.

Let N(E)dE be the number of electronic states per unit volume between energy range of E and E+dE , then

Using equation (6.16),

$$N(E)dE = 2g\frac{dp_x dp_y dp_z}{h^3} (6.17)$$

where , $dp_x dp_y dp_z$is the volume in the momentum space within which electron energy liesbetween E a dE, g is the degeneracy i.e. number of equivalent minima in the conduction band and 2 factor accounts for Up and Down Spin of electron

If the electron kinetic energy is not too high then we can safely consider the energy-momentum relation of electron near the minima of conduction band to be parabolic such that:

$$E - E_{min} = \frac{p_x^2}{2m_x} + \frac{p_y^2}{2m_y} + \frac{p_z^2}{2m_z} \tag{6.18}$$

On rearranging equation (6.18),

$$1 = \frac{p_x^2}{2m_x(E - E_{min})} + \frac{p_y^2}{2m_y(E - E_{min})} + \frac{p_z^2}{2m_z(E - E_{min})} \tag{6.19}$$

Equation (6.19) describes a ellipsoid in momentum space where m_x represents effective mass along longitudinal axis,$m_y and\ m_z$represents effective masses along other two transverse axes respectively and $E - E_{min}$ is the Kinetic energy of the electron,$E_{min}$is the lowest sub-band energy level occupied by the electron.

$$\text{Now, Volume of the ellipsoid} = \frac{4}{3}\pi\left(\sqrt{2m_x(E - E_{min})}\right)\left(\sqrt{2m_y(E - E_{min})}\right)\left(\sqrt{2m_z(E - E_{min})}\right)$$

$$= \frac{4}{3}\pi\left(8m_x m_y m_z\right)^{\frac{1}{2}}(E - E_{min})^{\frac{3}{2}} \tag{6.20}$$

In order to find infinitesimal increment of volume in momentum space ($dp_x dp_y dp_z$)within which the electron energy lies between E and E+dE,we need to obtain infinitesimal increment of volume of ellipsoid in momentum space.

But since Equation (6.20) is also a function of E so we would be differentiating both sides by E to get,

$$dV = 4\pi\left(2m_x m_y m_z\right)^{\frac{1}{2}}(E - E_{min})^{\frac{1}{2}}dE$$

$$=> dp_x dp_y dp_z = 4\pi\left(2m_x m_y m_z\right)^{\frac{1}{2}}(E - E_{min})^{\frac{1}{2}}dE \tag{6.21}$$

Putting value of $dp_x dp_y dp_z$from Equation (6.21) to (6.17),

$$N(E) = \frac{8\pi g\left(2m_x m_y m_z\right)^{\frac{1}{2}}(E - E_{min})^{\frac{1}{2}}}{h^3} \tag{6.22}$$

Total number of electrons per unit volume occupying vacant energy states in the conduction band is given by

$$n = \int_{E_{min}}^{\infty} f(E)N(E)dE\ ,\ \ f(E)\ is\ Fermi - Dirac\ distribution$$

$$=> n = \int_{E_{min}}^{\infty} \frac{1}{1 + e^{\frac{E - E_F}{k_B T}}} \cdot \frac{8\pi g\left(2m_x m_y m_z\right)^{\frac{1}{2}}(E - E_{min})^{\frac{1}{2}}}{h^3} dE\ ,\ \ E_F\ is\ Fermi\ Energy\ Level$$

Using Boltzmann Approximation,$E - E_F > 3\mathrm{k_B T}, k_B\ is\ Boltzmann\ Constant$

$$=> n = \int_{E_{min}}^{\infty} e^{-\frac{E-E_F}{k_BT}} . \frac{8\pi g\left(2m_x m_y m_z\right)^{\frac{1}{2}} (E - E_{min})^{\frac{1}{2}}}{h^3} dE$$

On solving above integral,

$$=> n = \frac{8\pi g\left(2m_x m_y m_z\right)^{\frac{1}{2}}}{h^3} e^{-\frac{E_{min}-E_F}{k_BT}} \Gamma\left(\frac{1}{2}\right) (k_BT)^{\frac{3}{2}}$$

$$=> n = 2g\left(\frac{2\pi k_BT}{h^2}\right)^{\frac{3}{2}} \sqrt{m_x m_y m_z} e^{-\frac{E_{min}-E_F}{k_BT}} \quad (6.23)$$

$$E_{min} = E_C' + E_j \, , E_j \; is \; the \; minimum \; energy \; for \; j^{th} sub - band$$

$$=> E_{min} = E_C - q\psi_B + E_j, \psi_B \; is \; Bulk \; Potential \quad (6.24)$$

Till now,we assumed all six minima of conduction band of Silicon having equivalent energies with g=6, in <100> direction wave vector.

But under quantum confinement ,the minimum conduction band valley gets split into two valleys ,one with lower energy and degeneracy (g=2) and m_x is longitudinal effective mass of electron and the other valley with higher energy having degeneracy (g=4) and m_x' is transverse effective mass of electron.

For lower energy valley , E_{min} for j^{th} sub-band $= E_C - q\psi_B + E_j$ (6.25)

For higher energy valley , E_{min}' for j'^{th} sub-band $= E_C - q\psi_B + E_j'$ (6.26)

From Equation (6.15),

$$E_j = \left(j + \frac{1}{2}\right) \hbar \sqrt{\frac{q^2 N_D}{\epsilon_{Si} m_e^*}} \, , j = 0,1,2,3.. \quad (6.27)$$

$$E_j' = \left(j' + \frac{1}{2}\right) \hbar \sqrt{\frac{q^2 N_D}{\epsilon_{Si} m_e^{*\prime}}} \, , j' = 0,1,2,3.. \quad (6.28)$$

Total charge density summing over all sub-bands in both valleys,

$$Q_t^{QM} = qn$$

From equation (6.23),

$$=> Q_t^{QM} = q\left[\sum_j 2(2)\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_x m_y m_z}\,e^{-\frac{E_{min}-E_F}{k_B T}} + \sum_{j'} 2(4)\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m'_x m'_y m'_z}\,e^{-\frac{E'_{min}-E_F}{k_B T}}\right]$$

Using Equation (6.25) and (6.26),

$$=> Q_t^{QM} = q\left[\sum_j 4\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\,e^{-\frac{E_C-q\psi_B+E_j-E_F}{k_B T}} + \sum_{j'} 8\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_t m_l m_t}\,e^{-\frac{E_C-q\psi_B+E'_j-E_F}{k_B T}}\right]$$

$$=> Q_t^{QM} = 4q\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\,e^{-\frac{E_C-E_F-q\psi_B}{k_B T}}\left[\sum_j e^{-\frac{E_j}{k_B T}} + 2\sum_{j'} e^{-\frac{E'_j}{k_B T}}\right]$$

Using Equation (6.27) and (6.28) and putting $\xi = \frac{\hbar}{\mathrm{k_B}T}\sqrt{\frac{q^2 N_D}{\epsilon_{Si}}}$, *we get*

$$=> Q_t^{QM} = 4q\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\,e^{-\frac{E_C-E_F-q\psi_B}{k_B T}}\left[e^{-\frac{1}{2}\left(\frac{\xi}{\sqrt{m_l}}\right)}\sum_{j=0,1,2..} e^{-\frac{j\xi}{\sqrt{m_l}}} + 2e^{-\frac{1}{2}\left(\frac{\xi}{\sqrt{m_l}}\right)}\sum_{j'=0,1,2,..} e^{-\frac{j'\xi}{\sqrt{m_l}}}\right]$$

$$=> Q_t^{QM} = 4q\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\,e^{-\frac{E_C-E_F-q\psi_B}{k_B T}}\left[\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1-e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1-e^{-\frac{\xi}{\sqrt{m_t}}}}\right] \quad (6.29)$$

Now,threshold voltage shift due to Quantum Confinement effects can be expressed as [71]:

$$\Delta V_{TH}^{QM} = \frac{k_B T}{q} ln\left(\frac{n_{3D}^{CL}}{n_{3D}^{QM}}\right) \quad (6.30)$$

Degeneracy of conduction band minima in Silicon is g=6 without Quantum Confinement effects.So electron concentration occupying conduction band energy levels without any Quantum Confinement effects having longitudinal effective mass of electron along X axis,

From equation (6.23),

$$n_{3D}^{CL} = 2(6)\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\, e^{-\frac{E_{min}^{CL}-E_F}{k_B T}} \tag{6.31}$$

Now,E_{min}^{CL}doesn't take into account any term responsible for Quantum Effects.

Thus we need to ignore the Energy eigen value of Quantum Harmonic Oscillator.

$$E_{min}^{CL} = E_C - q\psi_B \tag{6.32}$$

Putting value of E_{min}^{CL} from equation (6.32) into (6.31),

$$n_{3D}^{CL} = 12\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\, e^{-\frac{E_C-q\psi_B-E_F}{k_B T}} \tag{6.33}$$

Now ,

$$n_{3D}^{QM} = \frac{Q_t^{QM}}{q}$$

Substituting value of Q_t^{QM} from Equation (6.29),

$$=> n_{3D}^{QM} = 4\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}}\sqrt{m_l m_t^2}\, e^{-\frac{E_C-E_F-q\psi_B}{k_B T}}\left[\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1-e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1-e^{-\frac{\xi}{\sqrt{m_t}}}}\right] \tag{6.34}$$

From Equation (6.33) and (6.34),

$$\frac{n_{3D}^{CL}}{n_{3D}^{QM}} = \frac{3}{\left(\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1-e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1-e^{-\frac{\xi}{\sqrt{m_t}}}}\right)} \tag{6.35}$$

Putting value of Equation (6.35) in (6.30),

$$\Delta V_{TH}^{QM} = \frac{k_B T}{q}\left(\ln(3) - \ln\left(\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1-e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1-e^{-\frac{\xi}{\sqrt{m_t}}}}\right)\right) \tag{6.36}$$

Now,

Threshold voltage of JLFET under Quantum Confinement effects can expressed as :

$$V_{TH}^{CL+QM} = V_{TH}^{CL} + \Delta V_{TH}^{QM} \tag{6.37}$$

From Equation (4.42),

$$V_{TH}^{CL} = \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{\rho t_{Si}}{2C_{ox}} - \frac{\rho t_{Si}^2}{8\epsilon_{Si}} \quad (6.38)$$

Also,since $\rho = \rho'$ in uniform doping (explained in section 5.1),we can state:

$$V_{TH}^{CL} = \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{\rho' t_{Si}}{2C_{ox}} - \frac{\rho' t_{Si}^2}{8\epsilon_{Si}} \quad (6.39)$$

Combining Equation (6.36) and (6.39) into (6.37),

$$V_{TH}^{CL+QM} = \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2} + V_{FB} - \frac{\rho' t_{Si}}{2C_{ox}} - \frac{\rho' t_{Si}^2}{8\epsilon_{Si}} + \frac{k_B T}{q}\left(\ln(3) - \ln\left(\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1 - e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1 - e^{-\frac{\xi}{\sqrt{m_t}}}}\right)\right) \quad (6.40)$$

Therefore, the final expression for Threshold Voltage of JLFET under Quantum Confinement effects is given by Equation (6.40).

6.2Results and Discussion

For solution of 2D Schrodinger Equation and inclusion of Quantum Confinement effects in simulation, we used Bohm Quantum Potential (BQP) Model and properly calibrated it against coupled Schrodinger-Poisson (SP) Model under No Current Condition. For this, quasi-static Capacitance – Voltage (*C-V*) characteristics simulated for the above two models are presented in Fig.6.1, with appropriate BQP parameters yielding closest match between them.

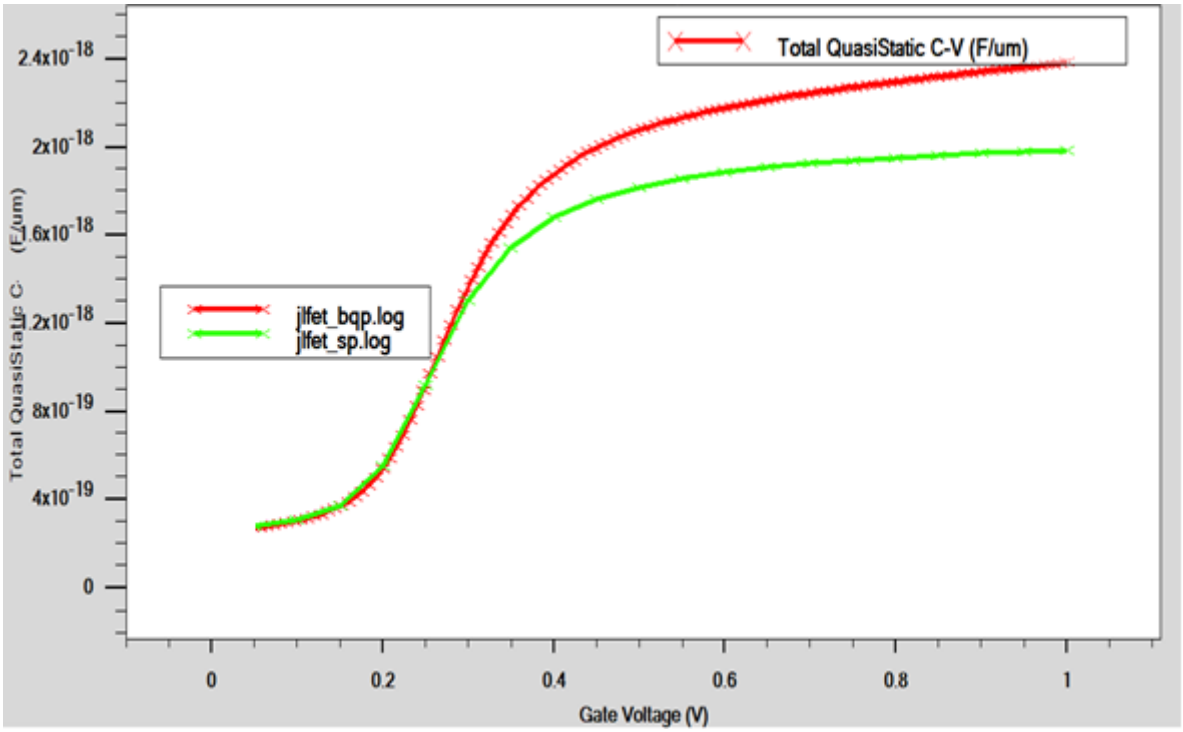

Fig.6.1:Total quasi-static CV showing the closest match between BQP and SP for BQP parameters , $\gamma = 0.36$, $\alpha = 0.16$.

We could see from Fig. 6.2. that the threshold voltage of the proposed model differ significantly from the simulation (ranging from -0.35V to 0.01V)fordonor concentrations below $5x10^{19}$ cm^{-3} and almost merges with that above $5x10^{19}$ cm^{-3}.For low donor concentrations, band bending in conduction band is not prominent for quantum confinement to occur. So, imposing quantum confinement effects in the proposed model would rather yield lowered threshold voltages, thereby causing large deviations from simulation results. On the other hand, for high donor concentrations, quantum confinement effects take place due to onset of quantum parabolic well, and thus introduction of quantum confinement effects in the model becomes reasonable,resulting in the same results as of the simulation.

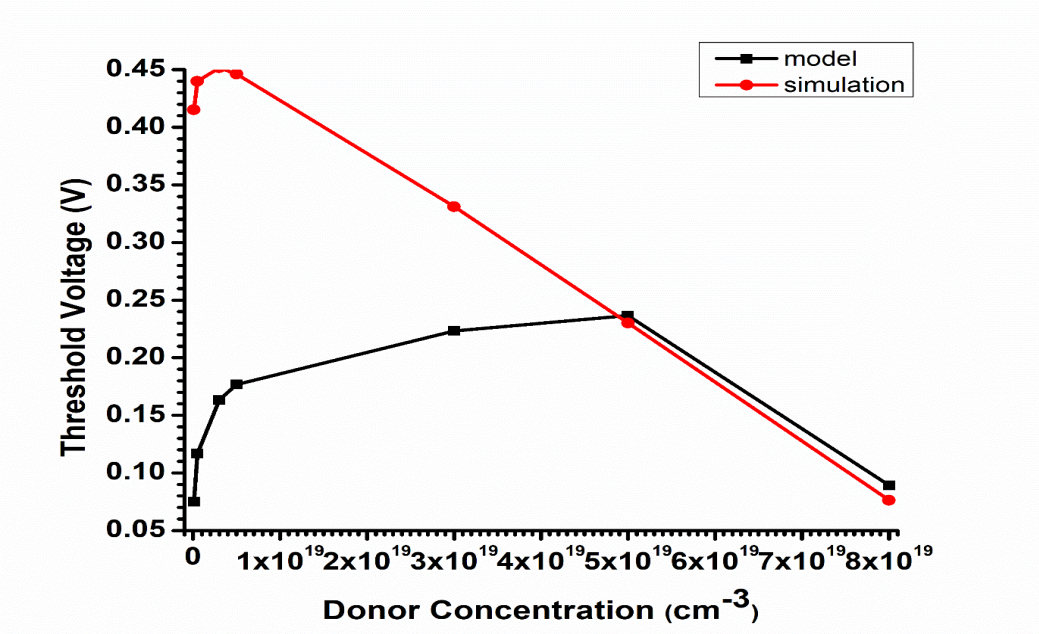

Fig.6.2: V_{TH} variation with N_D under Quantum Confinement for t_{ox}=1nm, L_G=20nm,t_{Si}= 2nm.

As Si bulk thickness increases, potential barrier of parabolic quantum well gradually gets lowered and weakens the carrier confinement. As a consequence, threshold voltage for the JLFET falls more rapidly with increase in t_{Si} in the case of proposed model, as shown in Fig. 6.3(ranging till -1.12V).

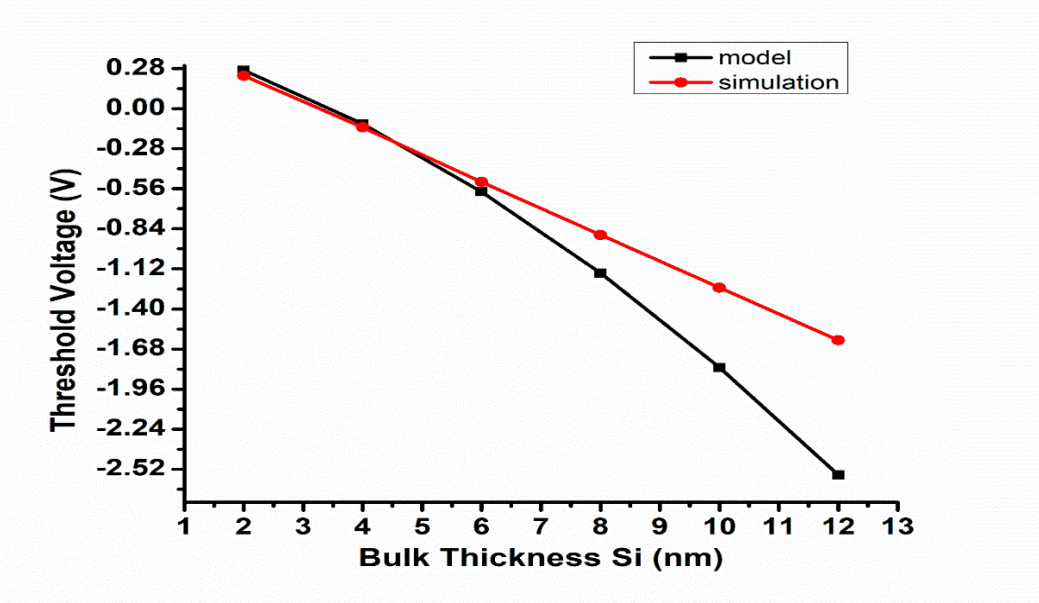

Fig.6.3: V_{TH} variation with t_{Si} under Quantum Confinement fort_{ox} = 1nm , N_D = 5x10^{19} cm^{-3}and L_G = 20nm.

Fig. 6.4 shows that the Threshold Voltage of the model exactly matches with simulation up to an oxide thickness of 5 nm.With increase in oxide thickness above 5nm,quantum confinement effects tend to get lower resulting in slight divergence of threshold voltage of the model from simulation within range of 0.03V .

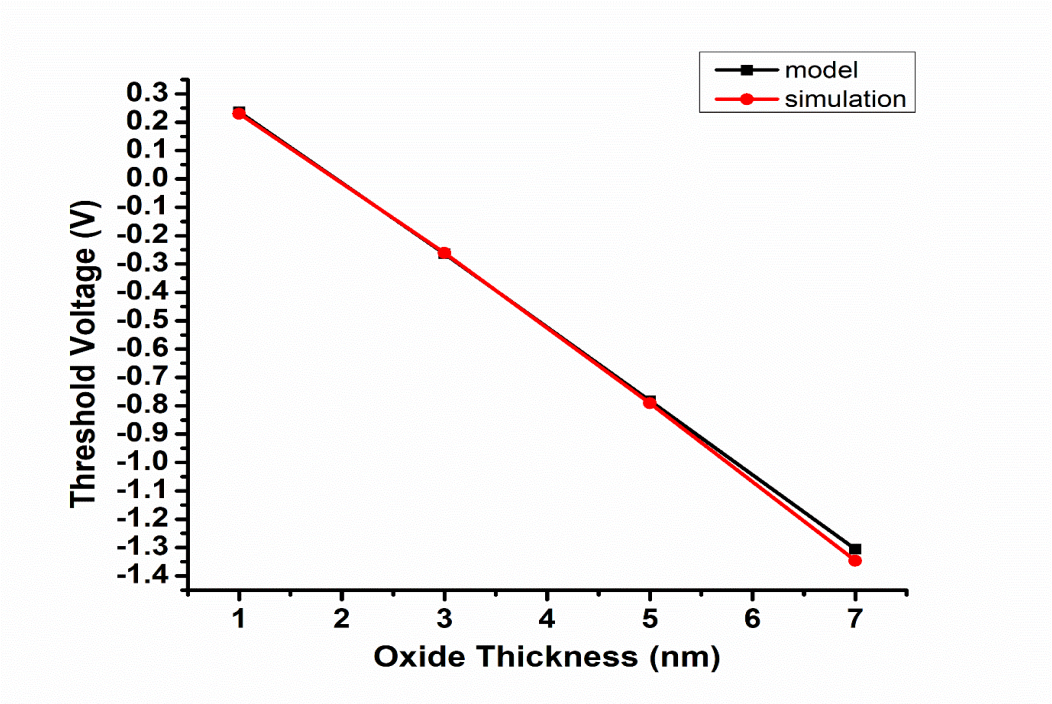

Fig.6.4: V_{TH} variation with t_{ox} under Quantum Confinement for L_G = 20nm , $N_D = 5x10^{19}\ cm^{-3}$, t_{Si}= 2nm

6.3 Conclusion

Variations in Threshold voltage with various physical parameters of the device are found to more-or-less match for the proposed model and simulation, thus proving the correctness of the approach adopted for quantum confinement in the model.

Chapter 7

Analysis of Random Dopant Fluctuationand its impact on Threshold Voltage of JLFET

In Chapter 5, we have already formulated Threshold voltage in uniform doping JLFET using a detailed approach taking into account spatial variation of dopant atoms in bulk channel region.

Now, as channel of JLFET is shortened to nano-scales, number of ionized dopant atoms participating in charge density under depletion regime are very less compared to long channel devices,making dopant atoms in the bulk channel discrete in positions and energy levels.

To account for discreteness in spatial locations of dopant atoms in bulk channel, we have alreadyintroduced an approach that takes into account their occupancy in lattice points of the channel.

7.1 Derivation of Threshold Voltage under RDFusing newModel

Here, we will formulate the threshold voltage of JLFET in depletion region, where current conduction occurs through bulk channel, and ionized dopant atoms provide the free electrons that contribute to bulk current through drift mechanism. Thus, all the ionized dopant atoms are located in the bulk channel and total charge contributed by them is the depletion charges under bulk conduction regime.

Using equation (5.7),charge density under bulk conduction regime with uniform doping is given by:

$$\rho' = \frac{q}{V} n_{eff}$$

We have seen , for uniform doping, $n_{eff} = N_t$,
where N_t is the total number of ionized dopants in bulk channel.

However, in practical cases, dopant atoms do not occupy the desired lattice sites that areexpected theoretically;rather they undergo fluctuations in their spatial positions. In other words, dopant atoms occupy some other different lattice positions that were not supposed to

occupy in case of uniform doping.The lattice position each dopant atom would occupy cannot be predicted beforehand. Such this randomness in lattice position occupancy of dopant atoms due to discreteness of atoms gives rise to Random Dopant Fluctuations (RDF) phenomenon.

Let us now explore RDF with further clarity.

In uniform doping, we calculate desired j^{th} lattice point for n^{th} dopant atom occupancy using equation (5.1) and we verify if that j^{th} lattice point been actually occupied by n^{th} dopant atom in bulk channel across the central potential line.

For that,we introduce a Kronecker delta function as follows :

$$x_n = \sum_{k=\left\lceil \frac{L_S}{a_0} \right\rceil + 1}^{k\_\max = \left\lceil \frac{L_S + L_G}{a_0} \right\rceil - \left\lceil \frac{L_S}{a_0} \right\rceil} \delta[k - k'] \, \delta[\mathrm{j} - k'] \, , n = 1,2,\ldots . N_t \quad (From\ equation\ 5.4)$$

Here,x_n denotes the contribution of n^{th}dopant atom in depletion charge density in the semiconductor bulk, k' gave us the actual lattice point in bulk channel that has been occupied by thenthdopant atom.

For uniform doping ,x_n had been 'ONE' for all dopant atoms .In other words, k'lattice point becomes practically equivalent to j^{th} lattice point thus makingn_{eff} equal to total ionized dopant atoms in bulk channel, .i.e. $n_{eff} = N_t$.

However, due to RDF in uniform doping,x_n would not be 'ONE' for all the dopant atoms rather only for a few dopant atoms.So, k'lattice point is now random and thus probability for it to become equivalent to j^{th} lattice is completely random. So, in the presence of RDF, $n_{eff} \neq N_t$.

Thus , in our mathematical model, we need to introduce a term that would account for randomness on the k'lattice point.

Equation 5.4 here gets modified as :

$$x'_n = \sum_{k=\left\lceil \frac{L_S}{a_0} \right\rceil + 1}^{k\_\max = \left\lceil \frac{L_S + L_G}{a_0} \right\rceil - \left\lceil \frac{L_S}{a_0} \right\rceil} \delta[k - (\eta + k')] \, \delta[\mathrm{j} - (\eta + k')] \, , n = 1,2..N_t \qquad (7.1)$$

where,$\eta$is the factor that accounts for randomness in k'lattice point.

Now, the range of η needs to be chosen such a way that it can either pull down k' to the lowest lattice position or push up k'to the highest lattice position in the bulk channel

alongwith putting k' somewhere between the two extreme lattice positions, lattice positions being counted from the source side as presented in the model in Fig. 5.1.

Therefore,with an assumption that a lattice position can be occupied by one dopant atom only, ηbeing an integer, can randomlyvary within the range $\left[\left[\frac{L_S}{a_0}\right]+1-k', \left[\frac{L_S+L_G}{a_0}\right]-\left[\frac{L_S}{a_0}\right]-k'\right]$.

Now, for n^{th}dopant atom ,desired j^{th} lattice point may not be obtained by$(\eta+k')$ lattice point due to RDF. Then, x_n would give 0 that means n^{th}dopant atom would not contribute to charge density.

Now summing for all dopant atoms in the bulk channel, we write

$$n'_{eff}=\sum_{n=1}^{N_t}\delta[\mathrm{j}-(\eta+k')] \tag{7.2}$$

where, due to RDF ,n'_{eff}would not be equal to total number of dopant atoms in the bulk channel.

Now, charge density under bulk conduction regime due to RDF becomes:

$$\rho'_{RDF}=\frac{q}{V}n'_{eff} \tag{7.3}$$

Modifying Equation (5.3)using (7.3),

Threshold voltage due to RDF becomes :

$$V_{TH\_RDF}=\frac{(8\mathrm{V_{bi}}\beta_2\beta_3+4\beta_1\beta_2+4\beta_1\beta_3)-\left((8\mathrm{V_{bi}}\beta_2\beta_3+4\beta_1\beta_2+4\beta_1\beta_3)^2-4(1+4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3+\beta_2\beta_1+\mathrm{V_{bi}}\beta_2\beta_3)+\beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3+2}+V_{FB}-\frac{\rho'_{RDF}t_{Si}}{2C_{ox}}-\frac{\rho'_{RDF}t_{Si}^2}{8\epsilon_{Si}} \tag{7.4}$$

7.2 Introducing Random Factor for Model Simulation under RDF effects

We would now look into properties of the Random Factor for simulating RDF effects in our model.

Properties of Random Factor ,η:

- Random Factor (η) is a random integer varying between $\left(\left\lceil\frac{L_S}{a_0}\right\rceil + 1 - k'\right)$ and$\left(\left\lceil\frac{L_S+L_G}{a_0}\right\rceil - \left\lceil\frac{L_S}{a_0}\right\rceil - k'\right)$,where k' is the lattice position occupied by dopant atom in the channel region.
- RDF gets more prominent with decrease in gate length and diminishes with increase in gate length of JLFET.
- We incorporated a raised cosine function relating Gate Length of JLFET (L_G)to the Random Factor (η).
- Randomness of the Random Factor(η) depends on the raised cosine function value for a particular Gate Length (L_G) and roll-off factor (β).
- Random Factor(η) is governed by a Uniform Distribution with Lower Limit $\left(\left\lceil\frac{L_S}{a_0}\right\rceil + 1 - k'\right)$ and Upper Limit $\left(\left\lceil\frac{L_S+L_G}{a_0}\right\rceil - \left\lceil\frac{L_S}{a_0}\right\rceil - k'\right)$.But we need to incorporate dependence of ηonL_G; so the Lower Limit and Upper Limit get modified as$\left(\left\lceil\frac{L_S}{a_0}\right\rceil + 1 - k'\right)H(L_G)$ and $\left(\left\lceil\frac{L_S+L_G}{a_0}\right\rceil - \left\lceil\frac{L_S}{a_0}\right\rceil - k'\right)H(L_G)$ respectively, where $H(L_G)$ is raised cosine function such as :

$$H(L_G) = \begin{cases} 1\,, L_G \leq (1-\beta)L_C \\ \frac{1}{2}\left(1 + \cos\left(\frac{\pi}{2\beta L_C}(L_G - (1-\beta)L_C)\right)\right), (1-\beta)L_C < L_G < (1+\beta)L_C \\ 0\,, L_G \geq (1+\beta)L_C \end{cases}$$

where $L_C$is Critical Gate Length for onset of RDF and$\beta$is roll-off factor.

- For a particular roll-off factor, Lower the Gate Length,higher is the value of $H(L_G)$ and thus the Uniform Distribution for generating that Random Factor (η) has a wider difference between Upper and Lower Limits implying increased randomness. On the contrary, Higher the Gate Length smaller is the value of $H(L_G)$, narrower the difference between Upper and Lower Limits of Uniform Distribution that eventually decreases the randomness.

- Randomness of Random Factor (η) is maximum for $H(L_G) = 1$ and minimum for $H(L_G) = 0$.

7.3 Results And Discussion

In our proposed model, we have taken 500 trials of measurement of V_{TH} and introduced randomization of our random factor for each trail to account for RDF, and observed fluctuation of threshold voltage in every trial run.Results are presented inFigs. 7.1 to 7.6 .

We have used different gate lengths of JLFET and observed impact of RDF in V_{TH} for each gate length.We could see V_{TH} is facing fluctuations due to RDF in every specified gate length except one , but fluctuations are critical in 5nm and 20 nm Gate Lengths. In case of 5nm gate length, V_{TH} has only two states due to single dopant atom in bulk channel, whereas 20nm gate length has higher states of V_{TH} . In 25nm Gate Length , RDF effect is found to be absent and there is no fluctuation in resulting V_{TH}., which is essentially the same as V_{TH}obtained earlier without RDF. Critical Gate Length (L_C) in our model is taken as 15nm.

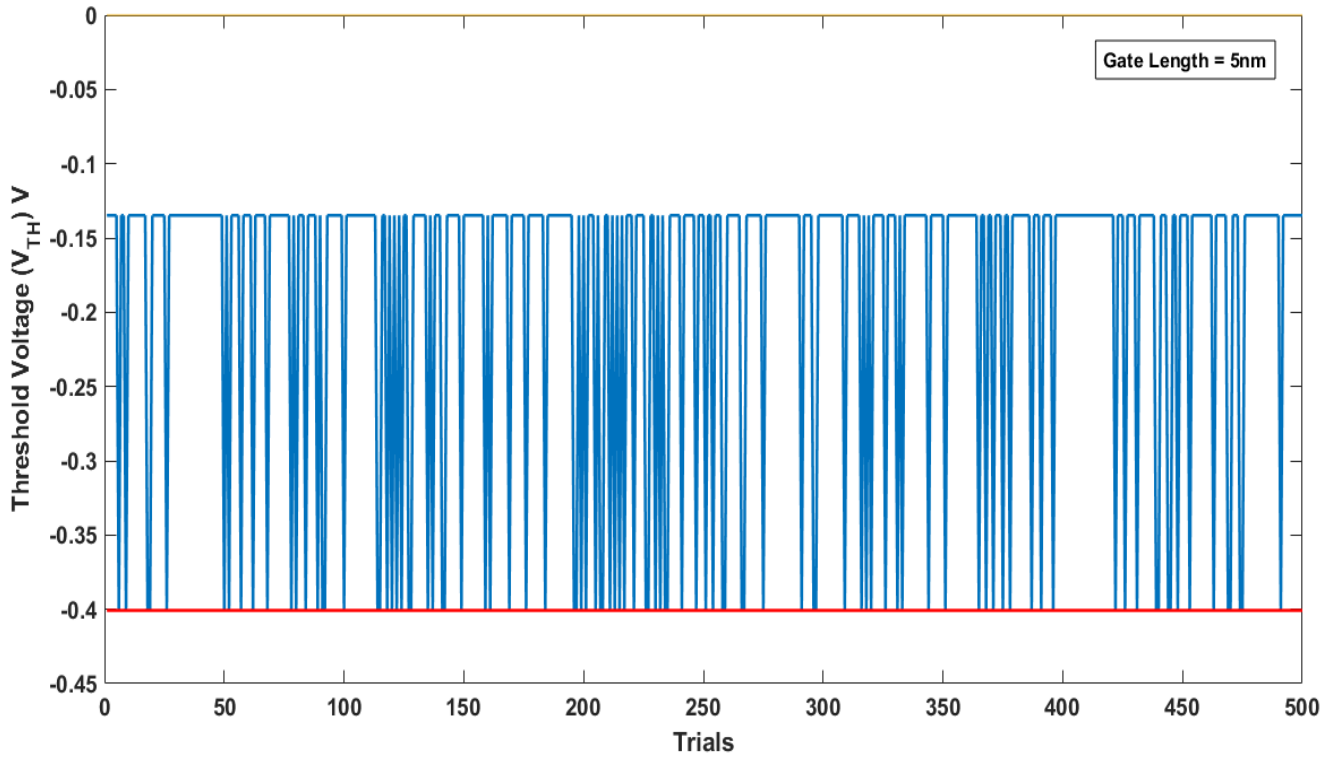

Fig.7.1:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 5nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

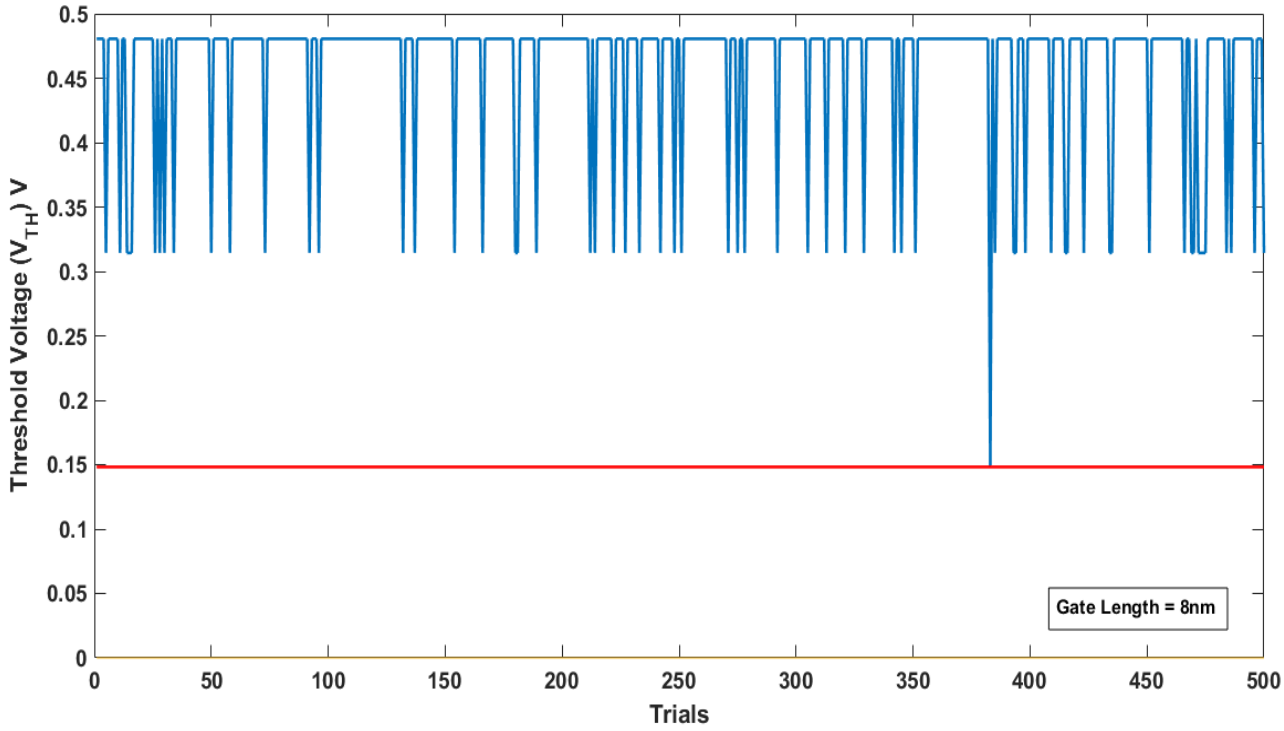

Fig.7.2:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 8nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

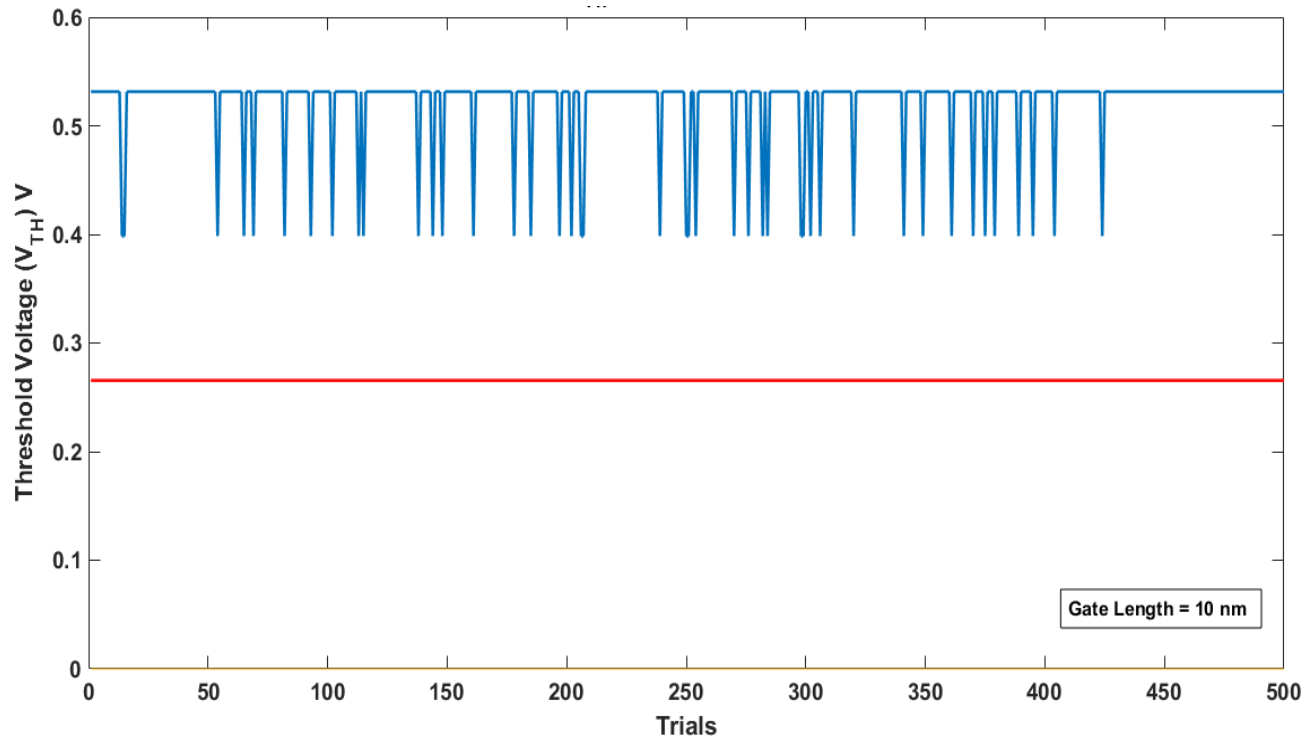

Fig.7.3:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 10nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

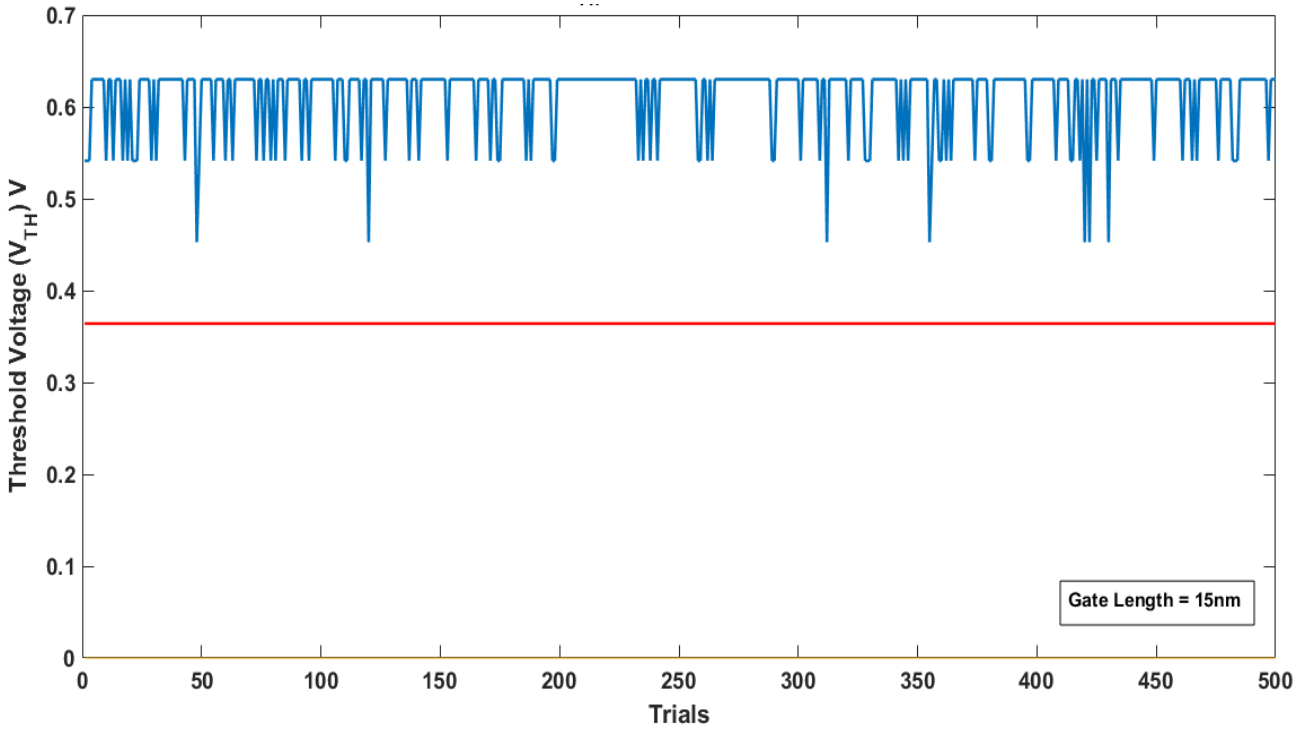

Fig.7.4:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 15nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

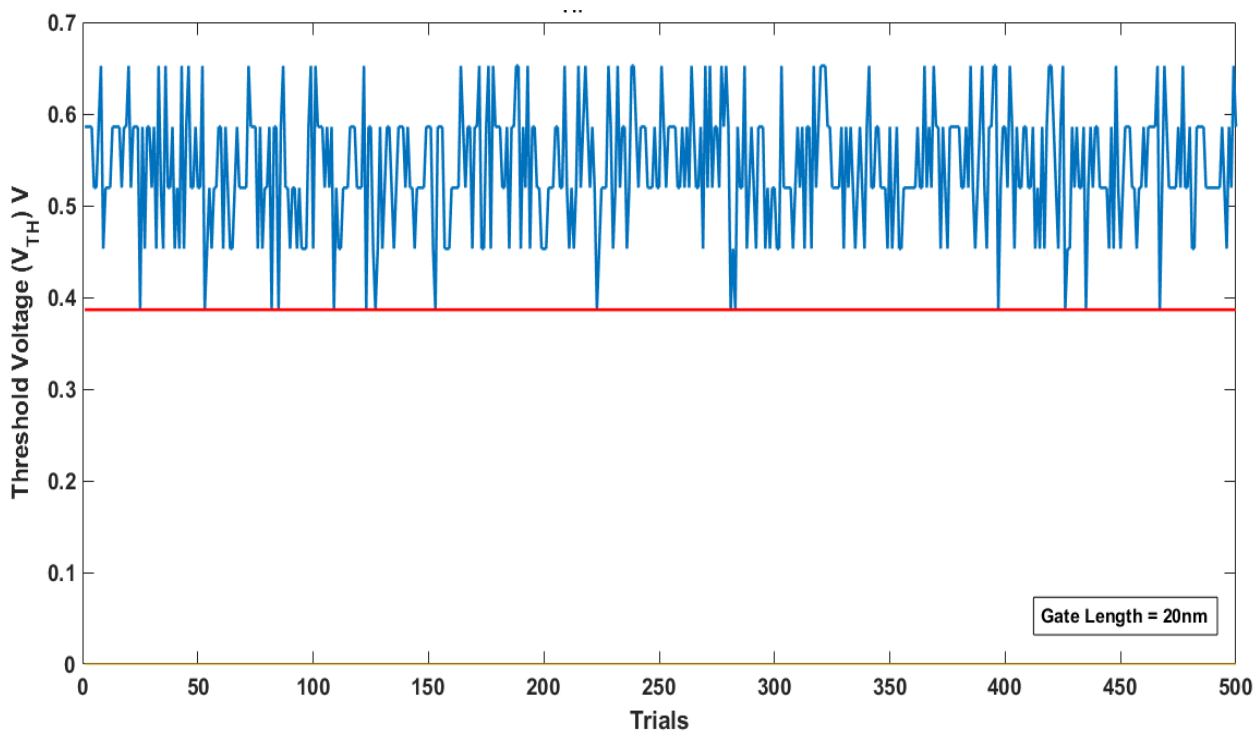

Fig.7.5:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 20nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

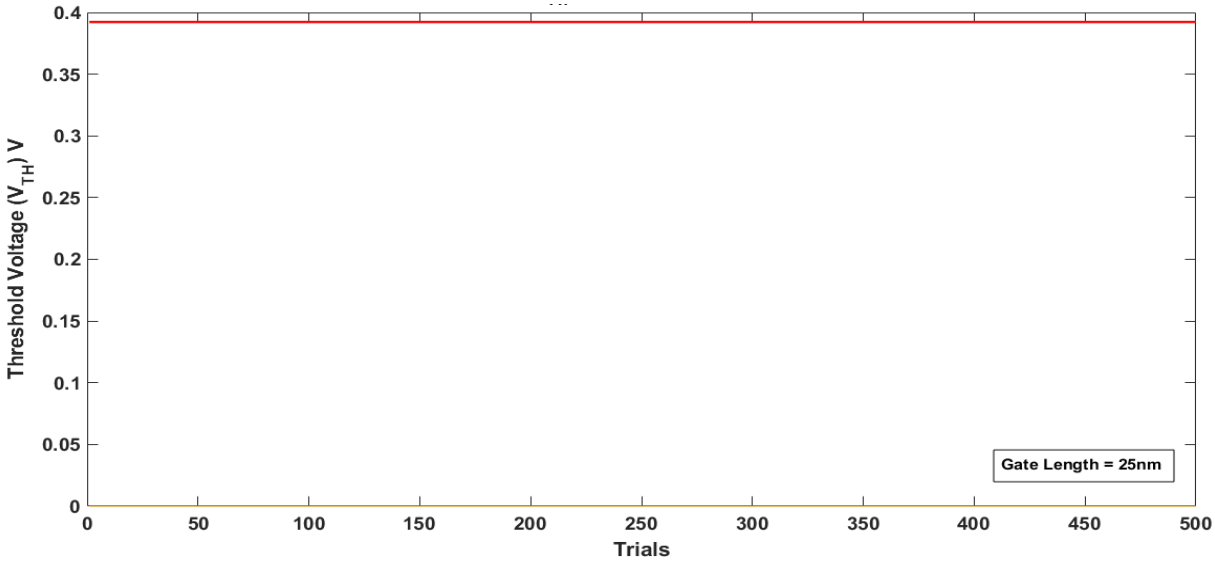

Fig.7.6:500 trials of measurement of Threshold Voltage and its fluctuations due to RDF in 25nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

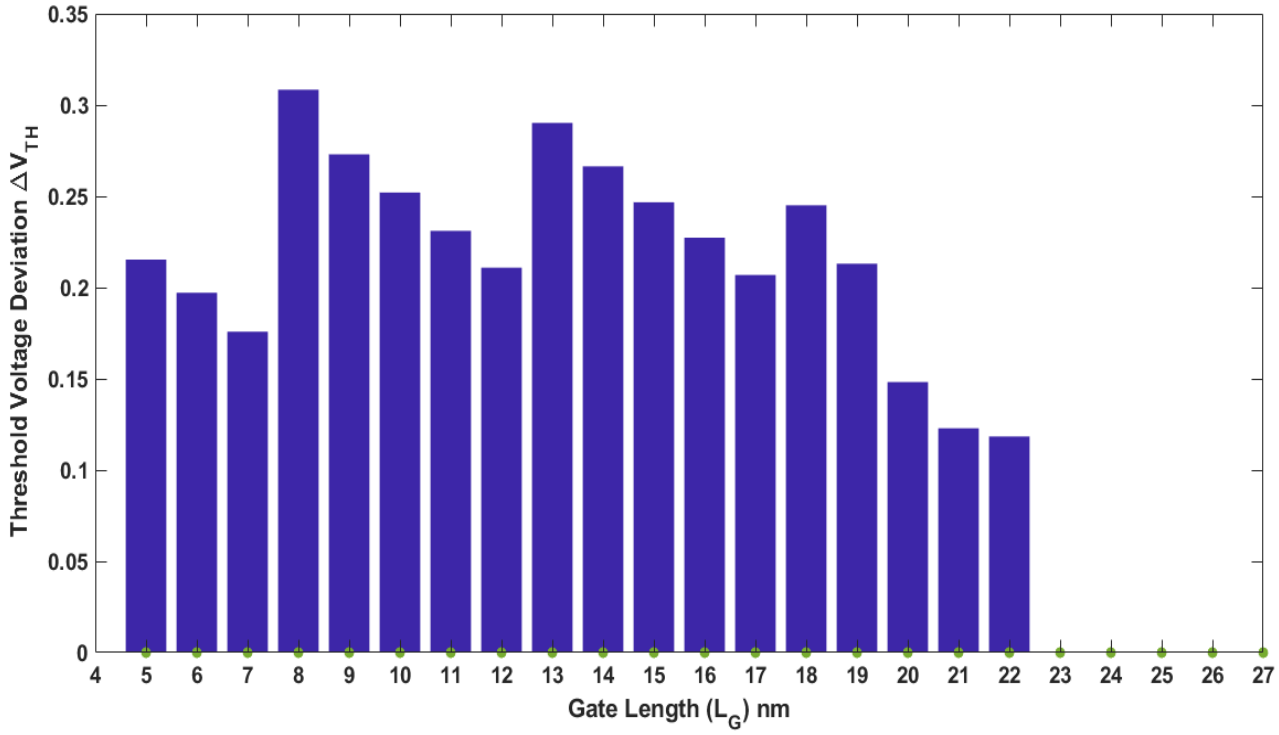

Fig.7.7:Deviation of V_{TH}under RDFfor different L_G in JLFET

For each gate length spanning from 5nm to 27nm,we have taken 500 trials of measurement of V_{TH} under RDF effects. We have taken mean of 500 samples for each gate length and compared with the mean of the same samples without RDF, and plotted their difference in

Fig.7.7.The figure indicates that Threshold Voltage deviation vanishes as the gate length increases above 22nm.

7.3 Conclusion

In this chapter, we introduced RDF effects in our proposed model and performed Model Simulation. We used Raised Cosine function to incorporate gate length variation with RDF and accordingly adjusted randomness of Random Factor to account for RDF . We observed fluctuations in V_{TH} due to RDF for gate lengths spanning from 5nm to 22nm with critical fluctuations in 5nm and 20nm gate lengths. We inferred that V_{TH}fluctuations depend on thegate lengths as well as number of dopant atoms present in the central line channel region and associated roll off factor of Raised Cosine function accounting for RDF.

Chapter 8

Analysis of Random Dopant Fluctuations and its impact on Threshold Voltage of JLFET under Quantum Confinement

In the previous chapter we have observed impact of RDF in classical threshold voltage of short channel JLFET.

Now we would be introducing quantum confinement effects and observe how V_{TH} gets affected under both the Quantum confinement and RDF effects .

8.1 Inclusion of RDF and Quantum Confinement Effects in new Model

To get the threshold voltage of JLFET in presence of both the above effects, we start with

Equation (6.40)

$$V_{TH}^{CL+QM} = \frac{(8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8V_{bi}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1+4\beta_2\beta_3)(4V_{bi}(\beta_1\beta_3+\beta_2\beta_1 + V_{bi}\beta_2\beta_3)+\beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3+2}$$

$$+ V_{FB} - \frac{\rho' t_{Si}}{2C_{ox}} - \frac{\rho' t_{Si}^2}{8\epsilon_{Si}} + \frac{k_B T}{q}\left(\ln(3) - \ln\left(\frac{e^{-\frac{\xi}{2\sqrt{m_l}}}}{1-e^{-\frac{\xi}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi}{2\sqrt{m_t}}}}{1-e^{-\frac{\xi}{\sqrt{m_t}}}}\right)\right)$$

$$where\ \xi = \frac{\hbar}{k_B T}\sqrt{\frac{q^2 N_D}{\epsilon_{Si}}}$$

where, ξ can also be written as $\xi' = \frac{\hbar}{k_B T}\sqrt{\frac{q\rho'}{\epsilon_{Si}}}$.

Equation (6.40) can further be written as:

$$V_{TH}^{CL+QM}$$

$$= \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2}$$

$$+ V_{FB} - \frac{\rho' t_{Si}}{2C_{ox}} - \frac{\rho' t_{Si}^2}{8\epsilon_{Si}} + \frac{k_B T}{q}\left(\ln(3) - \ln\left(\frac{e^{-\frac{\xi'}{2\sqrt{m_l}}}}{1 - e^{-\frac{\xi'}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi'}{2\sqrt{m_t}}}}{1 - e^{-\frac{\xi'}{\sqrt{m_t}}}}\right)\right)$$

$$where\ \xi' = \frac{\hbar}{k_B T}\sqrt{\frac{q\rho'}{\epsilon_{Si}}} \qquad (8.1)$$

Now to introduce RDF ,we would use Equation (7.3) into (8.1), such as

$$V_{TH\_RDF}^{CL+QM}$$

$$= \frac{(8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3) - \left((8\mathrm{V_{bi}}\beta_2\beta_3 + 4\beta_1\beta_2 + 4\beta_1\beta_3)^2 - 4(1 + 4\beta_2\beta_3)(4\mathrm{V_{bi}}(\beta_1\beta_3 + \beta_2\beta_1 + \mathrm{V_{bi}}\beta_2\beta_3) + \beta_1^2)\right)^{\frac{1}{2}}}{8\beta_2\beta_3 + 2}$$

$$+ V_{FB} - \frac{\rho'_{RDF} t_{Si}}{2C_{ox}} - \frac{\rho'_{RDF} t_{Si}^2}{8\epsilon_{Si}} + \frac{k_B T}{q}\left(\ln(3) - \ln\left(\frac{e^{-\frac{\xi'_{RDF}}{2\sqrt{m_l}}}}{1 - e^{-\frac{\xi'_{RDF}}{\sqrt{m_l}}}} + 2\frac{e^{-\frac{\xi'_{RDF}}{2\sqrt{m_t}}}}{1 - e^{-\frac{\xi'_{RDF}}{\sqrt{m_t}}}}\right)\right)$$

$$where\ \xi'_{RDF} = \frac{\hbar}{k_B T}\sqrt{\frac{q\rho'_{RDF}}{\epsilon_{Si}}} \qquad (8.2)$$

Thus, we have formulated a complete model for threshold voltage of Quantum Confined JLET taking the RDF into account, and Equation (8.2) can be used to find the desired voltage for further simulation.

8.2Results and Discussion

Using Eq. 8.2 and the device parameters mentioned in Table 3.1 , we would be repeating the same stepsas described in Chapter 6 for investigating fluctuations of V_{TH} under RDF and Quantum Confinement Effects.

Simulation results have been presented in Figs.8.1 to 8.6. From figures, we could see V_{TH} under RDF and Quantum Confinement is facing more fluctuations compared to that only under RDF effects for every specified gate length except one, but fluctuations are very critical in 5nm and 20 nm Gate Lengths. In 5nm gate length, V_{TH} has only two states due to single dopant atom in the bulk channel, whereas 20nm gate length causes higher states of V_{TH} with high-valued peaks. In 25nm Gate Length , RDF effect is absent and so no fluctuation in V_{TH} (under Quantum Confinement) is observed. Critical Gate Length (L_C) in our model is taken to be 15nm.

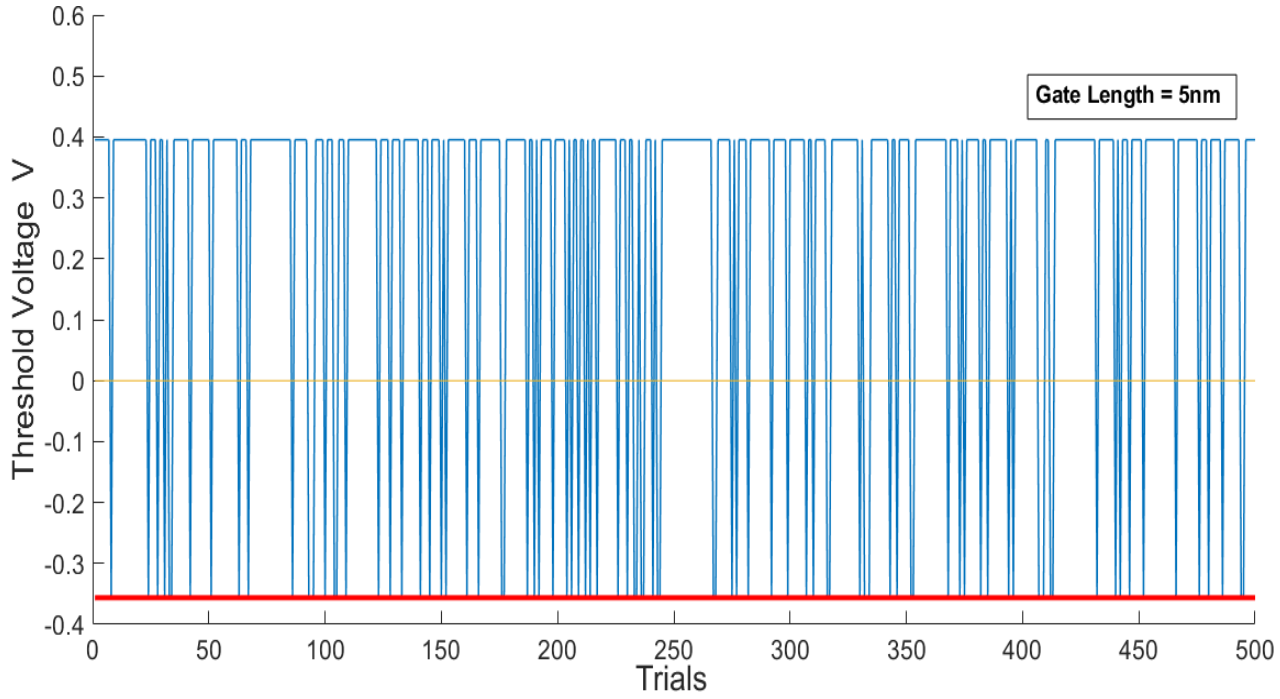

Fig.8.1:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in JLFET of 5nm Channel Length (blue and red line represent V_{TH} with and without RDF respectively)

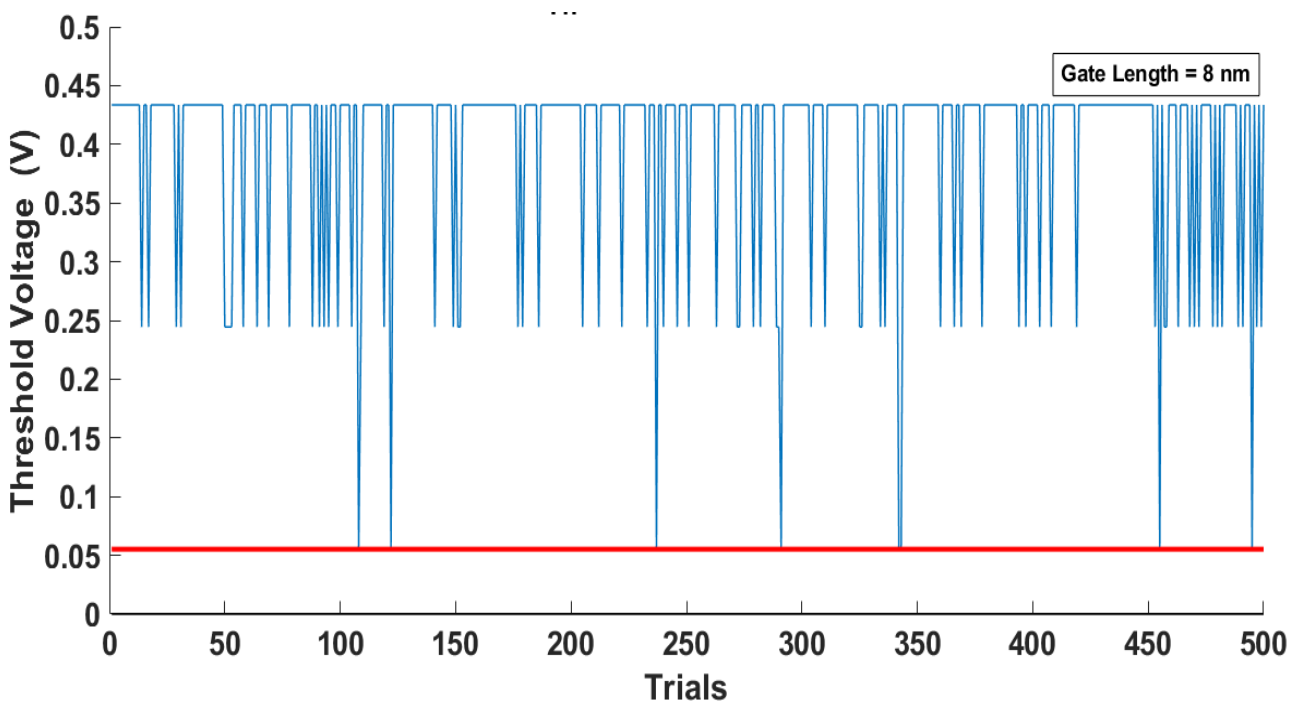

Fig.8.2:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in 8nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

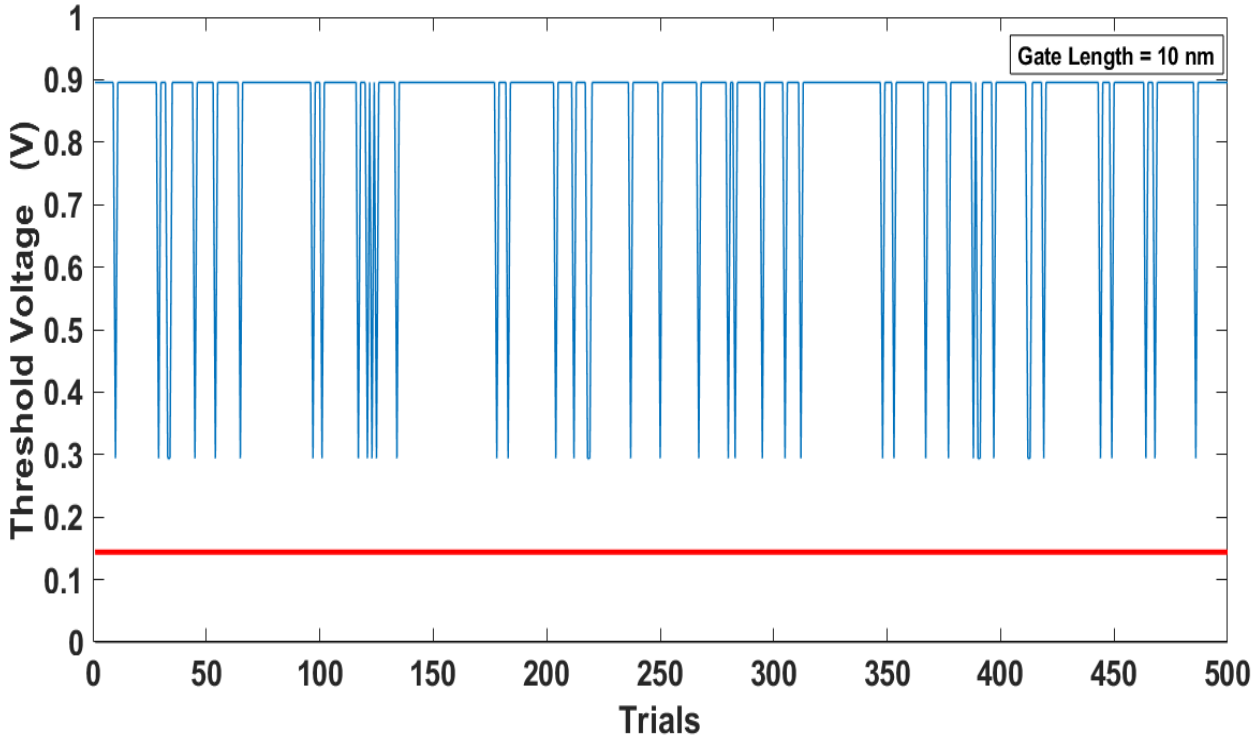

Fig.8.3:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in 10nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

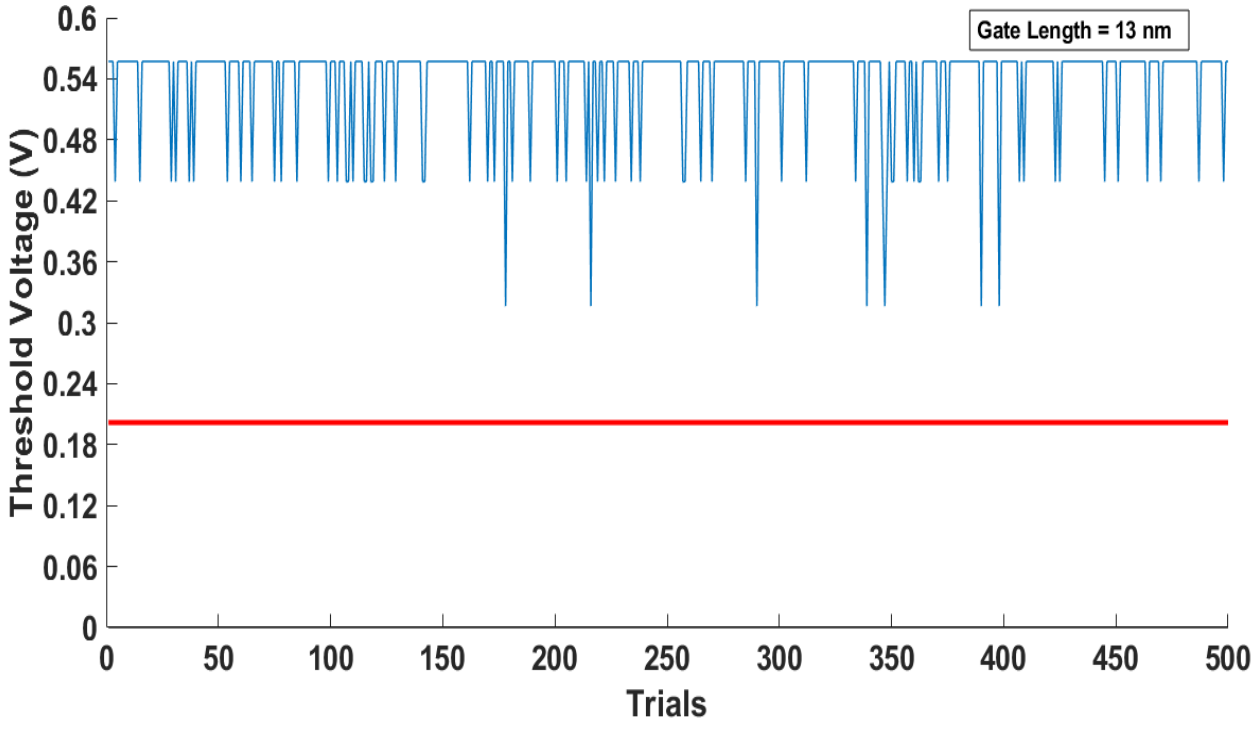

Fig.8.4:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in 13nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

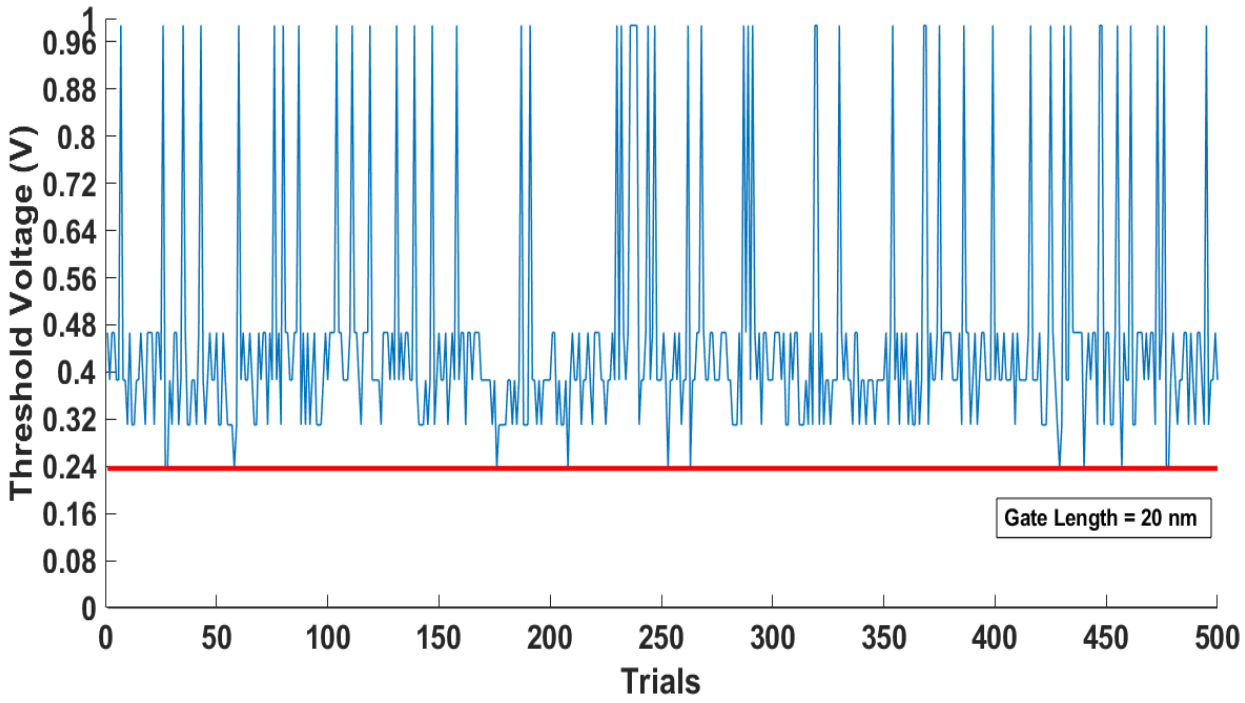

Fig.8.5:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in 20nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

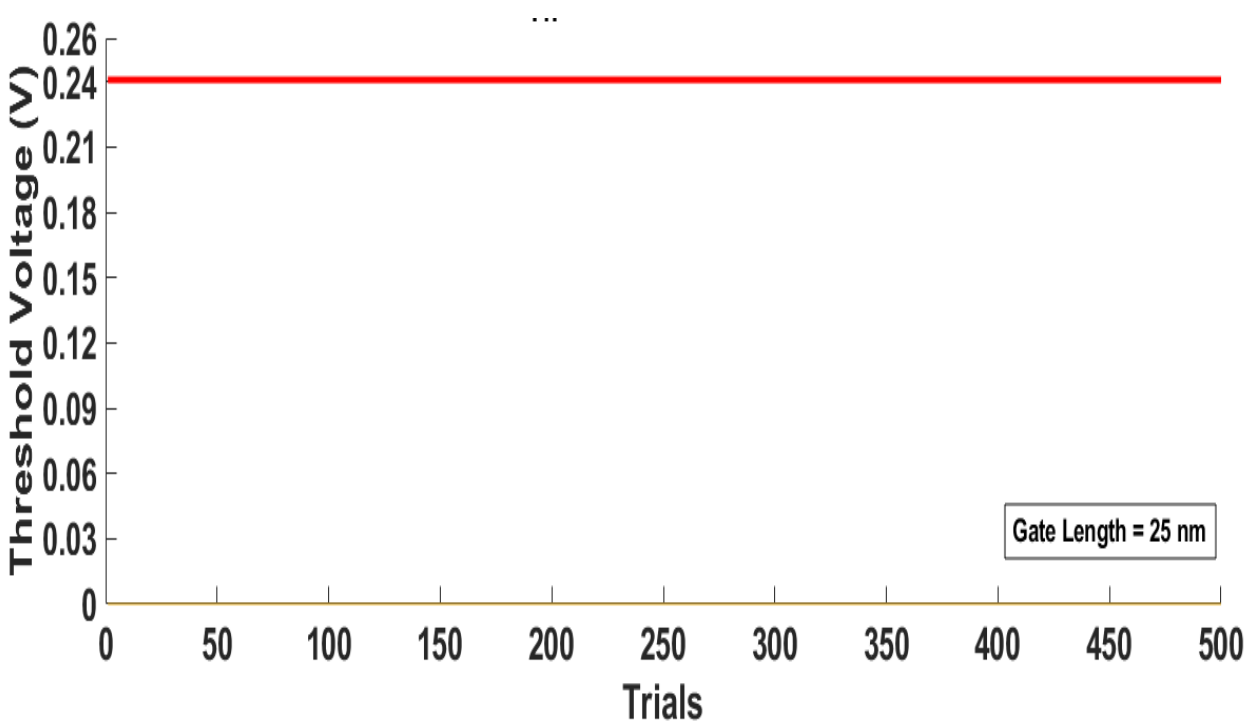

Fig.8.6:500 trials of measurement of Threshold Voltage under Quantum Confinement and its fluctuations due to RDF in 25nm Channel Length JLFET (blue and red line represent V_{TH} with and without RDF respectively)

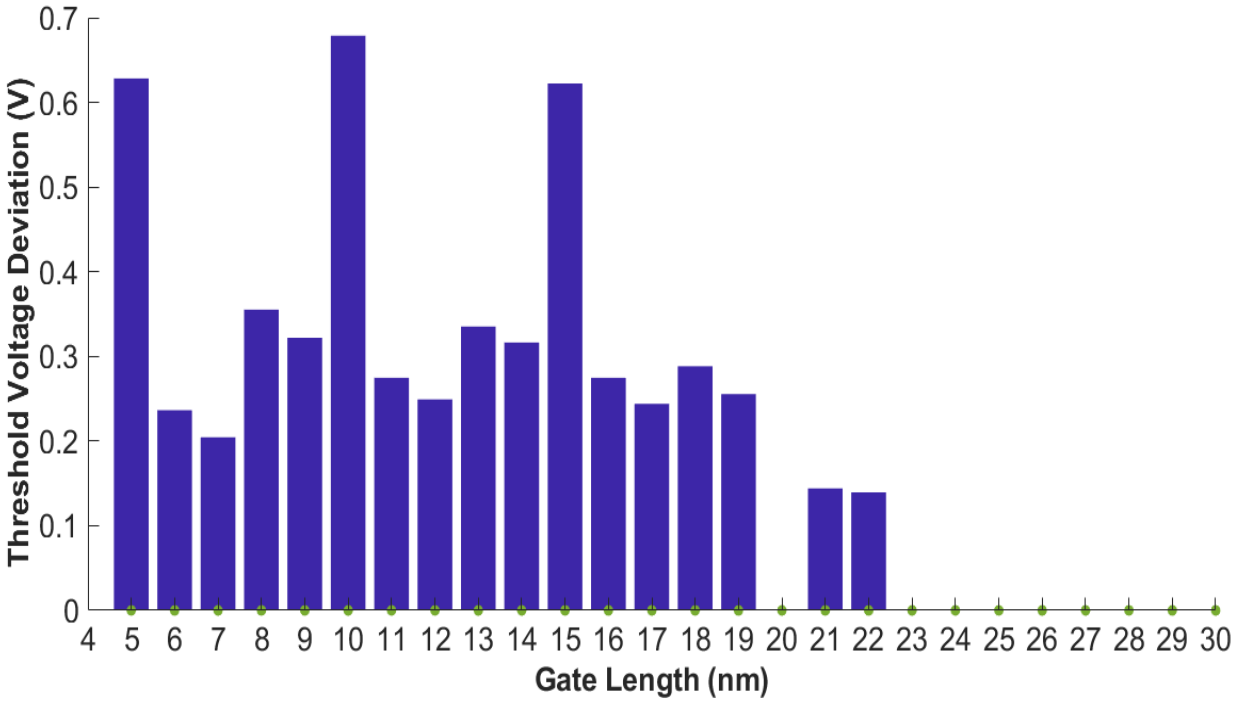

Fig.8.7: Deviation of V_{TH} under Quantum Confinement and RDF for different L_G in JLFET

For each gate length spanning from 5nm to 30 nm,we have taken 500 trials of measurement of V_{TH} under Quantum Confinement and RDF effects. We considered the mean of 500 samples for each gate length and compared it with the mean of same samples without RDF, and plotted their difference in Fig.8.7.Here we can see Threshold Voltage Deviation starts to diminishas gate length increases above 19nm; the deviation is highest for 10nm and smallest for 22 nm gate length.

8.3 Conclusion

In this chapter we included both RDF and Quantum Confinement effects in our model and formulated threshold voltage of JLFET. Fluctuations observed in V_{TH} due to RDF under Quantum Confined JLFET are more critical with higher peaks (both positive and negative) compared to those under classical JLFET. Threshold Voltage deviation due to RDF for different gate lengths is also higher in Quantum Confined JLFET compared to classical JLFET, but deviation of samples from the maximum value is higher in Fig. 7.7 than Fig. 8.7.It is seen from Fig. 8.7 that most of the samples tend to settle down to minimum threshold deviation value, where the scenario is opposite in Fig. 7.7, implying that Quantum Confinement effects tend to stabilize threshold voltage deviations due to RDF.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

In this thesis, we have proposed a model for threshold voltage of short channel DG SMG JLFET with inclusion of the effects of Quantum Confinement and Random Dopant Fluctuation (RDF). We introduced the concept of lattice site occupancy of dopant atoms and its impact on the threshold voltage for better understanding of the phenomenon of RDF. MATLAB Simulations of our model have been performed to observe fluctuations of threshold voltage in Quantum Confined JLFET under RDF . Silvaco TCAD Atlas has been used to perform device simulation of JLFET to comprehend the device physics as well as to make a comparison with our model in terms of variation in threshold voltage with various physical parameters. For inclusion of Quantum Confinement Effects in Silvaco, we used Bohm Quantum Potential Model to get accurate results and make precise comparison with our analytical model. Plausible explanations for deviation, if any, of analytical results from the simulation results have also been provided.

Threshold Voltages obtained from our model match with the simulated valueswhen Quantum Confinement effects are considered in both MATLAB model and simulation model. Despite of using appropriate models for inclusion of Quantum Confinement effects in simulation, the influence of carrier confinement appears to be less prominent (shallow quantum parabolic well) on the resulting threshold voltages compared to those obtained from theoretical model. As a consequence, threshold voltages obtained from simulation tend to have optimistic values, whereas those from the proposed model tend to have rather depressed negative values. In Simulation model, the gradual transition of Quantum Confinement effects from being more prominent to less prominent occur with change in the physical parameters of the device, whilethat is absent in our MATLAB model.

Fluctuations observed in threshold voltage of our model due to RDF is more frequent with greater peaks in Quantum Confinement JLFET compared to classical JLFET, as it should be. In both cases, gate length of 5nm and 20nm yield maximum fluctuations. In JLFET with gate length greater than 25 nm, the RDF effect becomes insignificant. We used Raised Cosine Function to incorporate dependence of RDF on the gate length of JLFET. Critical gate length of 15nm has been used in our model for investigation of RDF.

9.2 Future Work

Simulating JLFET with distinct Quantum Confinement effects using proper physical parameters needs to be carried out in future for more precise comparison with our model. Our model has employed only 1D linear lattice array spanning across the central line potential for determining the threshold voltage. But such 1D array has its inherent limitation as uniformity among dopant atoms in terms of lattice site occupancy across the central line channel is not always feasible for any donor concentration. To ensure such uniformity, lattice array also across the width of the channel, i.e. a 2D lattice array should be considered. Inclusion of other parameters of crystal lattice in our model will make it more accurate and informative. Dependence of Quantum Confinement effects on physical parametersof JLFET (with more sensitivity) needs to be incorporated in our model so that accurate variation in threshold voltage for stronger or weaker QM effects could be presented.

As our proposed model for threshold voltage formulation of JLFET is based on intrinsic physical properties of crystal lattice,one maywell apply our model, with appropriate modifications, to other MESFET (Metal Semiconductor FET) and MISFET (Metal Insulator Semiconductor FET) devices for studying carrier confinement and RDF effects, and their influences on threshold voltage.

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