DESIGN OF A LOW-POWER ASYNCHRONOUS 10-BIT SAR ADC IN 65 nm TECHNOLOGY

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CERTIFICATE OF RECOMMENDATION

This is to certify that the thesis entitled "**DESIGN OF A LOW-POWER ASYNCHRONOUS 10-BIT SAR ADC IN 65 nm TECHNOLOGY**" has been carried out by **SHIBMALYA SEN (University Registration No: 154114 of 2020-2021**) under my guidance and supervision and be accepted in partial fulfilment of the requirement for awarding the degree of "**MASTERS OF TECHNOLOGY IN VLSI AND MICROELECTRONICS**". The research results presented in this thesis have not been included in any other paper submitted for the award of any degree to any other Institute or University.

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I hereby declare that this thesis contains literature survey and original research work done by the undersigned candidate, as a part of his degree of "**MASTER OF TECHNOLOGY IN VLSI AND MICROELECTRONICS**". All information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that as required by these rules and conduct, I have fully cited and referenced all materials and results that are not original to this work.

Thesis Title

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(SHIBMALYA SEN)

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ABSTRACT

Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is one of the most popular and widely used ADC architectures due to its high speed, low power, and reasonable resolution capabilities. SAR ADC has gained a lot of interest in recent years because of its suitability for portable and low-power devices. The SAR ADC works by comparing the input voltage to a series of reference voltages generated by a digital-to-analog converter (DAC), and then using a binary search algorithm to determine the closest match. The resolution of the SAR ADC depends on the number of bits in the digital output, and higher resolutions can be achieved by increasing the number of bits. However, increasing the number of bits results in longer conversion times and higher power consumption. Therefore, there is a trade-off between resolution, speed, and power consumption in SAR ADC design. This thesis focuses on the design and optimization of SAR ADCs, including various circuit topologies, techniques, and architectures to achieve high performance, low power, and high resolution. The research also explores the impact of various process, voltage, and temperature (PVT) variations on the performance of SAR ADCs and proposes techniques to mitigate these effects. Finally, the proposed SAR ADCs are compared with existing state-of-the-art ADCs, and their performances are evaluated in terms of power consumption, speed, and resolution.

In recent years, there has been a growing need for Successive Approximation Register (SAR) Analog-to-Digital Converter in medical application such as pacemaker or neuromorphic applications. Accordingly, the demand for long battery life-time poses the requirement for designing ultra-low power SAR ADCs.

Presents work investigates an asynchronous 1.1V 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) implemented in 65nm CMOS technology. The asynchronous SAR ADC system consists of an internal clock generator, sample and hold switches, capacitive digital-to-analogue converter (DAC), dynamic comparator, and SAR logic. Running a 64-point FFT on the output of the SAR ADC with a 1.2 V differential input signal results in a maximum ENOB of 9.38 bits at 20 MHz sample rate, an SNR of 56.56 dB and aof total power consumption of 676 uW. This SAR ADC system can be used in systems where low power consumption, moderate resolution and moderate speed are mainly required, such as computer memory cores for artificial intelligence applications and sensors for applications, Biomedical and neuromorphic chips.

ABBREVIATIONS

ADC	Analog to Digital Converter
BWC	Binary-Weighted Capacitor
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
DFF	Delay type Flip Flop
DL	Delay Line
DR	Dynamic Range
ENOB	Effective Number of Bits
FOM	Figure of Merit
FFT	Fast Fourier Transform
HD	Harmonic Distortion
INL	Integral Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
SAR	Successive Approximation Register
SINAD	Signal to Noise and Distortion Ratio
SFDR	Spurious-Free Dynamic Range
SNR	Signal to Noise Ratio
SHC	Sample and Hold Circuit
TWC	Two-Stage Weighted Capacitor

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Chapter 1

Introduction

1.1 Overview

The increasing demand for solutions in disease diagnosis and treatment has led to a growing need for advancements in medical and healthcare systems. Biomedical applications, such as medical implants and wireless sensors, have emerged as critical tools for long-term patient monitoring without imposing significant limitations [1–4]. Figure 1 illustrates the architecture of a wireless body sensor network (WBSN) [5]. This network comprises wireless sensors strategically placed inside, or around the human body to monitor vital body parameters and movements. The collected biomedical data from these nodes needs to be wirelessly transmitted to a base station. Hence, the analog-to-digital converter (ADC) plays a crucial role in converting analog biomedical signals into a digital format suitable for storage and processing. Given that these nodes operate on portable battery-powered devices, there is a need for energy-efficient integrated circuit designs. It is evident that minimizing power consumption is a critical challenge in wireless biomedical applications due to limited battery life [6]. The ADC serves as a fundamental component by acting as an interface between the analog domain and digital processing domain.

1.2 Types of ADCs

There are several ADC architectures available in the market that serve different purposes and have their own advantages and disadvantages. Some of the commonly used ADC architectures are Delta-Sigma, Flash, Pipeline, and Dual-Slope ADCs. Here's a comparison of SAR ADC with other ADC architectures:

1. Delta-Sigma ADC: Delta-Sigma ADCs are known for their high resolution capabilities and low noise, making them ideal for high-precision applications. However, they have a slow conversion rate and require more power than SAR ADCs. In contrast, SAR ADCs have a higher conversion rate, consume less power, and have a simpler architecture, but may not provide the same level of resolution and noise performance as Delta-Sigma ADCs.

2. Flash ADC: Flash ADCs have a fast conversion rate, but they require a large number of comparators, which can increase the power consumption and cost of the system. Flash ADCs also have limited resolution capabilities and can only achieve resolutions up to 8 bits, while SAR ADCs can achieve resolutions up to 16 bits.

3. Pipeline ADC: Pipeline ADCs are known for their high speed and high-resolution capabilities, but they require more power than SAR ADCs. Pipeline ADCs also have a more complex architecture, making them harder to design and implement.

4. Dual-Slope ADC: Dual-Slope ADCs are known for their high accuracy and low cost, but they have a slow conversion rate and are sensitive to noise and temperature

variations. SAR ADCs have a higher conversion rate, consume less power, and have a simpler architecture, but may not provide the same level of accuracy as Dual-Slope ADCs.

Overall, each ADC architecture has its own set of advantages and disadvantages, and the choice of ADC architecture depends on the specific requirements of the application. SAR ADCs are a popular choice due to their high speed, low power consumption, reasonable resolution capabilities, and simple architecture, making them ideal for portable and low-power devices where power consumption is a critical concern.

1.3 Comparison between SAR ADC and other ADC architectures

SAR ADC is often considered the best choice for many applications:

1. Delta-Sigma ADC: Delta-Sigma ADCs offer high resolution and low noise, making them ideal for high-precision applications. However, they require a complex architecture, have a slower conversion rate, and consume more power than SAR ADCs. Delta-Sigma ADCs are often used in applications where high accuracy is required, such as medical equipment and instrumentation. In contrast, SAR ADCs offer a faster conversion rate, consume less power, and have a simpler architecture, making them a better choice for applications that require lower resolution and faster sampling rates.
2. Flash ADC: Flash ADCs offer fast conversion rates but require a large number of comparators, which can increase power consumption and cost. Flash ADCs are often used in applications that require low resolution and fast sampling rates, such as video and audio processing. In contrast, SAR ADCs offer a higher resolution, consume less power, and have a simpler architecture, making them a better choice for applications that require higher resolution and lower power consumption.
3. Pipeline ADC: Pipeline ADCs offer high resolution and high speed, but require more power and have a more complex architecture than SAR ADCs. Pipeline ADCs are often used in applications that require high resolution and high-speed sampling rates, such as imaging and wireless communication. In contrast, SAR ADCs offer a simpler architecture, consume less power, and provide reasonable resolution capabilities, making them a better choice for applications that require a balance between resolution and power consumption.
4. Dual-Slope ADC: Dual-Slope ADCs offer high accuracy and low cost but have a slow conversion rate and are sensitive to noise and temperature variations. Dual-Slope ADCs are often used in applications that require high accuracy but can tolerate slower sampling rates, such as temperature sensing and industrial process control. In contrast, SAR ADCs offer a faster conversion rate, consume less power, and have a simpler architecture, making them a better choice for applications that require a balance between speed, resolution, and power consumption.

1.4 Application of SAR ADC in Neuromorphic Chips

SAR (Successive Approximation Register) ADCs (Analog-to-Digital Converters) are widely used in neuromorphic vision chips due to their high precision and low power consumption. Neuromorphic vision chips are designed to mimic the structure and function of the human visual system, and require high-speed and high-resolution ADCs to convert analog signals from photoreceptors into digital signals for processing.

One of the main challenges in designing neuromorphic vision chips is achieving high resolution while maintaining low power consumption. SAR ADCs are well-suited for this task, as they are able to achieve resolutions of up to 24 bits while consuming very little power.

SAR ADCs are also able to operate at high speeds, which is important in neuromorphic vision chips where real-time processing is required. The fast conversion time of SAR ADCs enables them to capture and process visual information at a high rate, allowing the chip to respond quickly to changes in the environment.

Another advantage of SAR ADCs is their ability to perform accurate and precise conversions even in the presence of noise. Neuromorphic vision chips often operate in noisy environments, and SAR ADCs are able to filter out unwanted noise and provide accurate digital representations of the visual signal.

SAR ADCs are commonly used in neuromorphic vision chips to convert the output of photoreceptors into digital signals that can be processed by the neural network. The high precision and low power consumption of SAR ADCs make them an ideal choice for this application.

In addition to photoreceptor conversion, SAR ADCs are also used in neuromorphic vision chips to convert the output of the neural network back into analog signals for control of actuators such as motors and servos.

In summary, SAR ADCs are an important component of neuromorphic vision chips due to their ability to achieve high resolution and operate at high speeds while consuming very little power. Their ability to filter out noise and provide accurate digital representations of the visual signal make them an ideal choice for use in these types of systems.

1.5 Event Based SAR ADC

Event-based SAR (Successive Approximation Register) ADCs (Analog-to-Digital Converters) are a type of ADC that have been developed specifically for use in event-based neuromorphic systems. Event-based neuromorphic systems are designed to mimic the function of the brain, which processes information in an asynchronous, event-driven manner.

Traditional ADCs sample the input signal at a fixed rate and convert the signal into a series of digital values. However, in event-based systems, this approach is not practical, as the input signal may contain long periods of inactivity, which wastes power and reduces the efficiency of the system.

Event-based SAR ADCs overcome this issue by only sampling the input signal when a significant change in the signal is detected. This is achieved using an event-based architecture, where the ADC only operates when an event occurs, and the output of the ADC is generated in response to that event.

Event-based SAR ADCs operate by monitoring the input signal for changes and generating a digital output only when a significant change is detected. The ADC only consumes power when a change occurs, which reduces the overall power consumption of the system.

The output of the ADC is generated using a successive approximation register, which performs a binary search to determine the digital value that best represents the input signal. The SAR ADC can achieve high precision even with a low sampling rate, which further reduces the power consumption of the system.

Event-based SAR ADCs are commonly used in neuromorphic vision and audio systems, where the input signal is highly dynamic and asynchronous. In these systems, the ADC can sample the input signal only when a significant change occurs, which reduces the power consumption of the system and allows it to operate more efficiently.

In summary, event-based SAR ADCs are a type of ADC that have been developed specifically for use in event-based neuromorphic systems. Their event-driven architecture and low power consumption make them well-suited for use in vision and audio systems, where the input signal is highly dynamic and asynchronous.

Chapter 2

Literature Review

2.1 Chapter Overview

In recent years, there has been a growing interest in the successive approximation register (SAR) ADC, particularly for its application in biomedical fields [13]. This chapter aims to review and analyze various techniques proposed for low-power SAR ADCs in the past five years, focusing on their suitability for biomedical applications. The goal is to provide researchers in the field of energy-efficient SAR ADC design with a comprehensive understanding of the key components and different implementation schemes.

This survey offers the following contributions:

i. A comprehensive examination of different single SAR ADC implementations, highlighting their respective advantages, disadvantages, and challenges associated with each component.

ii. Investigation of various optimization techniques employed to reduce power consumption in SAR ADCs, based on a thorough analysis of numerous publications from 2017 to 2022.

iii. Clear comparisons of different single SAR ADC techniques across various CMOS technologies, enabling researchers to make informed design choices.

iv. Detailed analysis and discussion of results based on key performance metrics such as power consumption, resolution, speed, and linearity. This information is presented through tables and figures for easy reference and comparison.

The subsequent sections are structured as follows: Section 2.2 provides an overview of the SAR ADC architecture, outlining its fundamental operation. Section 2.3 explores the various approaches to sample and hold switching, discussing their characteristics and trade-offs. Section 2.4 presents different configurations of the dynamic comparator, highlighting their strengths and limitations. The architectures of the capacitor digital-to-analog converter (CDAC) are discussed in Section 2.5, with a focus on their design considerations. Section 2.6 delves into the SAR register and its control logic, explaining their role in the conversion process. A summary of recent performance parameters for SAR ADCs is presented in Section 2.7, offering a comprehensive overview of the state-of-the-art in the field. Finally, concluding remarks are provided in Section 2.8, summarizing the key findings and potential future research directions.

2.2 Overview of SAR ADC Architecture

SAR ADC Architecture

In this section, we will provide a comprehensive overview of the architecture of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) and highlight its advantages compared to other types of ADCs. The basic implementation of a SAR ADC is illustrated in Figure 2, which depicts the key components involved in the conversion process.

These components include a Sample-and-Hold (S/H) switch, an internal Digital-to-Analog Converter (DAC), a comparator, and successive approximation logic.

The operation of a Successive Approximation Register Analog-to-Digital Converter (SAR ADC) commences by sampling the input signal through the Sample-and-Hold (S/H) switch. Subsequently, the digital code stored in a register is converted into an analog value by an internal Digital-to-Analog Converter (DAC). This analog value is then compared to the sampled signal voltage using a comparator, generating a digital output. The digital output guides the successive approximation logic to update the code stored in the register. Initially, the most significant bit (MSB) is presented in digital form and converted into an analog value for comparison with the input signal.

Throughout the conversion process, the comparator output determines the next bit to be determined. If the comparator output is high (1), indicating that the input signal voltage (Vin) is greater than half of the reference voltage (Vref/2), the MSB remains stored in the SAR register, and a high bit is loaded into the next bit position. Conversely, if Vref/2 < Vin, the comparator output will be low (0). This prompts the control circuit to write a low bit to the current bit position and a high bit to the next bit position. This iterative process continues, determining each bit from the MSB to the least significant bit (LSB), until all N required bits are determined.

The Figure 3 shows clock and timing of the SAR ADC, illustrating the two main phases of operation: the sampling process and the conversion process. During the conversion process, each bit is determined sequentially following the described procedure, resulting in the final digital representation of the input signal.

By understanding the architecture and operation of a SAR ADC, we gain insight into its advantages and suitability for various applications. The SAR ADC offers high resolution, excellent linearity, and low power consumption, making it a popular choice in many signal processing systems.

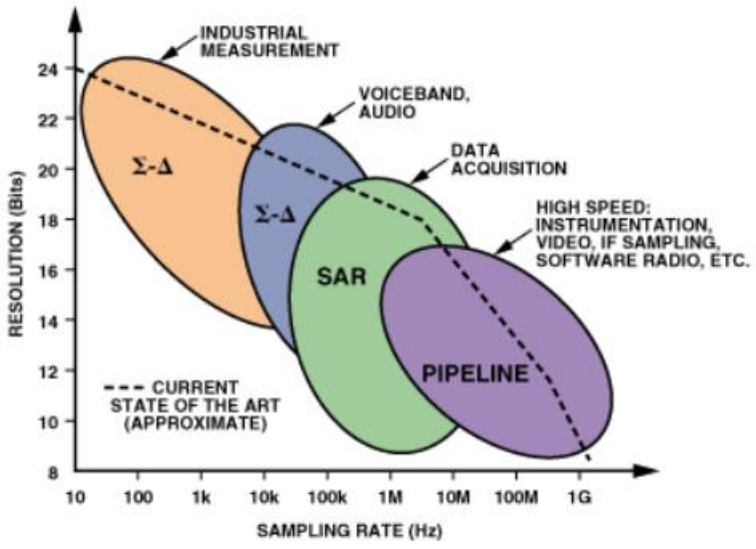


Figure 1: ADC architectures, applications, resolution, and sampling rates.

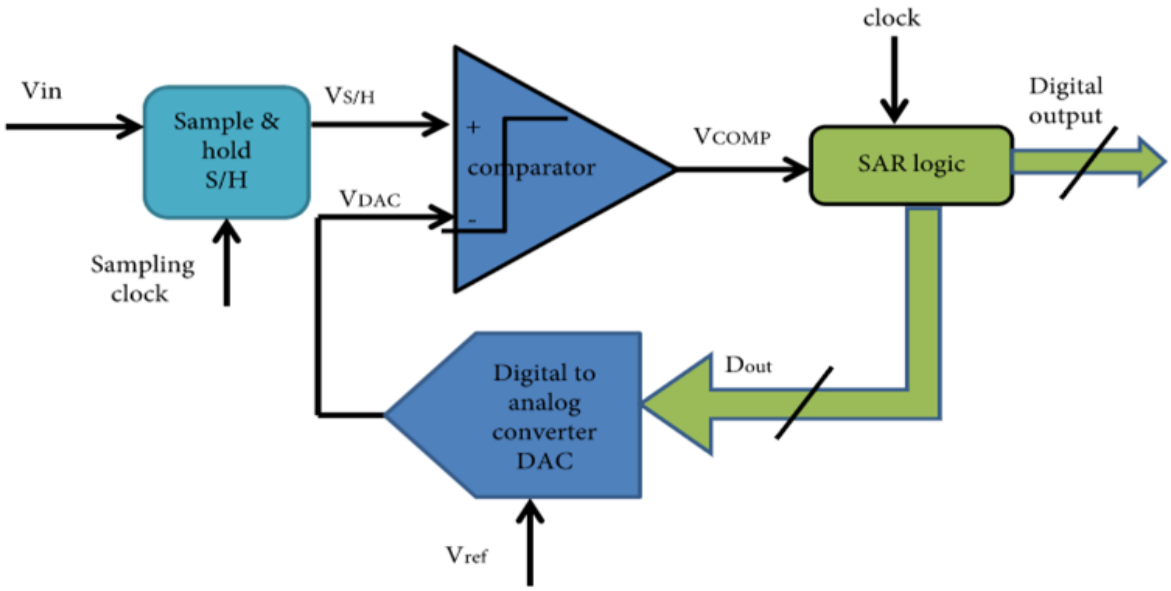


Figure 2: The SAR ADC Block diagram (Source: Hindawai.com)

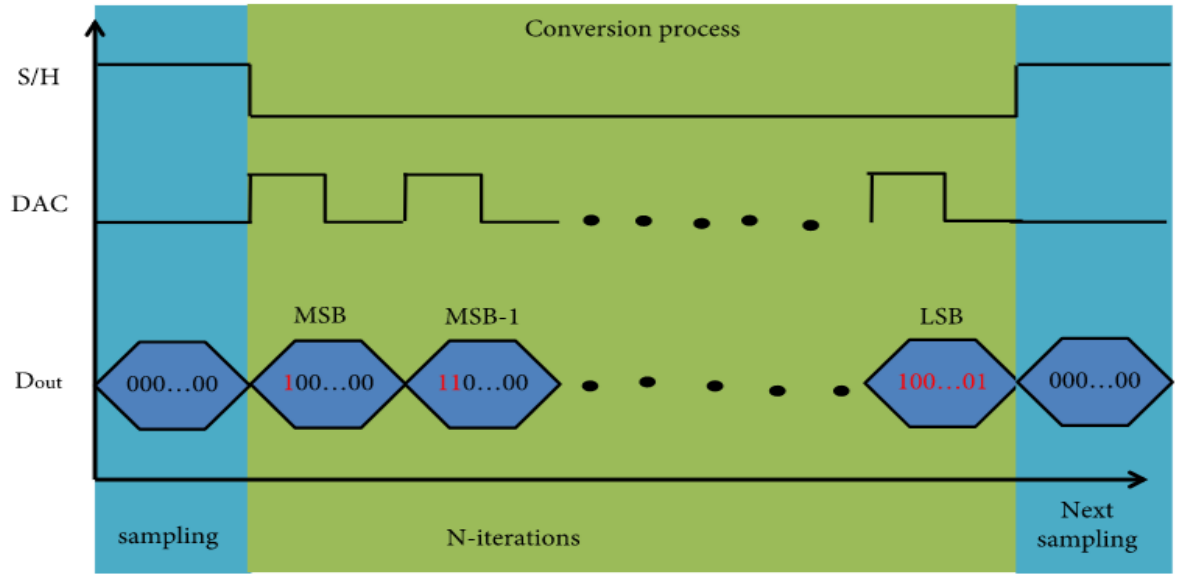


Figure 3: The SAR ADC Clock and timing profile(Source: Hindawai.com)

Primary advantage of a SAR ADC in comparison to other types of ADCs, is its ability to achieve low power consumption. This characteristic makes SAR ADCs highly desirable for various applications. In this thesis, we will explore and demonstrate various methods employed to further reduce power consumption in SAR ADCs.

The working principle of SAR (Successive Approximation Register) ADC involves a series of comparisons to determine the digital output of the analog input signal. Here are the basic steps involved in the working of a SAR ADC:

1. Sample and Hold: The input analog voltage is sampled and held by a Sample and Hold (S/H) circuit. The S/H circuit holds the input voltage constant during the conversion process.
2. Binary Search: The SAR ADC uses a binary search technique to determine the digital output of the analog input signal. The SAR ADC starts with the MSB (Most Significant Bit) and compares the input voltage with the midpoint of the DAC (Digital to Analog Converter) output voltage range. Depending on the result of the comparison, the SAR ADC sets the MSB to 1 or 0 and proceeds to the next bit.
3. Successive Approximation: The SAR ADC repeats the binary search process for each bit, moving from the MSB to the LSB (Least Significant Bit). Each bit is set to 1 or 0 depending on the comparison result with the DAC output voltage.
4. Output: Once all the bits have been determined, the digital output is available at the output of the SAR ADC.

Various configurations have been proposed for the comparator in SAR ADCs to address power consumption, time delay, and noise effects [14–24]. Additionally, modified binary-weighted capacitor digital-to-analog converter (CDAC) structures have been developed to save both area and energy [25–68]. Switching schemes for the CDAC reference voltage have also been explored to reduce power supply voltage and increase conversion speed [69–89]. Algorithmic techniques have been explored to decrease the count of iterations required for the process of conversion [90–100]. Furthermore, the SAR ADC architecture is particularly well-suited for CMOS processes [101].

However, when applied in biomedical applications, low-power SAR ADCs face several challenges. Designing a low-power, high-resolution SAR ADC becomes particularly challenging as the binary-weighted CDAC array's area increases exponentially with resolution, leading to higher power consumption and larger chip area [10]. The leakage current of the sampling switch becomes a critical consideration at low sampling frequencies, as it can introduce nonlinearity due to the extended conversion period [11]. Bit decision errors can also arise from noise sources such as the comparator, power supply, or settling time of the CDAC [12]. In the subsequent sections, we will provide a detailed explanation of the ADC components.

In wireless biomedical applications, the power consumption of Analog-to-Digital Converters (ADCs) plays a vital role in preserving battery life. These applications also have specific requirements, such as compact chip area, medium resolution, and variable sampling speeds that can range from kilo samples per second (KS/s) to mega samples per second (MS/s) [7, 8]. ADCs in these applications are expected to meet key performance parameters, including sampling frequency (FS), resolution, effective number of bits (ENOB), signal-to-noise-and-distortion ratio (SNDR), power consumption, and figure of merit (FOM). It is particularly critical to achieve higher resolution and speed simultaneously, making the ADC a crucial component in the overall design [2].

The ADC architecture plays a significant role in determining the system's performance [9]. Despite previous efforts in ADC design and implementation, developing high-speed ADCs with high resolution and low power consumption remains a challenge for biomedical applications. Therefore, adopting an energy-efficient architecture like the successive approximation register (SAR) ADC is a suitable choice for converting analog signals to digital data while meeting the low power requirements [10–12].

2.3 The Sample and Hold Circuit

At the forefront of the Successive Approximation Register Analog-to-Digital Converter (SAR ADC) lies the sample and hold (S/H) circuit. The sample switch, a crucial component of the S/H circuit, faces various challenges, such as maintaining dynamic linearity, minimizing power consumption, and enhancing noise immunity. The core function of the S/H operation is to transform a continuous-time signal into a sampled or time-discrete signal, ensuring a uniform sampling period. To prevent aliasing effects, it is imperative to adhere to the Nyquist theorem when selecting the appropriate sampling frequency.

One common approach is to employ a simple sample switch utilizing an NMOS transistor [102], which offers low power consumption at a lower cost. However, this type of switch is susceptible to sub-par switching effects, nonlinearity, harmonic distortion, and noise.
The crucial problem in S/H switching is the variation of conductivity between the gate and source terminals **(g_{gs})** of the sample transistor in the linear region. As the input signal changes **(V_{in})**, the conductivity **(g_{gs})** changes (1).

$$g_{gs} = \mu C_{ox}(W/L)\,(V_{dd} - V_{in} - V_{Tn}), \qquad (1)$$

where **μ** is the surface mobility,
c_{ox} is the capacitance per unit gate area,
and **V_{Tn}** the threshold voltage of MOSFET.
Sampled signal is subject to two common distortions: charge injection and clock feedthrough. Charge injection refers to the presence of charge between the source and drain terminals when the sample switch is turned off. Clock feedthrough, on the other hand, occurs due to the overlapping coupling capacitor between the gate and drain terminals, resulting in injected charge. To mitigate these distortions, it is best to implement the sample switch using CMOS transmission gates [8, 64, 103] or according to Figure 4 in bootstrap switch configuration [2, 5, 6, 11, 17, 22, 24, 31, 34, 45, 53, 58, 63, 65–67, 86, 90, 94, 104]. These alternative implementations help reduce the impact of charge injection and clock feedthrough, enhancing the overall performance of the sample and hold circuit.

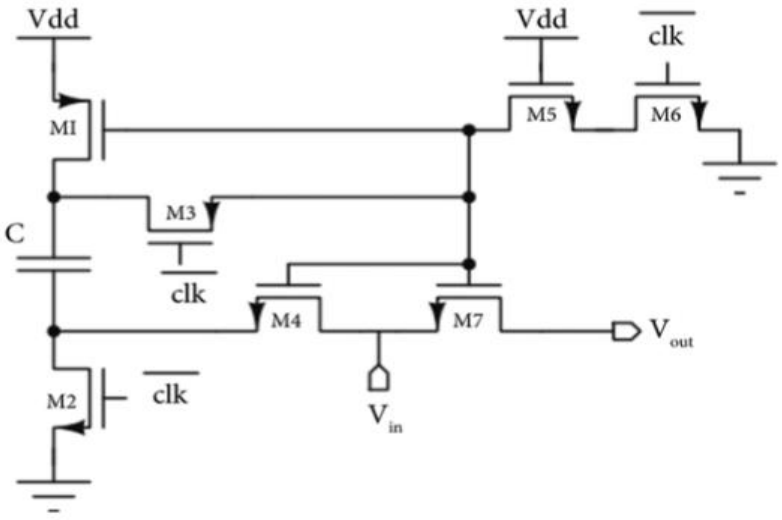


Figure 4: Conventional bootstrapped sample and hold circuit [63].

The utilization of CMOS transmission gates helps reduce conductivity variations, but it does not fully address the issue of input dependence. Furthermore, the presence of a large parasitic capacitor limits the resolution of the successive approximation register (SAR) ADC. To overcome these challenges and improve linearity while reducing power consumption, the implementation of a bootstrap switch has proven to be an effective solution [12, 23]. Figure 4 illustrates the operation of the bootstrap switch. When the complementary clock signal "$(clk)^{-}$" is high, transistors M1 and M2 are turned on, allowing the capacitor C to charge to the supply voltage. Transistors M3, M5, and M6 are employed to isolate the capacitor C from the gate of transistor M7. Contrarily, when "$(clk)^{-}$" not high, transistor M3 and M4 are switched on, enabling the capacitor C to discharge through the gate of M7. This configuration ensures that the conductivity remains constant and solely dependent on the supply voltage, thereby reducing nonlinearity error and voltage error caused by charge injection.

For enhanced linearity and improved common mode noise immunity, a double bootstrap switch is employed in some SAR ADC designs [12, 23]. This double bootstrap switch supports a fully differential architecture for the SAR comparator. By raising the gate-source voltage to twice the supply voltage, the double bootstrap switch achieves its objectives. Additionally, the use of a bootstrap switch followed by a dummy switch is employed to compensate for clock feedthrough [3, 4]. In this scheme, the charge injected during the conversion process is compared to the charge induced by the dummy switch.

In the context of SAR ADCs for biomedical applications, achieving power consumption of less than microwatts is a target design goal. Therefore, the bootstrap circuit is commonly adopted as the regular structure for the SAR sample and hold switch [63]. Table 1 provides a summary of different circuit schemes, highlighting the trade-off between power consumption, linearity, and noise. It can be seen that ultralow power consumption can be attained using CMOS TG [64], but at the expense of noise performance and dynamic linearity. On the other hand, the bootstrap switch offers improved linearity and noise characteristics. To further enhance

linearity, researchers have explored techniques such as the dual-path linearization technique [104], albeit with an associated increase in power consumption.

Table 1: Comparing different S/H structures.

Structure	CMOS TG	Bootstrap switch	Double bootstrap switch	Bootstrap switch with a dummy switch
Dynamic linearity	Poor	Good	Very high	High
Power	Very low	Low	High	Mediocre
Common-mode noise immunity	Low	Average	High	High
Distortion due to Charge injection and clock feed through	High	Average	Low	Very low

2.4 Different Configuration of Dynamic Comparator

The role of the comparator in Successive Approximation Register Analog-to-Digital Converters (SAR ADCs) is paramount, as it facilitates the comparison between the sampled input and the voltage stored on the capacitor arrays of the Digital-to-Analog Converter (DAC). The output of the SAR comparator serves as the basis for determining the equivalent digital representation, which is subsequently fed into the SAR logic for further processing. In this section, we delve into the exploration of different SAR comparator designs, with a particular focus on strategies aimed at minimizing power consumption to meet the specific requirements of biomedical applications.

In addition to power consumption, several performance factors are considered, encompassing accuracy, speed, resolution, propagation time delay, input-referred offset voltage, supply sensitivity, and meta-stability [14].

Among the different designs, the dynamic latch comparator has been widely employed in previous works [15]. The state-of-the-art Successive Approximation Register Analog-to-Digital Converters (SAR ADCs) employ four implementation techniques: the single-stage dynamic latch with a simple structure, the two-stage dynamic latch, the three-stage dynamic latch, and the multistage preamplifier dynamic latch. These techniques represent advancements in SAR ADC design, each offering unique characteristics and performance benefits.

2.4.1 Single-Stage Dynamic Latch Comparator

The primary approach for comparator design involves the utilization of single-stage dynamic latch comparators. These comparators offer advantages in terms of power and area efficiency

due to their minimal transistor count. Figure 5 illustrates the fundamental structure of a single-stage dynamic latch comparator [3, 4, 6, 16, 63, 86, 94], which comprises three sections: the differential amplification section (M1 and M2), the cross-coupled inverter section (M3:M6), and the reswitched section (S1:S4).

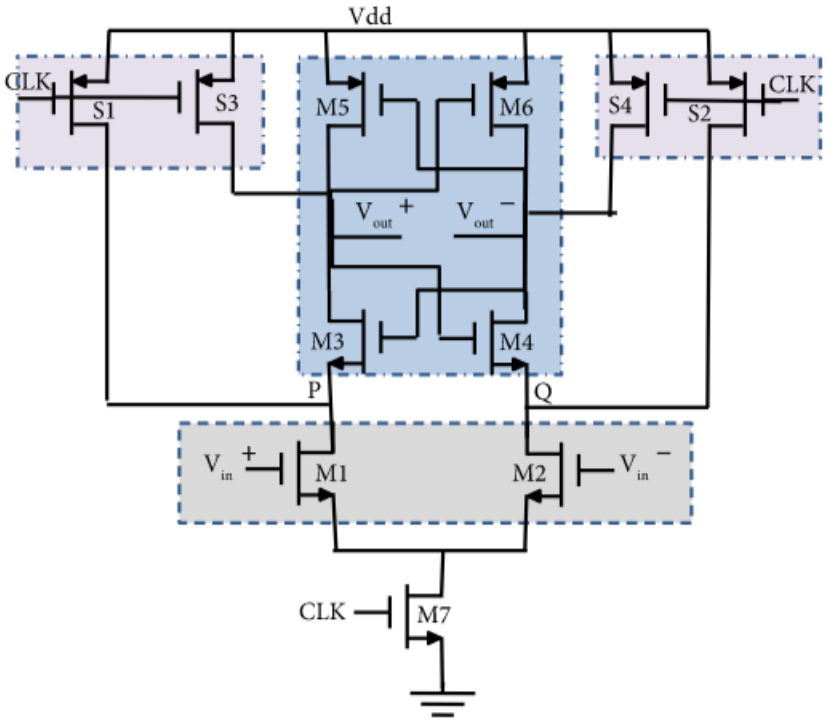


Figure 5: The basic structure of the single-stage dynamic latch comparator.[6]

The single-stage dynamic comparator operates in two distinct phases: the reset phase and the generation phase. During the reset phase, when the "clk" signal is low, the previous analog input is cleared, the switches are activated, and the output is charged to the supply voltage Vdd using the MOSFET loading capacitor. No static power is consumed during this phase. In the generation phase, when the "clk" signal is high, the amplification output is generated through a positive feedback loop established by the cross-coupled inverter section. The resulting output is determined by the differential input, and even a slight difference in the input is converted into digital levels at the full scale.

It can be observed from Figure 5, that if V+ in exceeds V- in, the node P discharges faster than the node Q, resulting in M3 and M4 to turn off until the Vgs (gate-source voltage) of M3, M4 reaches Vdd - Vthn. Once this threshold is reached, M3 and M4 are turned on. As a result, the V+ out and V- out nodes begin to discharge. The V+ out node discharges faster than the V-out node until the Vgs of M5 and M6 reach Vdd - Vthn, at which point M5 and M6 are turned on. Consequently, V+ out is grounded, and V-out is connected to Vdd, or vice versa. When V-in exceeds V+ in, the output is inverted, with V+ out connected to Vdd and V- out grounded.

A fully differential comparator offers the advantage of converting changes in input voltage signals to full-scale signals quickly and provides common mode noise rejection [6]. However,

designing the comparator involves challenges such as noise and nonlinear distortion, particularly at high Vdd. To address these challenges, adaptive supply techniques have been employed, such as using Vdd during sampling and MSB conversion, while using Vdd/2 in subsequent conversions a reduction in power consumption is observed. [16].

2.4.2 Two Stage Dynamic Latch

Two-stage comparator design as illustrated in Figure 6 involves the cascaded connection of a preamplifier stage and a single-stage dynamic latch [2, 5, 7, 11, 12, 15, 18–20, 27, 33, 35, 44, 53, 65, 90, 102].

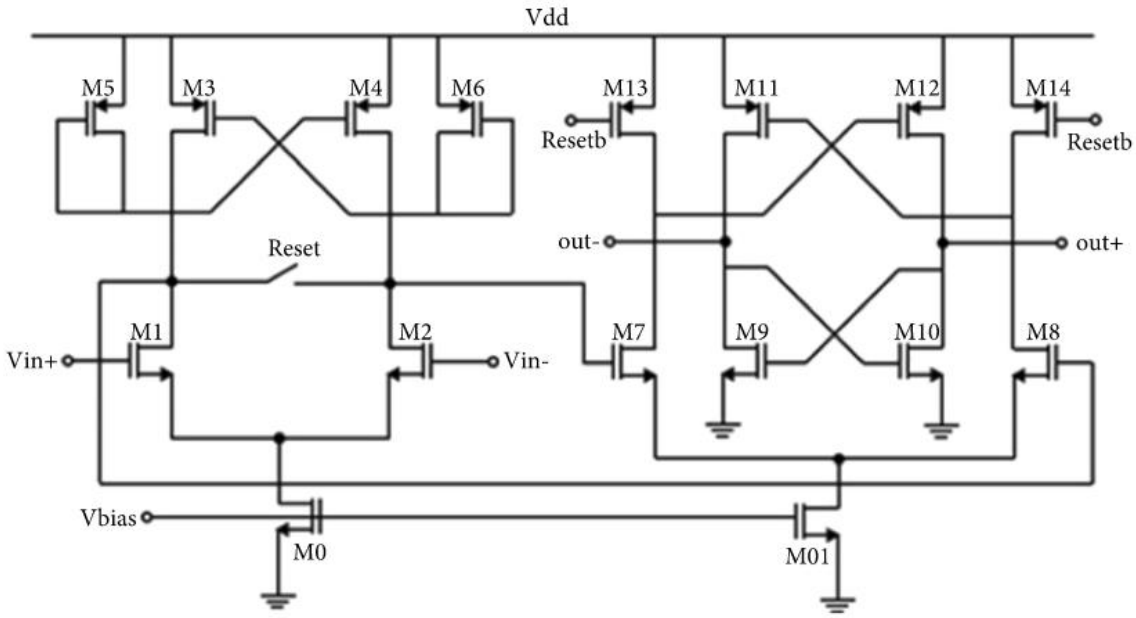


Figure 6: Two stage preamplifier and dynamic latch [27].

Two-stage dynamic latch SAR comparator offers various improvements in performance for SAR ADC. It addresses issues such as kick-back noise, input-referred offset voltage, and comparison speed [14]. Different implementations have been employed to further enhance the performance of the comparator [15]. In [17], an inverter-based amplifier is utilized to enhance common mode regulation. [18] explores the application of forward body bias with lower threshold voltages, resulting in reduced delay, improved noise sensitivity, decreased RMS input-referred noise, and enhanced offset voltage. The folded cascade preamplifier comparator introduced in [19] achieves reduced delay and power consumption, while also improving the standard deviation of the offset voltage. Furthermore, [20] focuses on transistor sizing optimization to enhance input-referred offset and minimize kick-back noise. Lastly, the dynamic latch design incorporates a complement differential pair, leading to a decrease in the input-referred offset voltage [7]. These research works demonstrate various techniques and approaches aimed at improving different performance aspects of SAR ADCs.

2.4.3 Three-Stage Dynamic Latch Comparator

To address issues related to delay, power consumption, kick-back noise, and input-referred offset voltage, the SAR comparator incorporates the preamplifier stage, single-stage dynamic latch, and buffer stage [1, 31, 103]. This integration aims to optimize the performance of the comparator. Moreover, certain designs incorporate the use of two inverter stages in conjunction with the single-stage dynamic latch [29, 52, 58]. This configuration offers multiple advantages such as eliminating static current consumption during the reset phase, improving the driving capability, and enabling a rail-to-rail digital output. In a specific approach described in Section 5, a four-input dynamic comparator is utilized [58], leveraging the dual sampling technique.

2.4.4 Multistage Preamplifier Dynamic Latch Comparator

To address the trade-off between sensitivity, offset voltage, and speed, a comparator scheme utilizes multiple stages of the preamplifier stage and a single-stage dynamic latch, combining their advantages while achieving rejection of common mode voltage and external noise [21]. This configuration takes into consideration process and temperature (PT) variations by employing a single preamplifier stage and a bistable multivibrator latch stage, resulting in PT variation of less than 0.58 LSB [22].

Conversely, alternative designs utilize a time-domain comparator to achieve power reduction, enhance the signal-to-noise and distortion ratio (SNDR), and accelerate the conversion process [23, 24]. This type of comparator operates by converting the input voltage into pulses with varying durations and employs logic circuits such as D-flip flops for signal processing.

Table 2 provides a comprehensive overview of different comparator circuit schemes, offering a comparison based on several factors including power consumption, speed, kick-back noise, input-referred offset voltage, and resolution. Among these architectures, the single-stage dynamic latch comparator stands out with its minimal transistor count, resulting in the lowest power consumption. However, it operates at relatively slower speeds and exhibits larger offset voltage and least significant bit (LSB) values, which can impact the overall resolution of the ADC. Nevertheless, for biomedical applications where lower-to-medium sampling rates and resolution requirements are acceptable, the use of single-stage dynamic latch comparators remains a viable option. An alternative approach involves incorporating an amplifier stage into the dynamic comparator to improve the offset performance. Examples of such approaches include the utilization of two-stage dynamic latch comparators, tail transistor latch comparators, and PMOS latch comparators, which provide enhanced offset voltage at the expense of higher power consumption.

Table 2: A comparison between various configurations of the comparators is presented.

Configurations	Single-stage dynamic latch comparator	Two-stage dynamic latch comparator	Three-stage dynamic latch comparator	Multistage dynamic latch comparator
No. of transistor	Least	Moderate	High	Highest
Area	Small	Moderate	Large	Largest
Power consumption	Very low	Moderate	High	Highest
Speed	Very low	Low	High	Moderate
Kick-back noise	High	Low	Moderate	Very low
Offset voltage	Highest	Moderate	Low	Very low

The provided comparison in Table 2 serves as a valuable resource for designers to select the most suitable comparator circuit configuration based on their specific power and throughput requirements. In the context of biomedical applications, where the focus is on reducing power consumption while maintaining a low sample rate and moderate accuracy, the single-stage dynamic latch comparator, with appropriate modifications [16], can be a favorable option. Alternatively, the two-stage dynamic latch comparator offers a familiar solution that strikes a balance between power, speed, and noise considerations [27]. Some researchers have explored the use of tail transistors [2, 4, 7] or PMOS latch comparators [2, 4, 12, 102] to achieve decreased power consumption in their designs.

2.5 CDAC Architecture

With the increasing demand for power consumption reduction in various biomedical applications, the role of the digital-to-analog converter (DAC) has become crucial [31]. The purpose of the DAC is to convert digital input bits into an analog output voltage using a reference voltage and an array of capacitors controlled by switches, as depicted in Figure 2. The resulting voltage is determined by the weight of the input bits relative to the reference voltage. Hence, the performance of the Digital-to-Analog Converter (DAC) is greatly influenced by the design of the capacitor array and the allocation of the reference voltage.

In previous works, a resistor-based DAC has been commonly employed [103]. An example of this is the R-2R ladder DAC shown in Figure 7. This implementation offers simplicity and high-speed conversion. However, it suffers from drawbacks such as high power consumption, large area occupation, lower stability, nonlinearity, and stringent matching requirements. Some studies have explored this DAC technique [25–89]. An alternative approach is to replace the resistor string with a capacitor array, which results in significant power and area savings. The

capacitor-based DAC (CDAC) exhibits lower energy dissipation, improved linearity, and reasonably shorter processing time. Nevertheless, the accuracy of the CDAC can be affected by leakage. Since the conversion time is typically within a few microseconds, the impact of leakage can be considered negligible [101].

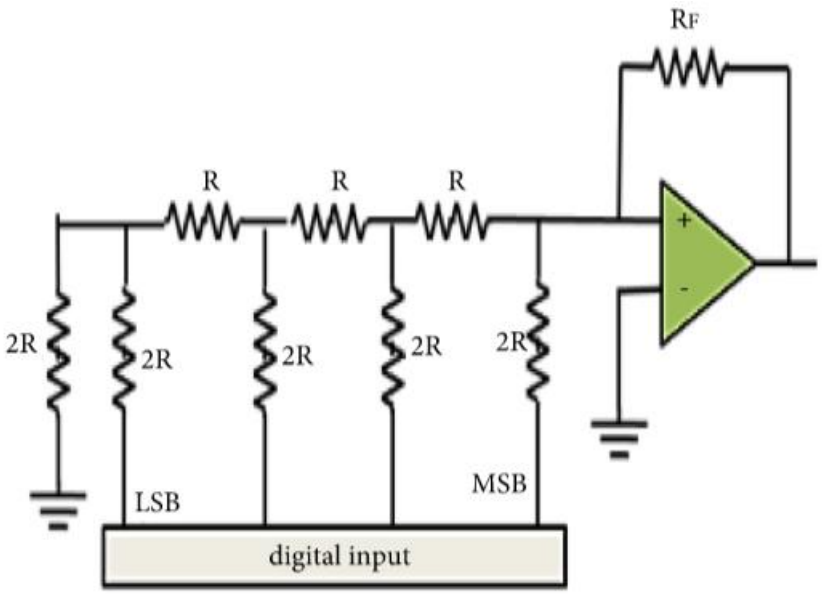


Figure 7: The R-2R DAC structure.[101]

As depicted in Figure 3, the conversion process from digital input to analog output involves two main phases: sampling and conversion. In the sampling phase, the input voltage is stored on the capacitor array of the CDAC. Subsequently, in the conversion phase, the switches are manipulated until the equivalent digital code is achieved. It is worth noting that the switching operations of the DAC represent a significant source of power consumption in SAR ADCs. In the following subsection, various techniques for implementing the CDAC will be discussed.

2.5.1 Capacitive DAC Array (CDAC)

Undoubtedly, the arrangement of the capacitor array plays a crucial role in the energy consumption of the CDAC. This section provides a detailed introduction to different techniques for implementing the capacitor array in the CDAC. Several capacitor techniques have been proposed in previous works to improve power efficiency and reduce the area occupied by the CDAC arrays [25-68]. These approaches aim to achieve power reduction and area optimization through effective management of the capacitor arrays.

The conventional structure of the capacitor array consists of binary-weighted capacitors along with a dummy capacitor for full-scale operation. In an N-bit DAC, N capacitors are utilized. However, for high-resolution DACs, a large-sized capacitor is required, as illustrated in Figure 8. In the traditional voltage switching approach, the initial configuration involves connecting the most significant bit (MSB) capacitor to the reference voltage (Vref), while the remaining capacitors are connected to ground (gnd). The voltage present on the MSB capacitor corresponds to half of the Vref. When the input voltage is below Vref/2, the MSB capacitor is switched to ground, and the subsequent capacitor is connected to Vref. Conversely, if the input

voltage exceeds or equals Vref/2, the MSB capacitor remains connected to Vref, while the next capacitor is switched to Vref. Previous studies have employed this conventional structure and voltage switching scheme [1, 25]. In order to further enhance the power efficiency of the capacitor arrays in the Digital-to-Analog Converter (DAC), various capacitive-based DAC techniques have been proposed [25-68].

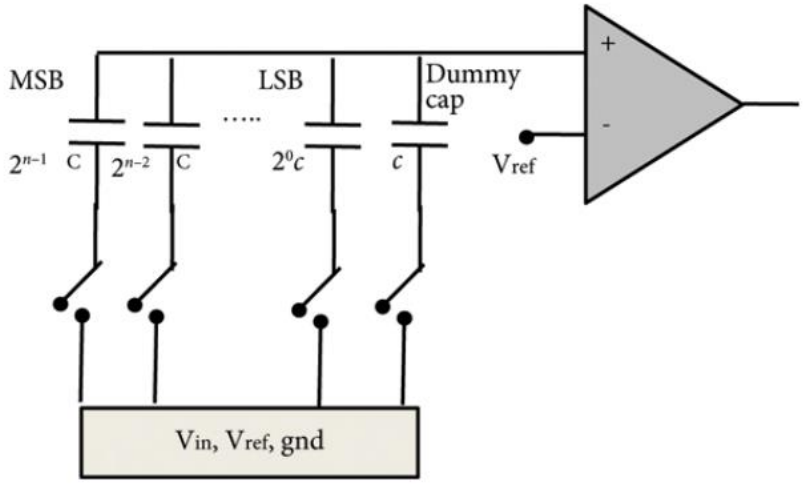


Figure 8: The scheme of conventional capacitive DAC.[27]

Various implementation techniques have been proposed to enhance the efficiency of the capacitor digital-to-analog converter (CDAC) and achieve energy and area savings [25-68]. These techniques mainly involve modifications to the CDAC array structure. Four main techniques have been introduced: the CDAC array structure technique, one capacitor splitting technique, hybrid redistribution technique, and special capacitor array arrangement technique. These approaches aim to reduce the size of the CDAC and improve its performance. Furthermore, the use of multiple reference voltages has been explored as a means to achieve power savings. These techniques collectively contribute to the optimization and efficiency of CDAC implementations.

In the CDAC array structure technique, modifications are made to all capacitors in the conventional CDAC array. The fully differential CDAC architecture, as shown in Figure 9, has been proposed to address static power consumption, improve the dynamic range, and enhance common-mode noise rejection [12, 87]. This technique involves the use of two symmetric CDAC arrays on the upper and lower sides, along with a differential input comparator. One of the key advantages of this architecture is the reduction in size of the most significant bit (MSB) capacitor, which is achieved by employing a capacitor size of 2^{n-2} instead of the original 2^{n-1} size. However, it is important to note that this technique may introduce a varying common-level problem, which needs to be carefully addressed and mitigated in the design process. Overall, the fully differential CDAC architecture offers several benefits in terms of power consumption, dynamic range, and common-mode noise rejection, but it requires careful consideration of common-level variations.

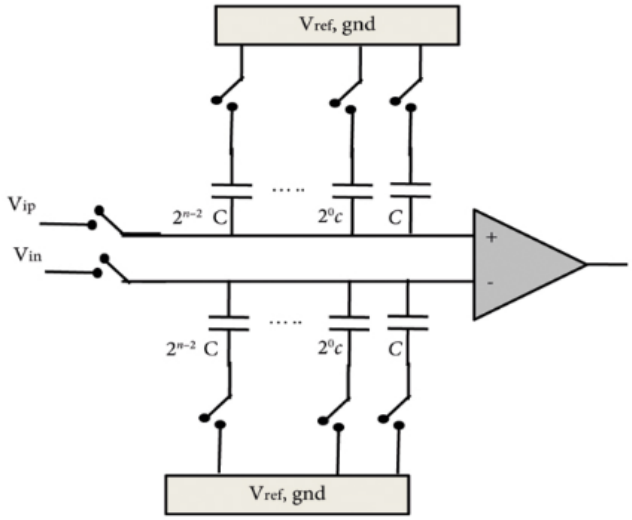


Figure 9: Structure of a Fully differential CDAC.[27]

The two-stage subarray capacitor technique has been widely explored in various studies [2–6, 19, 27–30, 90, 95]. This technique involves dividing the capacitor digital-to-analog converter (CDAC) into two subarrays: the most significant bit (MSB) subarray with m bits and the least significant bit (LSB) subarray with L bits, as depicted in Figure 10. The utilization of this technique offers several advantages, including improved energy efficiency and reduced area compared to conventional techniques. Additionally, it contributes to enhanced linearity and eliminates the influence of parasitic capacitors [27–30]. Overall, the two-stage subarray capacitor technique is a valuable approach for achieving efficient and accurate digital-to-analog conversion.

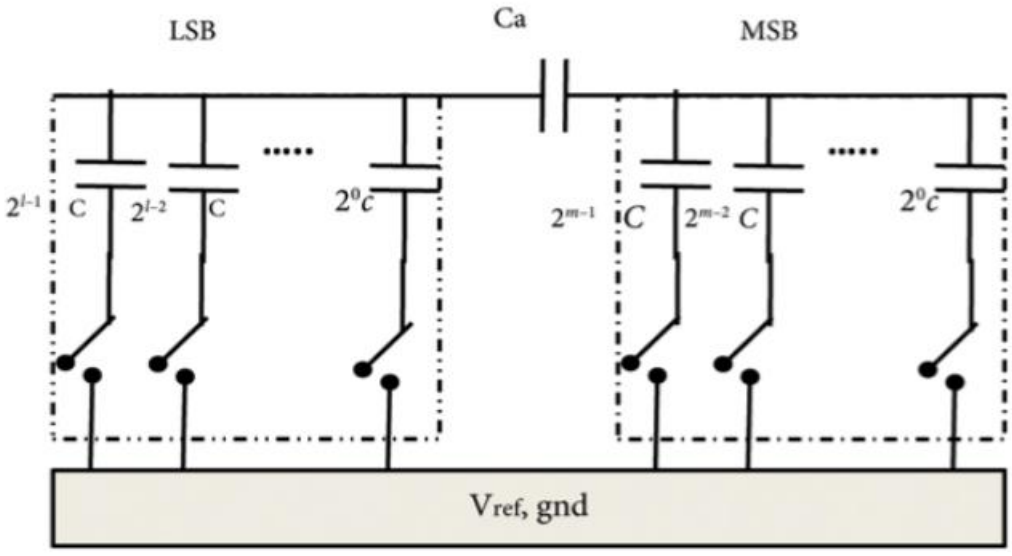


Figure 10: Two-stage subarray capacitor technique.[27]

In order to reduce die size, cost, and threshold voltage, the MOS capacitor has been adopted as a replacement for the MIM (metal-isolated-metal) capacitor DAC array [29]. Furthermore, a modified two-stage dual split CDAC array technique has been utilized to mitigate mismatch

offset and decrease the size of the capacitor array [31–34]. This structure consists of three stages: subarray capacitor, most significant bit (MSB), and middle and least significant bits (MLSB and LSB), as depicted in Figure 11. By employing the hybrid capacitor technique, it is possible to achieve high resolution and optimize the area of the capacitor digital-to-analog converter (CDAC). However, it should be noted that this technique may introduce a higher level of mismatch compared to the two-stage subarray capacitor technique. As a result, the linearity of the three-stage subarray capacitor technique may be slightly lower than that of the two-stage subarray capacitor technique. Nonetheless, the hybrid capacitor technique still offers advantages in terms of resolution and CDAC area optimization.

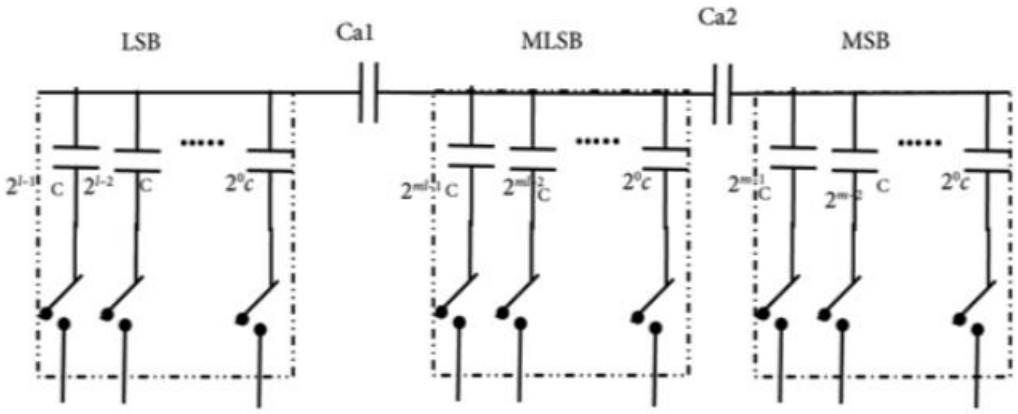


Figure 11: Dual split three-stage subarray CDAC.[31]

Unlike in the merge-split technique as indicated in Figure 12, capacitors on each side are split into two similar capacitors except the dummy capacitor and unit capacitors [35–37].

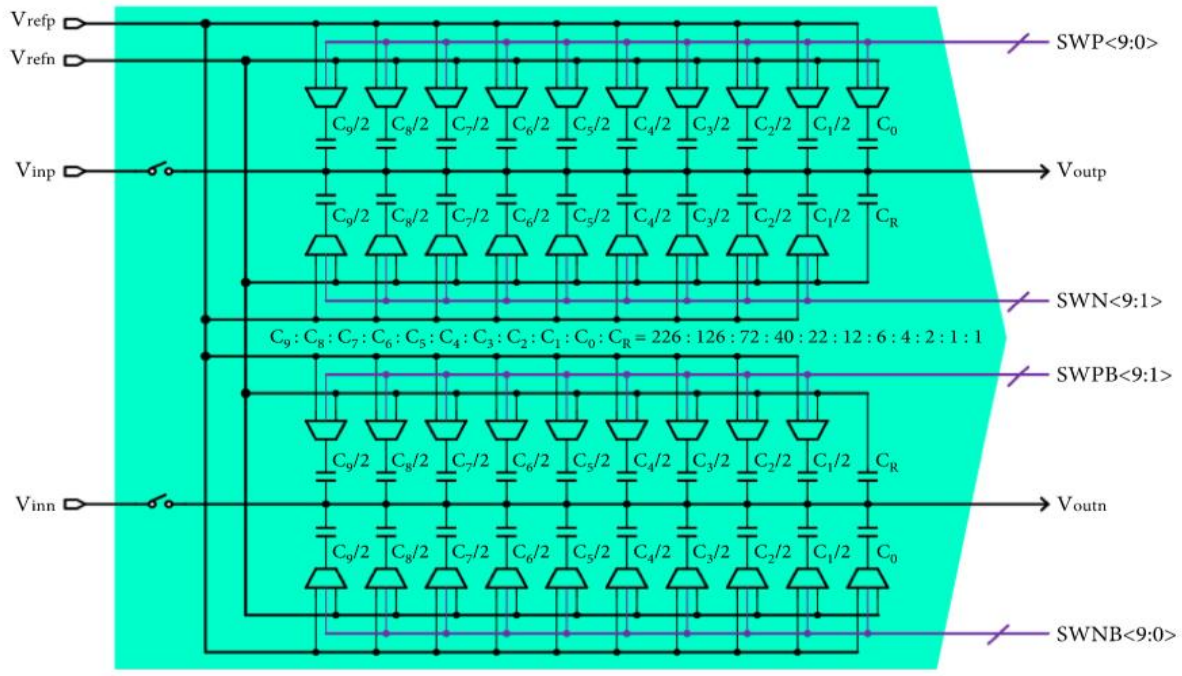


Figure 12: Merge-split CDAC technique [35].

Rather than managing the entire CDAC array, it may be sufficient to employ a single capacitor splitting technique. The MSB splitting technique, which divides the MSB capacitor into binary-weighted capacitors (Figure 13), is a widely adopted approach [11, 12, 22, 25, 38–46]. Significant power savings of up to 37% have been reported in [25]. Another technique that enhances linearity with minimal additional hardware is the reswitching technique [45]. This technique enables the reuse of previously switched capacitors between neighboring codes.

On the other hand, the LSB capacitor technique involves splitting the LSB capacitor into two serial capacitors (Figure 14) [47, 48]. This technique effectively reduces the overall capacitance by one-eighth. Similarly, the splitting of the dummy capacitor into two capacitors, known as C-2C, has been utilized in [28, 49–51] (Figure 15). This technique achieves a remarkable reduction in average energy consumption of up to 99.6% and decreases the capacitor area by up to 87.21% [51].

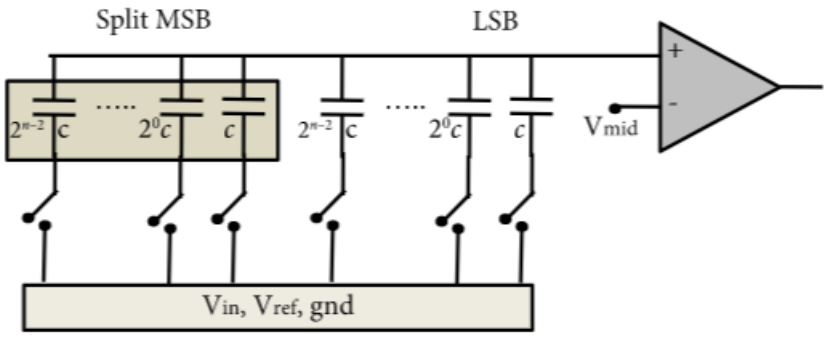


Figure 13: MSB split Capacitive DAC.[25]

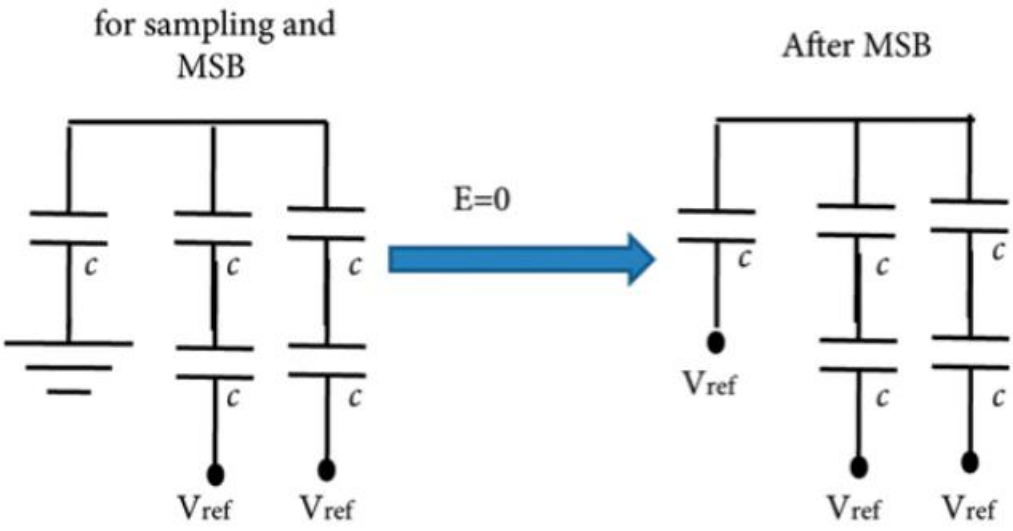


Figure 14: LSB split-Cap-DAC.[47]

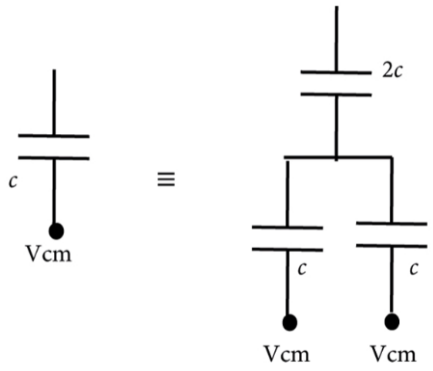


Figure 15: C-2C dummy capacitor.[47]

Various studies have investigated hybrid capacitor techniques that combine different approaches, as described in [28, 30, 49–51]. For example, in [30], a hybrid capacitor technique is proposed, which combines binary-weighted and unary capacitors. In Figure 16, the capacitor digital-to-analog converter (CDAC) is divided into two subarrays: the main array and the auxiliary array. The main array utilizes the binary-weighted technique, while the auxiliary array employs a unary capacitor array. This approach introduces the dummy capacitor charge-sharing technique, where the values of the four least significant bits are determined through charge-sharing between the dummy capacitor and the unary capacitor in the auxiliary array. Additionally, the paper utilizes the charge-sharing voltage switching scheme, which will be discussed in the subsequent subsection. Compared to the conventional structure, this hybrid approach achieves significant energy and area savings, with reductions of at least 99.5% and 93.5%, respectively.

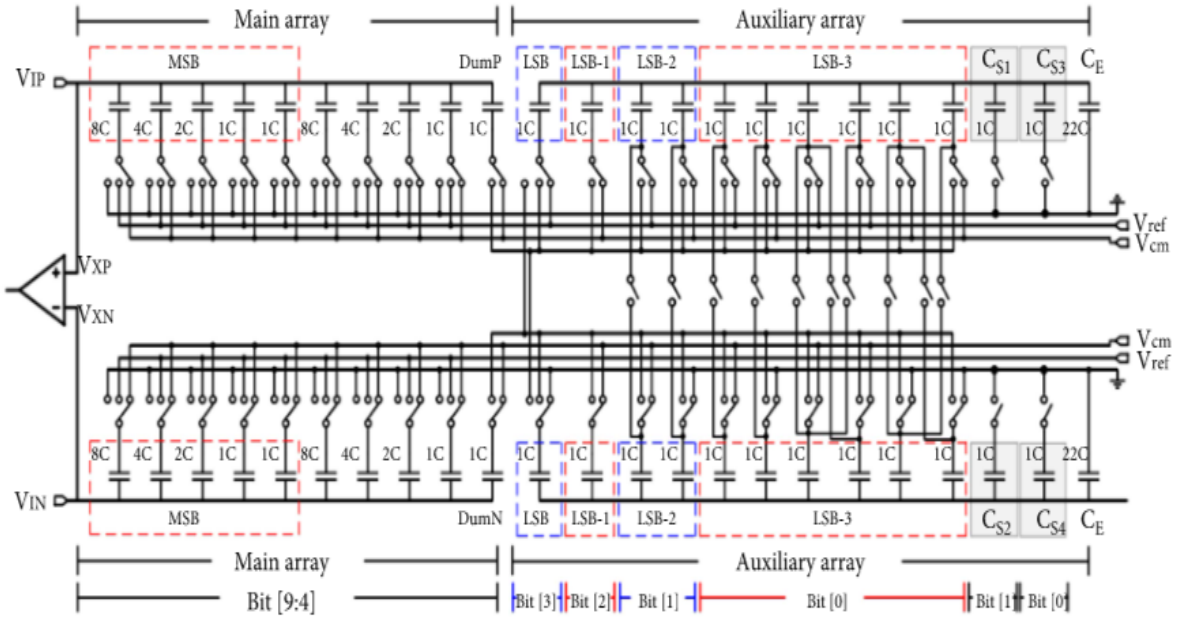


Figure 16: Charge sharing switching scheme[30].

By employing the C-2C dummy capacitor scheme, a two-stage subarray capacitor technique, and the charge-sharing voltage switching scheme [28], improvements in linearity and capacitor

matching have been achieved. Similarly, the enhancement of linearity has been addressed in [49] through the utilization of the C-2C dummy capacitor technique and the charge-sharing scheme. Another approach [50, 51] has incorporated the C-2C dummy capacitor technique with a floating capacitor scheme. Additionally, [50] has proposed the splitting of the most significant bit (MSB) and MSB-1 capacitors into equivalent binary-weighted capacitors. The floating capacitor scheme connects the MSB capacitor only during the MSB bit generation, resulting in improved linearity, reduced power consumption, and enhanced capacitor matching. This scheme has demonstrated a significant reduction in average energy by up to 99.6% and a reduction upto 87.21% in capacitor area.[51].

To achieve higher conversion speed, improved resolution, and reduced switching energy, researchers have utilized the hybrid RC technique [10, 52, 53]. In [52], a binary-weighted capacitive digital-to-analog converter (CDAC) is implemented in the most significant bit (MSB) array, while the resistor-2-resistor (R-2R) technique is employed in the least significant bit (LSB) array. Similarly, [10] explores the integration of the binary-weighted capacitor technique and the string resistor technique. Another approach described in [53] involves the incorporation of first-order and second-order cascaded low-pass filters (LPF) before the CDAC, aiming to enhance the dynamic range of the ADC.

To achieve a trade-off between linearity, area, and power consumption, researchers have utilized a segmented CDAC array technique [24]. This approach involves dividing the capacitor array into three sections. The most significant bit (MSB) capacitor follows the conventional binary-weighted technique. However, for the subsequent 9 bits, a two-stage subarray capacitor configuration is employed. In this configuration, the large-weight capacitors are replaced with seven equal capacitors, effectively reducing the area and power consumption.

Various works have explored specialized arrangements for the capacitor array technique [54–61]. The asymmetric capacitors technique [54] (Figure 17) removes the MSB on the higher side of the capacitor array. Different implementation techniques, as depicted in Figures 18 and 19, have been proposed in [55, 56] utilizing capacitance multiplexing. These approaches divide the DAC capacitor array into two subarrays, MSB and LSB, and employ two reference voltages during the comparison phase to reduce energy consumption.

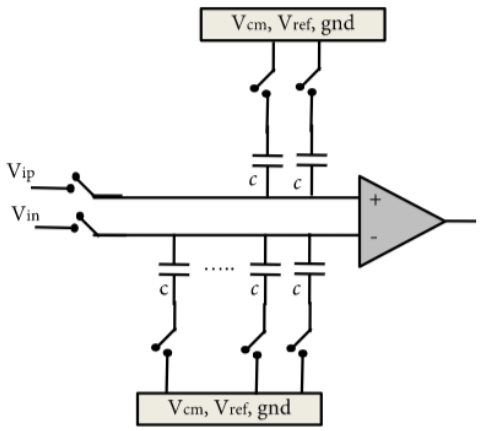


Figure 17: The Asymmetric Cap-DAC.[47]

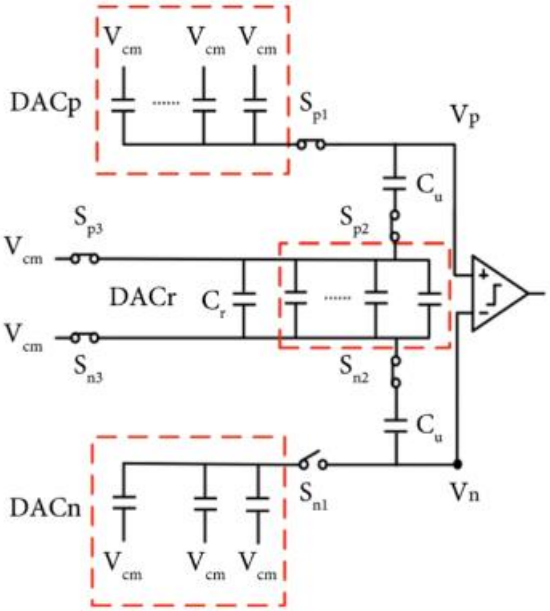


Figure 18: Schematic showing Capacitance multiplexing [56].

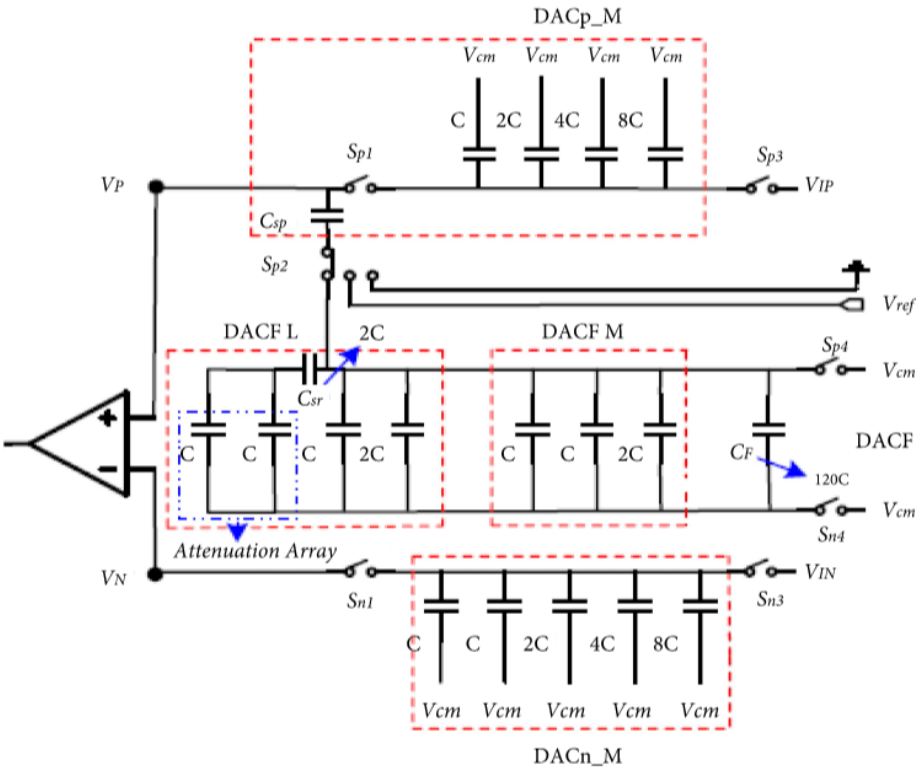


Figure 19: The Asymmetric switching using segment CDAC [55].

Achievement of energy and area reduction is demonstrated in [57] through the utilization of the goblet architecture for the capacitor array. This architecture eliminates the necessity of an additional reference voltage and allows for the capacitors to be pulled up and down to different levels, as illustrated in Figure 20.

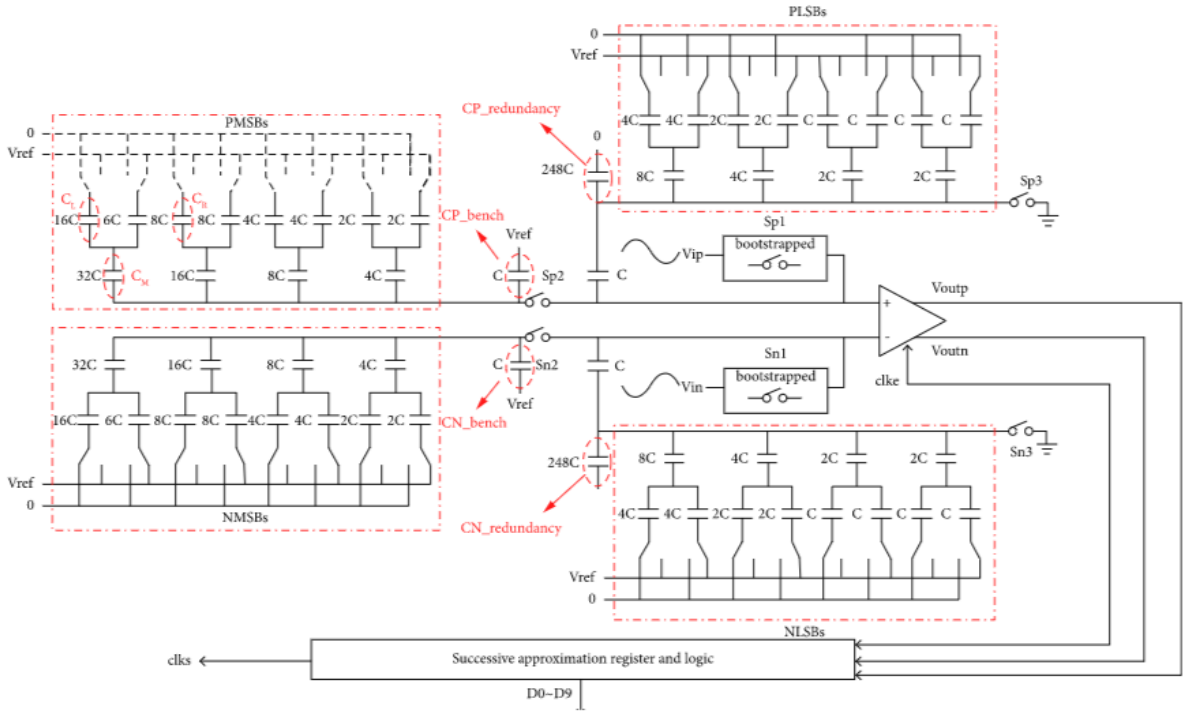


Figure 20: Extra reference voltage by using goblet architecture [57].

In the study [58], a dual sampling technique is employed, utilizing a four-input dynamic comparator. This technique introduces an additional bit, as illustrated in Figure 21. Similarly, in [59], the subrange single-side technique is adopted to handle the initial bits, allowing the proposed single-side technique to identify and bypass unnecessary switching in the main stage. Furthermore, the junction splitting technique is utilized in [60, 61], where the capacitor array is divided into subsections consisting of subcapacitors connected in series using switches, as depicted in Figure 22. Implementing this technique leads to a significant increase in the number of capacitors in each stage during the conversion process.

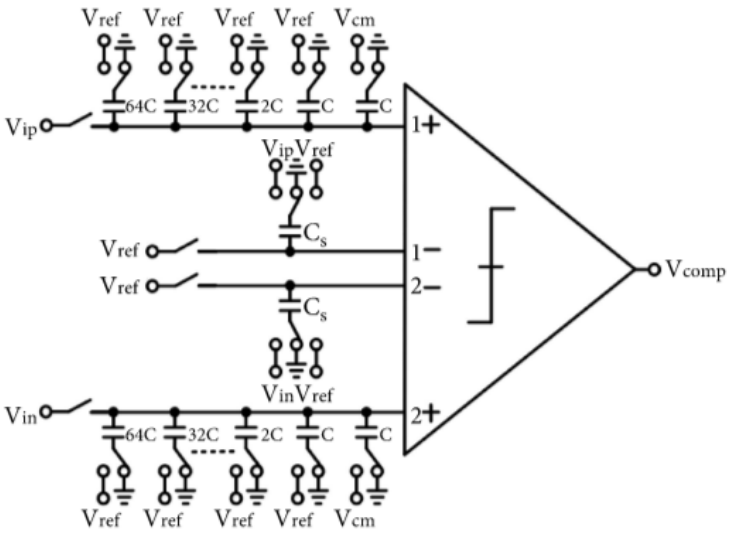


Figure 21: Technique involving dual sampling [57].

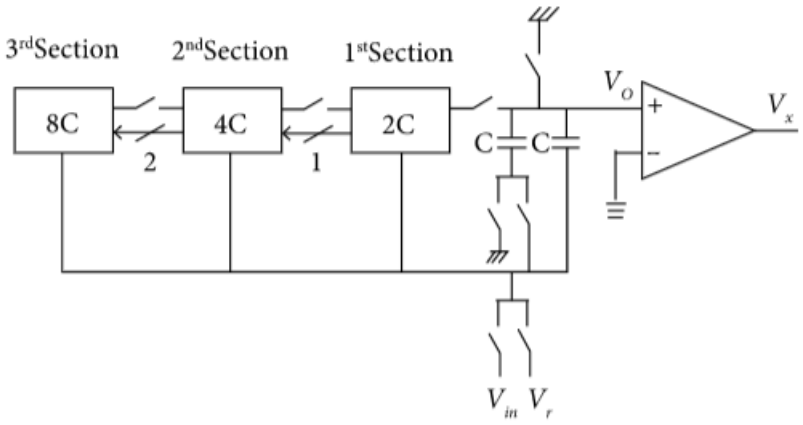


Figure 22: Hybrid and junction splitting [59].

Different and unconventional implementation techniques for SAR digital-to-analog converters (DAC) have been explored in various studies. To mitigate the impact of parasitic capacitance, the charge-sharing scheme and a switched capacitor (SC) integrator have been employed in the work presented in [62–64], as depicted in Figure 23. The operation is performed over the course of the initial three phases. During the sampling stage, the input is stored in a variable capacitor, and in the subsequent two phases, the charge is transferred to the integrator. Another approach, described in [2, 65], utilizes a thermometer decoder to reduce static errors and glitches caused by most significant bit (MSB) switching. Additionally, a pseudo-two-stage SAR technique is employed in [66]. The initial stage of the capacitor digital-to-analog converter (CDAC) array involves splitting the most significant bit (MSB) into two capacitors of equal value, except for the unit capacitor. Subsequently, in the second stage, an active charge-transferring technique is employed for the least significant bit (LSB), as shown in Figure 24. This approach effectively reduces capacitive loading and cost, requiring less design effort.

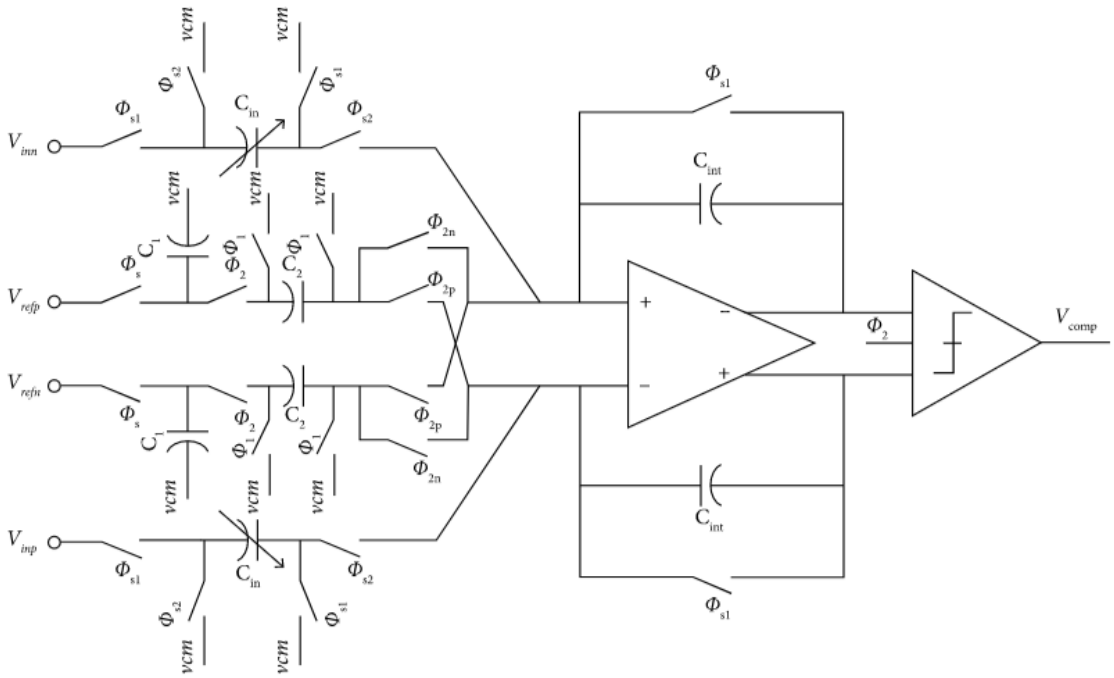


Figure 23: Schematic of the SC integrator [62].

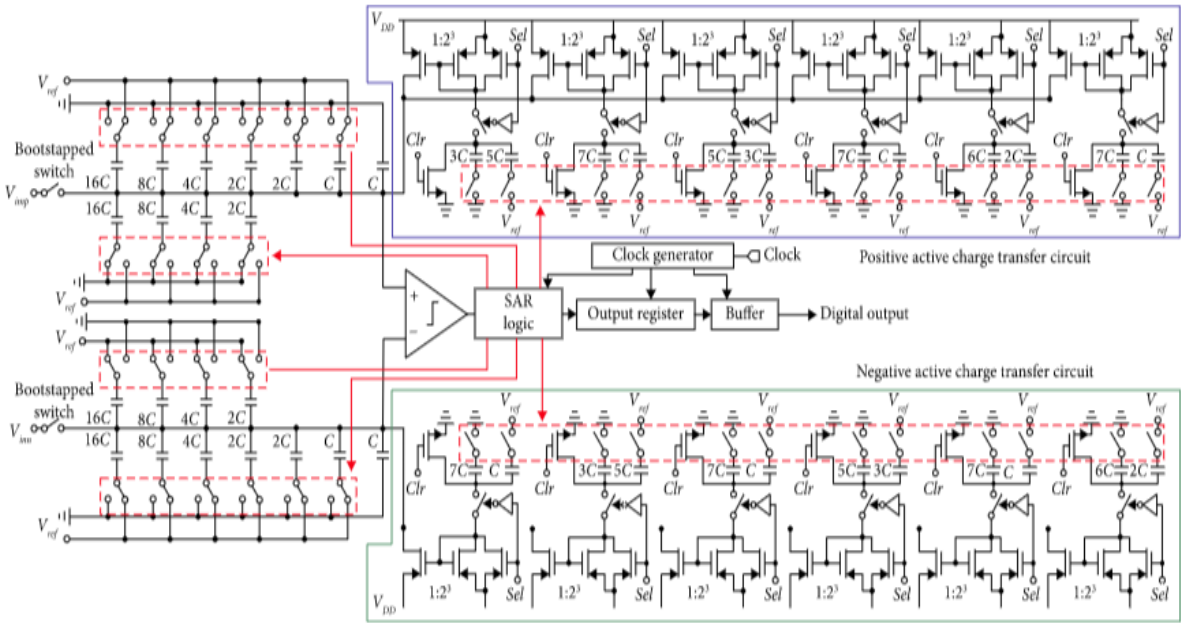


Figure 24: Pseudo two-stage SAR with active charge-transferring technique [66].

On the other hand, [67] introduces a novel technique where the difference current between the input sampling and the four most significant bits (MSB) of previous samples is quantized to achieve energy reduction. This method is illustrated in Figure 25. Another innovative approach presented in [68] involves the integration of memristors into the SAR digital-to-analog converter (DAC). Memristors are dynamic resistors that change their resistance based on the applied voltage. In [68], a memristor-based DAC configuration is proposed, utilizing two memristors connected in opposite directions, as depicted in Figure 26.

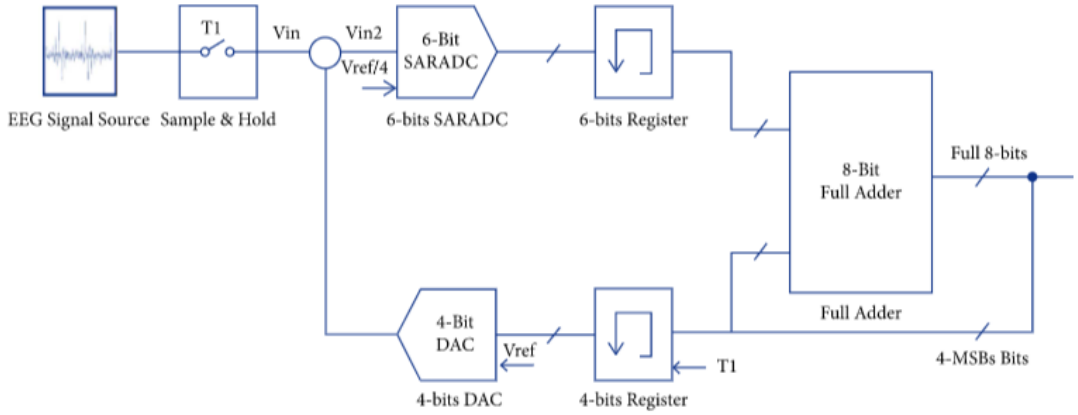


Figure 25: Block diagram of SAR ADC in [67].

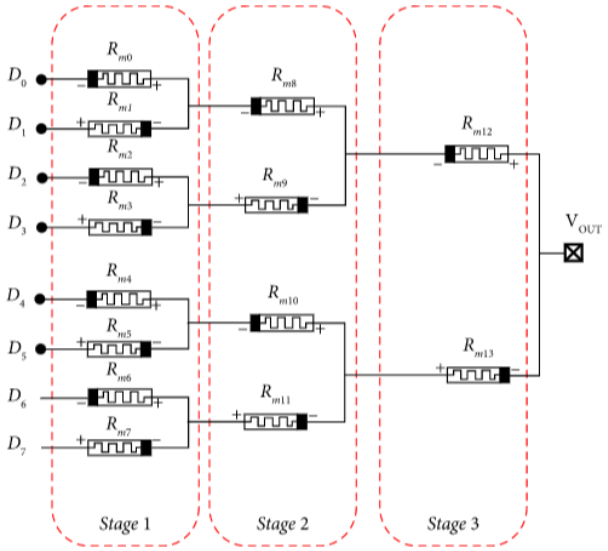


Figure 26: DAC of two oppositely connected memristor [68].

2.5.2 CDAC Voltage Switching Schemes

In order to improve energy efficiency and minimize chip area, various voltage switching schemes have been developed, with a focus on optimizing the utilization of reference voltages. These schemes can be broadly classified into three categories: two-level, three-level, and four-level voltage switching schemes.

The two-level voltage switching scheme has been employed in [41, 44, 57, 69–73] to enhance power consumption, stability, and accuracy of the capacitive digital-to-analog converter (CDAC). By utilizing two-level voltages, these schemes achieve higher precision and linearity while minimizing average switching energy.

In contrast to the conventional scheme [26], the monotonic voltage switching scheme (Figure 27) offers a distinct approach. During the sampling stage, the upper plate is charged to the input voltage, while the lower plate is shorted to Vref. Additionally, [70] introduces a third reference voltage into the scheme.

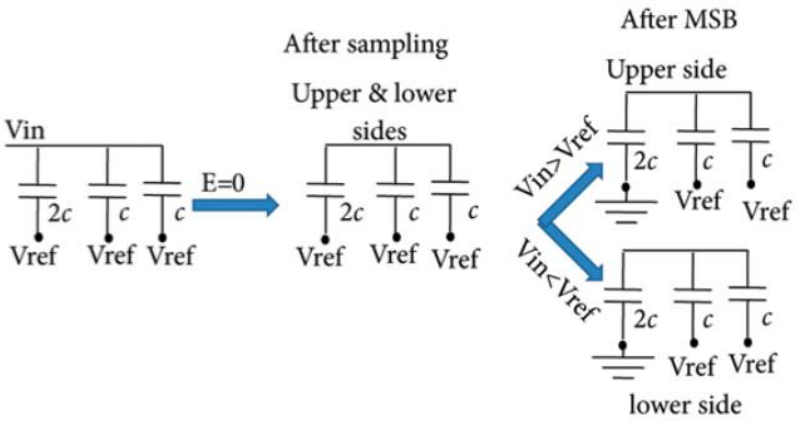


Figure 27: The monotonic voltage switching scheme.[69]

Subsequently, the comparator directly performs the determination of the MSB generation without requiring any switch changes, resulting in zero energy consumption during the initial comparison. The MSB capacitor is then switched to either Vref or gnd based on the comparator's outcome. This process is done repetitively until the LSB generation is achieved. Another voltage switching scheme, known as the charge redistribution scheme [69], is depicted in Figure 28. In the first two conversion cycles, a common mode voltage Vcm (0.5 Vref) is utilized, which leads to energy-free operation. An advantageous energy-saving approach involves the usage of a unary weighted capacitor, eradicating the need for a third reference voltage [70].

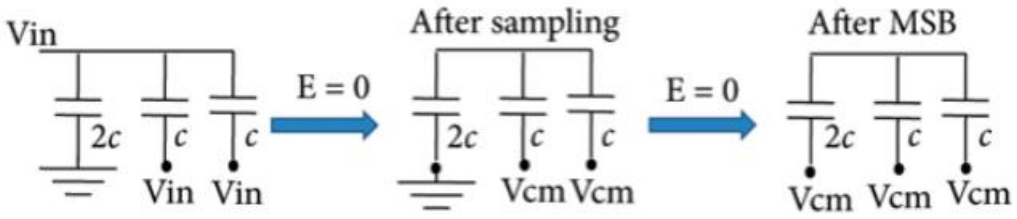


Figure 28: Scheme showing the charge redistribution[69]

In this research, a novel configuration of the capacitor array is proposed, as shown in Figure 29. This arrangement effectively eliminates energy loss from the common-mode voltage (Vcm) during the transition. Furthermore, the threshold voltage is determined as the average of the two previous threshold voltages in each conversion. However, it is important to consider that capacitor mismatch can affect the linearity of the system, and the number of clock cycles required will increase with the number of bits. In [72, 73], a DC-DC converter is employed in the design. Specifically, a two-step down DC-DC converter is utilized during the phase comparison stage, as illustrated in Figure 30. By incorporating an intermediate step in this scheme, the linearity is improved, regardless of the precision of the converter.

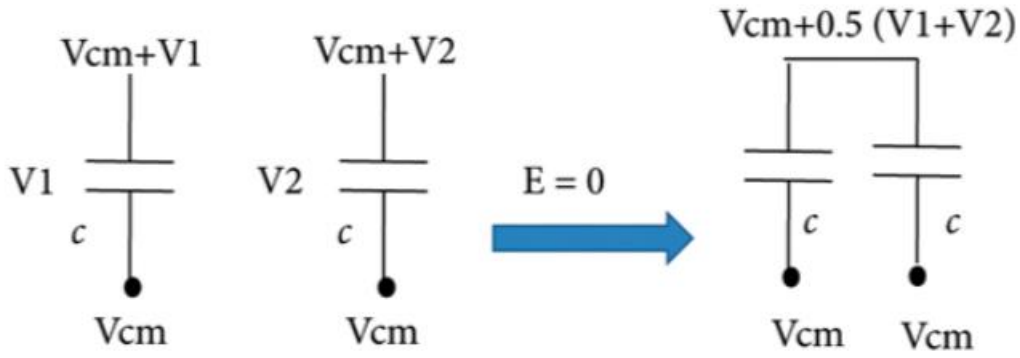


Figure 29: No energy drained from Vcm.[72]

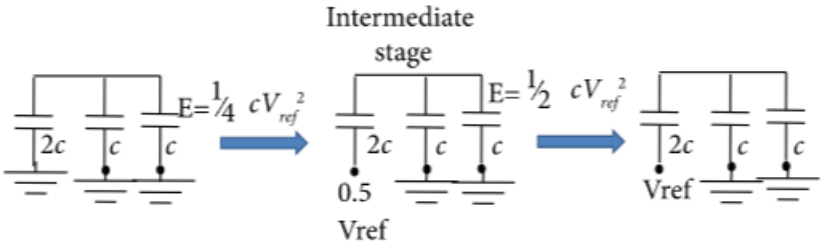


Figure 30: Two step switching method.[72]

Furthermore, so as not to use Vcm as a replacement dummy capacitor, a capacitor array approach has been proposed [44]. Previous studies [16, 26, 38, 43, 46, 51, 74–87] have employed a three-level voltage scheme (gnd, Vref, Vcm) to reduce the size of the Capacitor Digital-to-Analog Converter (CDAC) and relax the requirements for capacitor matching, without introducing additional switches. This approach introduces an additional bit to the existing schemes. Another scheme, known as the charge-sharing voltage switching scheme [30], utilizes the principle of charge sharing. In this scheme, the top plate of the upper and lower sides of the capacitor is connected to Vcm and Vref, respectively, while the bottom plate is switched to Vin. To determine the Most Significant Bit (MSB), the upper and lower voltage sides of the MSB capacitor are tuned to the same voltage of 3/4 Vref. This charge-sharing voltage switching scheme reduces overall power consumption compared to the monotonic voltage switching scheme.

As shown in Figure 32 the trilevel scheme [74] and VCM-based scheme [75] achieve nill energy consumption in the first two conversion cycles. Another distinct scheme [12, 34–36, 38, 43, 45, 76–79, 84] has been proposed to reduce the number of switching steps, as shown in Figure 33. This scheme combines a hybrid-switch capacitor array, trilevel, and VCM-based approaches. Due to the balanced charge storage on the capacitors, there is little to no energy consumption in the first three comparison cycles, effectively reducing any extra charge from the reference voltage. Following the sampling stage, the first comparison can be executed directly without consuming any switching energy. In [46], instead of feeding Vcm to all the DAC input bits, only the Least Significant Bit (LSB) depends on Vcm. Resulting to this design becoming less sensitive to variations in Vcm, but for the LSB where only one capacitor is switched.

In an alternative hybrid voltage switching scheme [80], a second bit decision scheme is implemented with the aim of reducing negative energy. Negative energy refers to the energy that flows back to the voltage sources without consuming additional energy. Figure 34 illustrates this scheme. To achieve energy savings, the reference voltage is scaled down to a quarter in [81]. This ensures that only the least significant bit (LSB) is affected by variations in the common-mode voltage (Vcm). In [41], a similar scaling down of the reference voltage (Vref/4) is combined with a monotonic scheme, and the most significant bit (MSB) is split to reduce dynamic power. In [82], a technique called higher side reset and set (HSRS) is employed for the first two bit decisions, resulting in no energy loss. All capacitors are connected to Vcm. The determination of the MSB is achieved without any changes to the switches, and then the

entire upper side is reset to ground for the MSB-1 determination. Subsequently, the upper side is set to Vcm in the next bit decision.

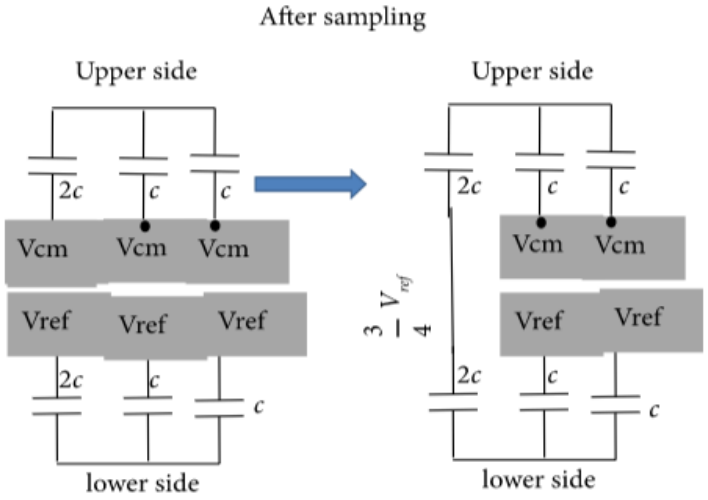


Figure 31: Charge sharing voltage switching [30]

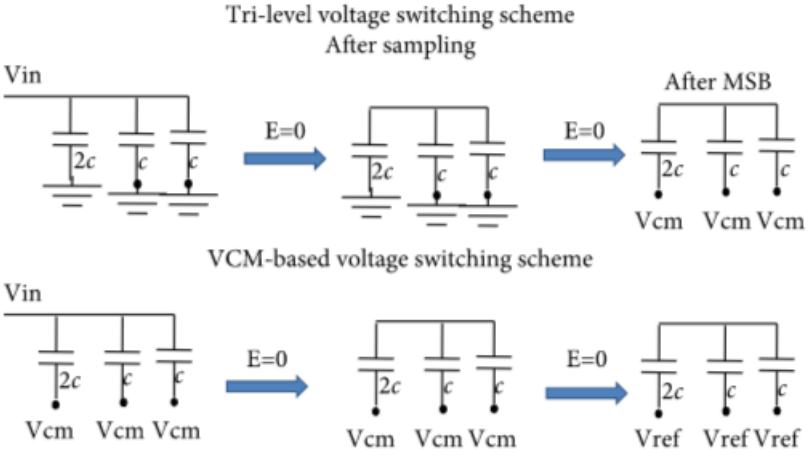


Figure 32: Trilevel and switched capacitor based on Vcm [30]

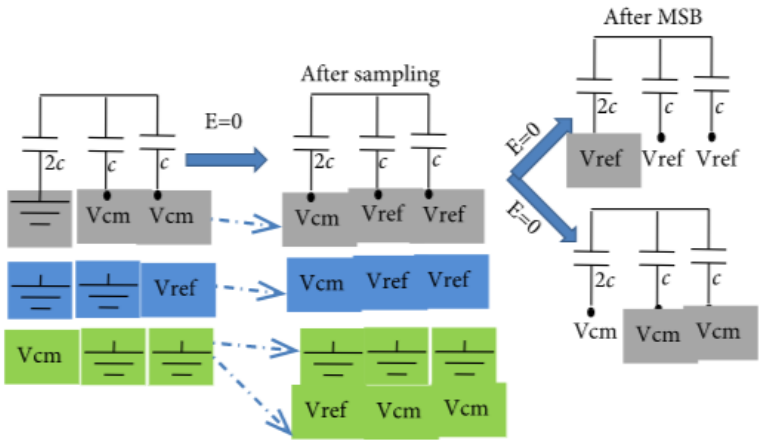


Figure 33: Scheme for Hybrid switching.[33]

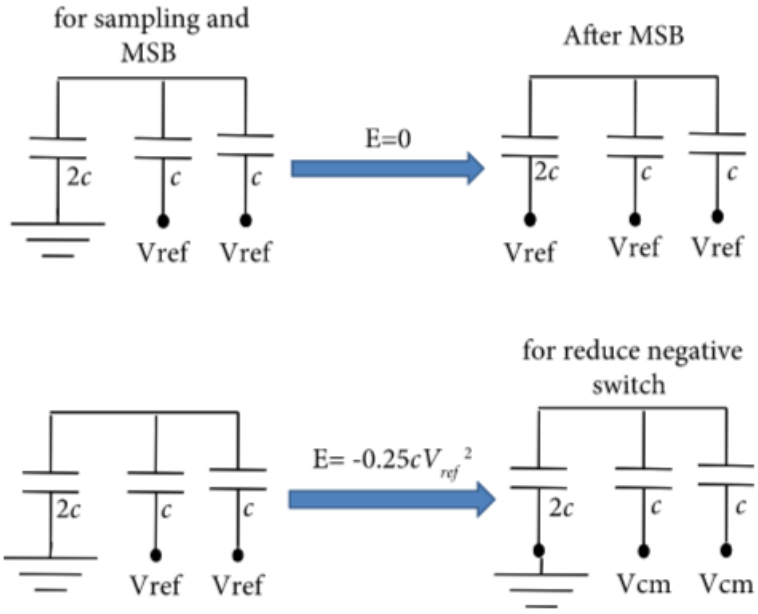


Figure 34: Energy saving method.[33]

In [85], the HSRS technique is applied in conjunction with a two-stage coarse-fine array architecture. The coarse array follows a binary weight configuration, while the fine array utilizes a unary weight configuration. Similarly, [83] introduces the spread second capacitor scheme, where all capacitors, except the MSB after the second decision, are connected to Vcm. Additionally, [87] shrinks the size of the capacitor array by employing a two-step scaled reference level. In the first stage, the MSB is set using the reference voltage Vref (top, bottom), while in the second stage, the LSB is determined using the same array capacitors and reference voltage Vref (top, bottom) + (Vreftop - Vrefbottom)/128.

In [39, 88, 89], a four-level voltage scheme (gnd, Vref, Vcm, Vaq) is utilized, where Vaq represents a quarter of the reference voltage Vref. This scheme adds two extra bits compared to the conventional approach. Furthermore, the MSB splitting capacitor technique is employed in conjunction with the four-level voltage scheme. Similarly, special works [28, 42, 46–50, 54, 56, 57, 78, 79, 89] considered the impact of parasitic capacitor array to reduce power consumption.

The reset energy, which is the energy required to recharge all capacitors to the initial state sequence, plays a crucial role in power consumption. Interestingly, the reset energy in some works [25, 39, 58, 60, 61, 71–73, 79–83, 88, 89] has been overlooked, despite its significance for the subsequent sampling period.

To reduce reset energy consumption, two approaches have been utilized. The first approach is the single-side switching method, which takes advantage of the switching variation on one side after initial compensations [43, 54, 55, 59]. The second approach is the two-step reset method, which introduces an intermediate stage between the final and initial states to achieve zero reset energy consumption. This technique has been implemented in [28, 41, 42, 49, 50, 56].

2.6 SAR Register and Its Control Logic

The final block of a successive approximation register (SAR) analog-to-digital converter is the SAR register and its control logic, which are positioned after the comparator output to fix the digital output of the SAR ADC [1–6, 8, 10, 12, 29, 31, 33, 34, 36, 40, 45, 52, 63, 65, 66, 68, 87, 90, 102, 103]. After the sampling phase, where the input signal is captured, the sampled input is compared with the reference voltage stored in the capacitor digital-to-analog converter (CDAC). The most significant bit (MSB) is determined based on the comparator output in the conversion stage. Subsequently, the SAR logic is tempered and triggered in the next clock cycle to predict the next bit, proceeding until the least significant bit (LSB) and its corresponding output code are stored in the SAR register group. As illustrated in Figure 35, SAR logic control can be achieved using a synchronous or asynchronous scheme. In the conventional synchronous SAR logic, an external regular clock is used during the sampling and conversion phases, [1–6, 8, 10, 12, 29, 31, 33, 34, 36, 40, 45, 52, 63, 65, 66, 68, 87, 90, 102, 103]. This approach involves a conversion clock that operates at a faster rate (N+1 times) than the sampling clock. Alternatively, a modified synchronous timing strategy has been proposed [90], which employs a specified time in each cycle and adjustable timing for the DAC and comparator. This strategy encompasses the settling time of the DAC thus reducing the comparison time. The choice between synchronous and asynchronous SAR logic control depends on specific design requirements. Synchronous SAR logic provides a straightforward implementation and precise timing control but requires an external clock signal. Asynchronous SAR logic, on the other hand, offers greater flexibility and potential power savings by eliminating the need for an external clock. However, it introduces challenges in terms of timing control and synchronization. The selection of the most suitable scheme depends on considerations such as power consumption, timing precision, and desired flexibility for the SAR ADC design.

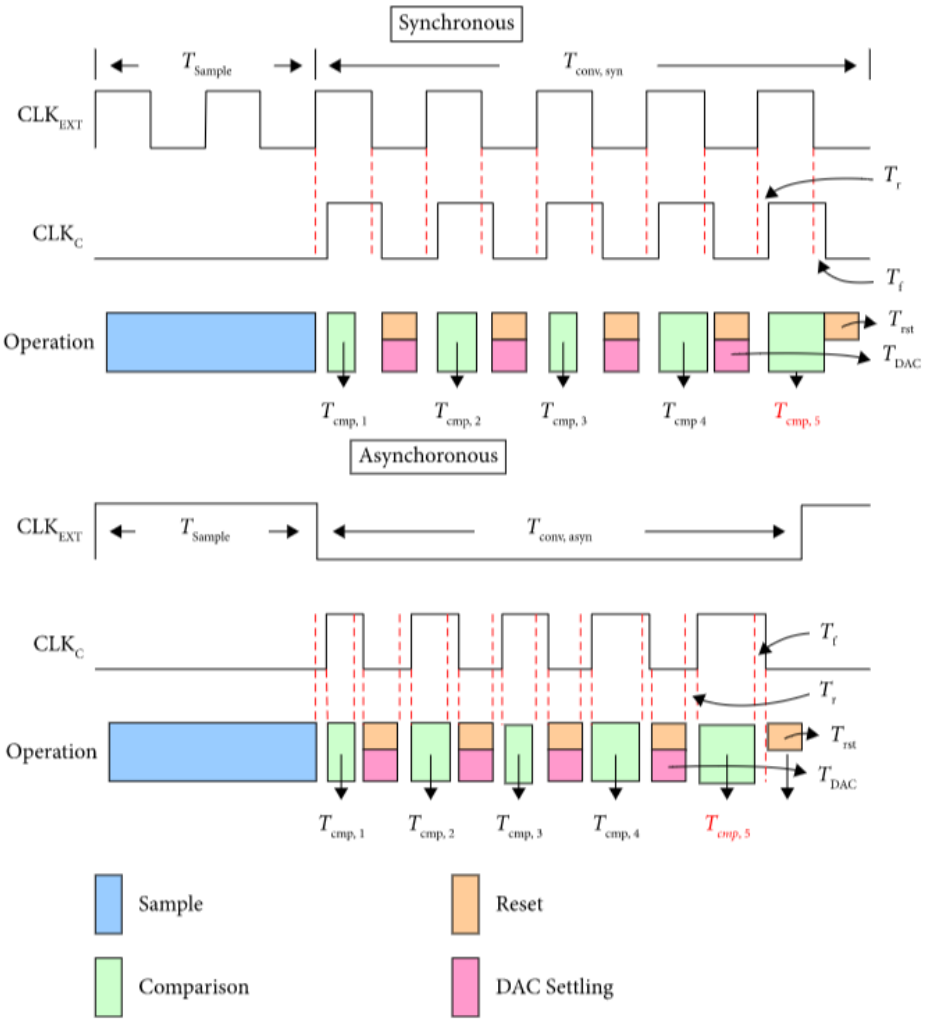


Figure 35: Showing the timing diagram of (a) synchronous (b) asynchronous control logic [91].

To improve the speed and power efficiency of the SAR ADC, an asynchronous scheme is implemented [7, 11, 16, 17, 24, 35, 44, 53, 58, 64, 86, 91], as shown in Figure 35. This approach reduces the complexity and area of the SAR control logic. Unlike the synchronous scheme, the asynchronous scheme generates the bit decision without relying on an external clock cycle for each bit. The least significant bit (LSB) is determined, and the reset clock and end-of-conversion (EOC) signals are generated in preparation for the next sampled signal [7, 11, 16, 17, 24, 35, 44, 53, 58, 64, 86, 91].

There are two distinct implementations of the SAR register and its logic control: the sequence/code register and the nonredundant SAR logic [92]. The sequence/code register, shown in Figure 36, is composed of two sets of registers. The first set, called sequence registers, acts as a ring counter to determine the output bits. The second set, referred to as code registers, stores the bit decisions [10, 11, 29, 33, 92, 102, 103].

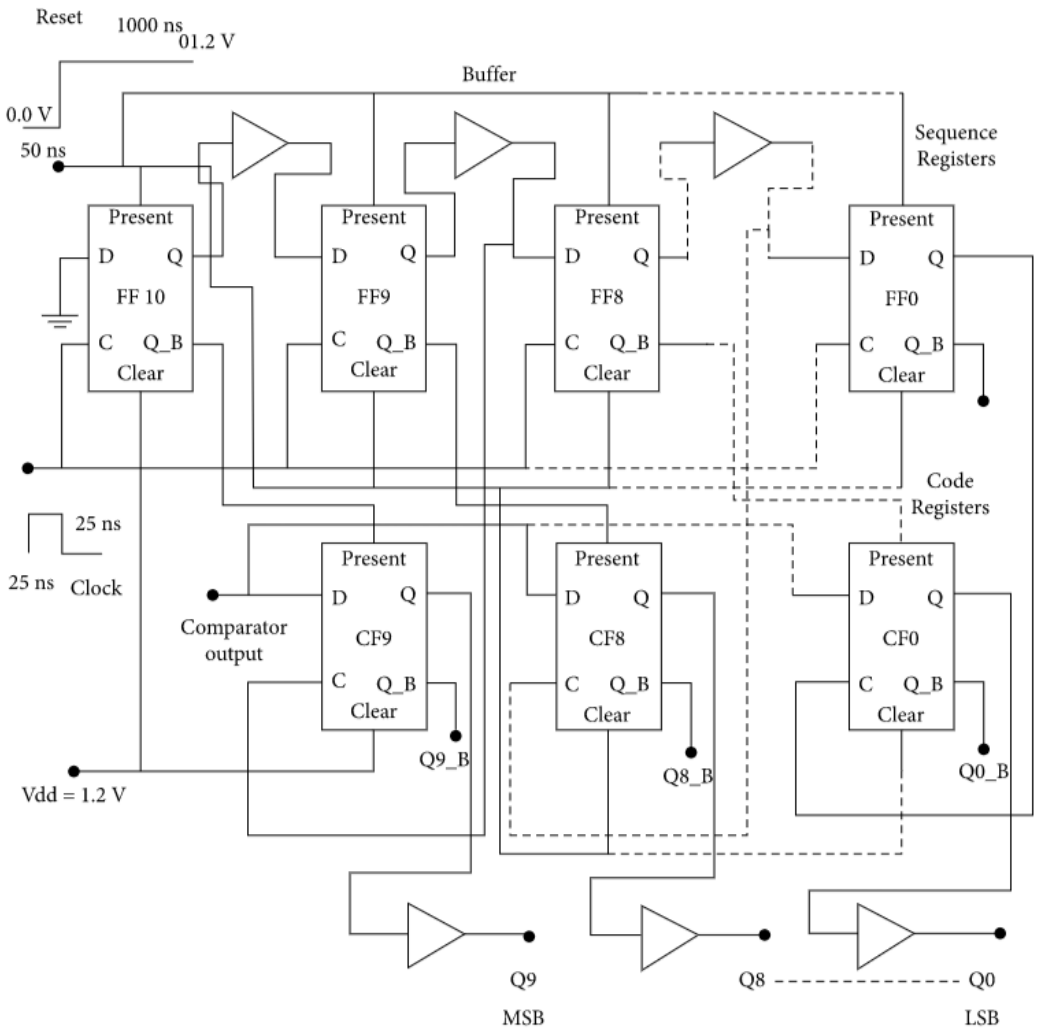


Figure 36: Schematic showing sequence/code register SAR logic [92].

The nonredundant SAR logic, as illustrated in Figure 37, is a design approach used in [4, 31, 64, 92] that offers significant advantages compared to the sequence/code structure. It achieves this by reducing the number of registers to less than half of what is required in the conventional structure. In this design, the state of each bit and the previous bits' states are utilized, leading to lower dynamic power consumption and reduced area requirements. The nonredundant SAR logic represents an efficient solution that improves the overall performance of SAR ADCs [4, 31, 64, 92].

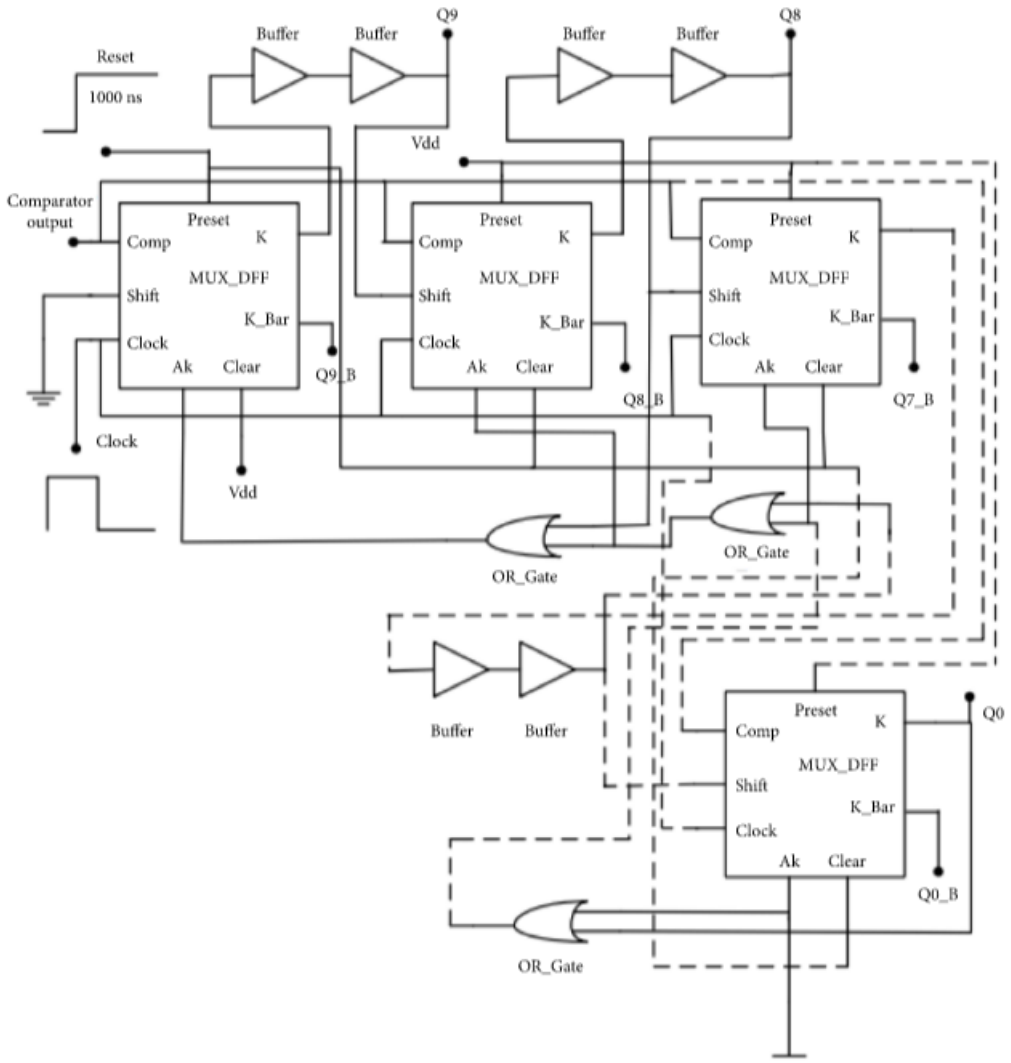


Figure 37: Schematic of the nonredundant register SAR logic [92].

The prediction algorithm [93–100] has emerged as an alternative approach to reduce power consumption and minimize the number of bit cycles in SAR ADC conversion. This algorithm incorporates advanced information about the sampled value, allowing for the detection of signal activity using a controlled SAR logic register [93]. By employing a logarithmic methodology, the prediction algorithm scales down the signal activity, resulting in reduced energy dissipation throughout the conversion process.

In the modified LSB-first algorithm [94], the variance between adjacent samples is utilized to optimize the conversion operation and reduce the size of the capacitor array. This approach enables a more efficient utilization of resources.

Furthermore, the LSB-first algorithm with a self-adaptive window is employed in [95, 96] to save higher energy. The quantization window, stated as the space between two reference voltages where the input signal is situated, is dynamically adjusted based on the input signal characteristics. This adaptive window combines the advantages of both constant-size windows and dynamic windows, resulting in improved efficiency.

Another technique, the floating window tracking algorithm [98], aims to reduce power consumption during idle time. By utilizing a three-stage biasing comparator involving a folded cascade, a differential pair with a cross-coupled load, and a dynamic latch, it is possible to accurately track the changing input signal while being turned off during idle periods.

In [99], a subrange prediction is achieved by employing a two-step loading technique to reduce charge variation in the CDAC. This helps maintain accuracy while minimizing power consumption.

Additionally, [100] focuses on minimizing the number of capacitors in a charge-sharing DAC by searching for fractions of charge and determining the solution with the smallest possible number of unit capacitors.

2.7 Synopsis of Published SAR ADC Parameters

Successive Approximation Register ADCs are known for their high energy efficiency compared to other types of ADCs. The performance efficiency of a SAR ADC can be evaluated using the Walden figure of merit (FOMW) [105]. The FOMW is a crucial parameter that indicates the power savings achieved along with specific speed (FS) and resolution, given by the ENOB equation (2).

Another important performance metric is the spurious-free dynamic range (SFDR), which measures the ratio of the root mean square (RMS) signal amplitude and the RMS of the highest undesirable signal over the bandwidth of interest. Increasing SFDR helps improve linearity in the ADC, and minimizing differential and integral nonlinearity (DNL/INL) is essential for achieving high linearity and accuracy in the conversion process.

$$FOM_w = \frac{P_{ADC}}{2^{ENOB} F_s} \quad (2)$$

(fJ/conv. – step)

A comparison is made with the cutting-edge schemes of SAR ADC, listed in Tables 3–8. The parameters of SAR ADC from 2017–2021 are given in below tables based on the technology process.

Table 3: Synopsis of the published SAR ADC parameters in 500 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	(fJ/conv.-step)
[1]	3.3	21.9 μ	—	10 k	8	7.32	—	—	1.9/−1.9	0.17/−0.28	31.4

[27]	5	20.6 m	1.7	17 M	14	13.08	80	95	0.63/−0.74	0.95/−0.58	139.9
[7]	—	14.75 n	—	2 k	10	—	—	—	—	—	—

Table 4: Synopsis of published SAR ADC parameters in 180 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W(fJ/conv.-step)
[24]	0.8	647 n	0.23	20 KHz	12	10.48	64	85	0.49/−0.41	0.47/−0.42	22
[87]	3.3	477.2 μ	—	150 KHz	14	11.3	70.28	82.91	1.4/−0.25	1.1/−2.1	—
[98]	1	12.2 μ	0.05	—	5	—	—	—	—	—	—
[2]	1.5	2.7 μ	0.052	50 KHz	12	—	66.51	77	0.83/−0.26	0.88/−0.61	30.5
[6]	1.8	1.9 μ	0.086	10 KHz	13	12.6	—	—	—	—	30.6
[63]	1.8	0.28 μ	0.17	2 KHz	11	10.14	62.8	74.4	0.1/−0.6	0.35/−0.84	120
[39]	0.6	42 n	—	20 KHz	10	9.4	58.2	73.7	0.572/−0.569	0.533/−0.422	3.11
[19]	0.5	13.99 μ	—	1 MHz	10	7.69	61.96	68.54	0.9/−0.82	1.06/−1.31	—
[33]	1.5	90.15 μ	—	1 MHz	14	11	67.9	—	0.4/−0.2	1/−1	—
[8]	1.2	310 n	—	13.56 MHz	12	11.8	—	76.4	0.5/−0.68	0.62/−0.56	—
[29]	1.2	76.88 μ	0.19	20 MHz	5	4.74	30.3	40	max −1	Less than 1.1	144
[67]	1.8	0.26 μ	—	25 KHz	8	7.1	—	50.1	0.45–0.7	−0.9	7.58
[80]	0.6	43.7 n	0.1035	100 KHz	10	9.55	59.3	78.2	0.28/−0.24	0.67/−0.41	0.58
[47]	1A/0.5D	4.1 n	0.0249	1 KHz	10	9.73	60.3	69.8	0.31/−0.3	0.32/−0.2	4.1
[53]	1.8	490 μ	—	1 MHz	—	10.76	66.54	78.42	0.72/−0.55	0.92/−0.78	57.2

[16]	1.8/0.9	6.98 μ	—	200 KHz	9	8.3	51.9	56.2	—	—	111
[11]	0.75	250 n	0.12	10 KHz	11	9.76	60.5	72	0.6/−0.37	0.94/−0.89	28.8
[66]	1.2	90 μ	0.16	3.125 MHz	10	7.41	46.37		5.64/−1	4.76/−4.24	169000
[5]	1	306 n	0.05	40 KHz	10	9.02	56.1	67	0.56/−0.69	1.14/−0.7	14.3
[10]	1.8	78.8 μ	—	50 MHz	10	—	—	—	—	—	—
[12]	0.5	68 n	0.144	10 KHz	10	9.3	57.8	61.6	0.41/−0.45	0.57/−0.48	10.8
[65]	1.8A/0.9D	9.7 μ	0.35	50 KHz	12	—	68.6	—	—	—	88.4
[52]	1.8	5.18 m	—	100 MHZ	13	12.15	76.1	—	0.37/−0.44	0.56/−0.45	9.65
[83]	1.8	3.8 m	0.23	10 MHz	10	8.5	53.1	60.9	2.8/−1	3.7/−3.6	—

Table 5: SAR ADC parameters in 130 nm process.

Reference	**Supply (v)**	**Power (w)**	**Area (mm^2)**	**F_s (S/s)**	**Resolution (dB)**	**ENOB (dB)**	**SNDR (dB)**	**SFDR (dB)**	**DNL (LSB)**	**INL (LSB)**	**(fJ/conv.-step)**
[89]	1.2	11.56 μ	—	1 M	8	7.51	47.12	57.36	0.26/−0.24	0.26/−0.28	62.11
[23]	0.4	2.66 μ	—	250 k	9	6.66	41.91		0.49/−0.44	3.24/−1.31	105.4
[99]	0.6	0.85 μ	0.12	10 k	12	11.76	—	86.5	—	—	—
[34]	1	110 n	0.16	1 k	12	10.47	64.8	78.5	0.35/−0.41	0.6/−0.74	76
[97]	0.6	0.96 μ	0.126	10 k	12	11.77	72.6	85.4	—	—	28

Table 6: Synopsis of the recently published SAR ADC performance parameters in 90 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	(fJ/conv.-step)
[31]	1	42.82 m	—	125 M	14	13.16	—	—	±0.16	±0.16	37.43
[58]	1.2	0.664 m	0.024	50 M	10	9.26	57.6	65.8	0.36/−0.32	0.45/−0.38	21.68
[103]	1	77.26 μ	—	1 M	6	5.91	—	—	—	—	—
[40]	0.5	337.66 n	—	10 k	10	—	55.93	77.17	—	—	65.1875
[64]	0.7	931 n	0.00145	0.78 M	8	6.71	44.45	61	0.87/−0.54	1.37/−1.59	11.39
[96]	0.35	74 n	—	100 k	10	9.21	57.3	—	0.37/−0.45	0.37/−0.42	1.25
[102]	1.2	10 μ	—	100 k	8	—	—	—	—	—	—
[70]	1	500 n	—	100 k	10	8.5	52.84	55.92	—	—	9.76

Table 7: Synopsis of the published SAR ADC parameters in 65 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s(S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM (fJ/conv.-step)
[68]	1.2	21 μ	—	1 M	8	7.9	49.3	61	—	—	87.9
[94]	1.2	60.8 n	0.09	10 k	10	9.4	58.4	70.6	0.4/−0.24	0.39/−0.36	9
[100]	0.5A/1.1D	318.2 n	—	100 k	10	8.55	53.23	61.87	—	—	—
[73]	1.2	—	—	100 k	10	—	—	—	—	—	—

Table 8: Synopsis of the published SAR ADC parameters in less than 65 nm process.

Reference	Process (nm)	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	(fJ/conv.-step)
[90]	40	1.1	1.3 m	0.04	160 M	12	9.21	57.18	75.29	—	—	13.71
[86]	55	1	14.8 μ		1 M	10	9.74	60.39	—	0.7/−0.5	0.6/−0.7	17.3
[36]	55	0.9	40.2 μ	0.029	10 M	12	10.03	62.13	73.52	0.45/−0.46	1.15/−1.68	3.85
[3]	45	1.1	422.3 n	—	200 k	10	9.41	—	—	0.2	0.4	3.12
[35]	40	1.1	1.32 m	0.037	100 M	10	9.3	58.03	72.6	0.62/−0.4	0.67/−0.54	130
[45]	40	0.7	0.51 μ	0.014	200 k	12	11.19	69.1	81.72	0.45	0.79	1.1
[17]	14	0.85	7 m	0.006	300 M	12	—	60.5	78.5	—	—	—

Table 3 provides a summary of recently published SAR ADC implementations using the 500 nm process. To improve linearity, the utilization of a three-stage dynamic latch is recommended [1]. By employing different switching strategies [27], enhancements in resolution (14 dB), speed (17 MS/s), and linearity (95 dB) can be achieved. Power consumption reduction of 14.7 nW has been accomplished through the use of an asynchronous converter [7].

Table 4 presents the performance parameters of SAR ADC implementations in 180 nm CMOS technology. Power consumption reduction strategies have been explored in several studies [11, 12, 24, 39, 47, 63] by employing low sampling rates. In [39, 47], various hybrid voltage switching schemes have been employed to reduce power consumption and improve the Figure of Merit for Power (FOMW). The lowest power consumption achieved was 4.1 nW in [47], while the PMOS two-stage dynamic latch comparator in [12] achieved a power reduction of 68 nW. The charge-sharing scheme with the switched capacitor (SC) integrator presented in [63] resulted in a power consumption of 280 nW. Furthermore, the use of a voltage control delay line (VCDL)-based open-loop time-domain comparator in [24] improved linearity by up to 85 dB. In [80], a modified hybrid voltage switching scheme achieved a reduced FOMW of 0.58 fJ/conv.-step. The highest resolution achieved in these implementations was 14 bits, which was accomplished using techniques such as a dual split CDAC array [33] or a two-step scaled reference level voltage [87] to mitigate capacitor array mismatch.

These studies demonstrate the advancements made in power consumption reduction, linearity improvement, and high-resolution capabilities in SAR ADC designs using 180 nm CMOS technology.

Table 5 presents the fabrications of SAR ADCs in 130 nm CMOS technology. Power consumption reduction to 110 nW is achieved by employing the dual split CDAC array technique [34] and a low sampling rate. Furthermore, power consumption reductions to 960 nW and 850 nW, along with improved linearity (SFDR) of 85.4 dB and 86.5 dB, respectively, are achieved by using a dynamic tracking algorithm [97] and a predictive algorithm with a two-step loading technique [99].

Table 6 presents a summary of implemented SAR ADCs using 90 nm CMOS technology. In [96], a power consumption of 74 nW and a Figure of Merit for Power (FOMW) of 1.25 fJ/conv.-step were achieved by employing a timing control adaptive window technique. Another approach, the MSB-splitting technique with a low sampling rate, resulted in a power consumption of 337.66 nW [40].

These results highlight the successful reduction of power consumption in SAR ADC designs using 90 nm CMOS technology. The utilization of innovative techniques such as timing control adaptive window and MSB-splitting demonstrates the potential for achieving energy-efficient and high-performance ADCs in this technology node.

In Table 7, we can observe the performance parameters of SAR ADCs implemented in 65 nm CMOS technology. The utilization of a novel LSB-first algorithm [94] significantly reduces power consumption to 60.8 nW while improving linearity (SFDR) to 70.6 dB. Another approach, the modified algorithm proposed in [100], achieves a power consumption of 318.2 nW.

Moving to processes below 65 nm, Table 8 provides a summary of performance parameters for SAR ADCs. In [3], various building blocks, including a bootstrap switch, a dummy switch, a single-stage dynamic latch comparator, a two-stage subarray capacitor technique, and a conventional synchronous SAR logic, are employed to conserve power. With technology downsized to 45 nm, the power consumption is reduced to 422.3 nW, accompanied by a Figure of Merit for Power (FOMW) of 3.12 fJ/conv.-step. Furthermore, the reswitching technique presented in [45] achieves a power consumption of 510 nW, while enhancing linearity (SFDR) to 81.72 dB with a FOMW of 1.1 fJ/conv.-step.

These results demonstrate the advancements made in reducing power consumption and improving performance in SAR ADCs implemented in sub-65 nm processes. The utilization of innovative algorithms and techniques has led to significant improvements in power efficiency and linearity, paving the way for more energy-efficient and high-performance ADC designs.

2.8 Conclusion

I. Based on the analysis conducted in the previous tables, the following conclusions can be drawn:

II. I. Several techniques have demonstrated impressive results in achieving ultralow power consumption. The complement differential pair of the dynamic latch achieved a power consumption of 14 nW, the modified hybrid voltage switching scheme achieved 42 nW and 43 nW, the LSB capacitor technique achieved 4.1 nW, the dual split CDAC array technique achieved 110 nW, and the charge-sharing scheme with a switched capacitor integrator achieved 280 nW. Other techniques, such as timing control adaptive window, novel LSB-first algorithm, and modified algorithm with minimum capacitor count, also exhibited low power consumption. The key building blocks of the SAR ADC, including the bootstrap switch, two-stage dynamic latch comparator, and two-stage subarray capacitor technique, demonstrated power consumption ranging from 250 nW to 306 nW. These implementations are suitable for low sampling frequency applications, particularly in the field of biomedical applications.

III. II. The Figure of Merit Walden (FOMW), which considers the trade-off between power consumption, sampling frequency, and resolution, was evaluated. The modified voltage switching scheme and the quantization window of the SAR control logic algorithm achieved the best FOMW results, with values below 1.25 (fJ/conv.-step).

IV.

V. III. To achieve higher resolution and improved linearity, the two-stage subarray capacitor technique with a new voltage switching strategy and the segmented CDAC array have been proposed. Furthermore, the predictive algorithm and dynamic tracking algorithm have shown promising results in terms of resolution and linearity.

VI. IV. With increasing resolution, the mismatch of the capacitor array also increases, leading to reduced linearity in the SAR ADC. However, advancements in downsizing CMOS technologies have facilitated higher sampling frequencies.

VII. These findings highlight the significant advancements and trade-offs in power consumption, linearity, resolution, and sampling frequency in the design and implementation of SAR ADCs.

Overall, the state-of-the-art techniques discussed in the previous tables have made significant advancements in terms of power consumption, FOMW, resolution, linearity, and mismatch reduction in SAR ADC designs.

Chapter 3

SAR ADC Principles

3.1 Analog to Digital Conversion fundamentals

3.1.1 Resolution

The resolution of an ADC refers to the number of bits in its output. Each bit represents a specific voltage step, with VLSB (Voltage Least Significant Bit) being the smallest detectable step. For an N-bit ADC, the value of VLSB is equal to the ADC's voltage range divided by 2^N. However, in practical scenarios, the effective resolution of an ADC is often lower than its nominal value due to various sources of error.

3.1.2 Quantization Error

When an analog input signal is quantized into a finite number of steps in an ADC, quantization error occurs. This error arises from the discrepancy between the actual analog value and the nearest quantized representation. The maximum magnitude of quantization error is VLSB/2. It's important to note that even in an ideal ADC, quantization error is present. This error can be considered as uncorrelated and can be defined as white noise.

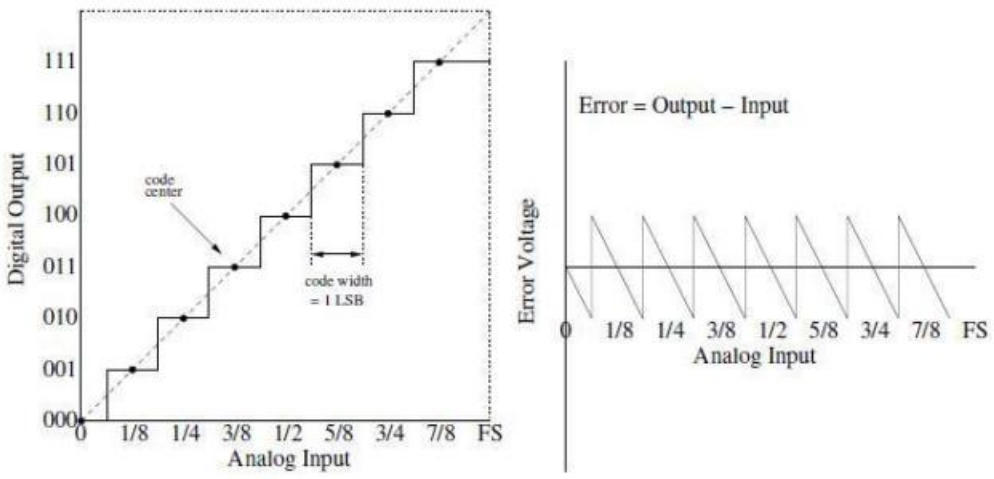


Figure 38: An ideal ADC with Quantization error[108]

3.2 Static Performance

3.2.1 Offset and Full-Scale Error

Offset error refers to the nonconformity of the code transition voltage at the first step from the ideal value, resulting typically half of the Least Significant Bit (LSB). On the other hand, full-scale error represents the deviation of the last code transition voltage from its ideal value. Figure 39 provides a visual representation of these errors.

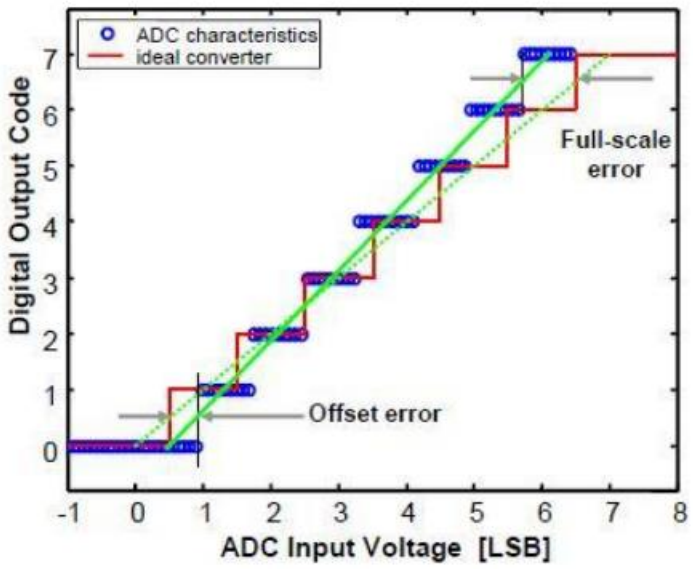


Figure 39: Offset and full scale error[108]

3.2.2 Differential Nonlinearity

Differential nonlinearity (DNL) refers to the deviation of the transition width between adjacent output codes from the ideal value of 1 LSB (Least Significant Bit). When the code width is narrower than the ideal, DNL becomes negative, and when it is wider, DNL comes positive. In an ideal ADC, where the code width is one, DNL is zero.

3.2.3 Integral Nonlinearity

Integral nonlinearity (INL) is the alteration between the centers of the output codes and the ideal line. It can be expressed as the sum of individual DNL values [5]. Alternatively, INL can be defined as the distance between the code centers and the best-fit line. Figure 40 illustrates the maximum INL, which is measured relative to the ideal line.

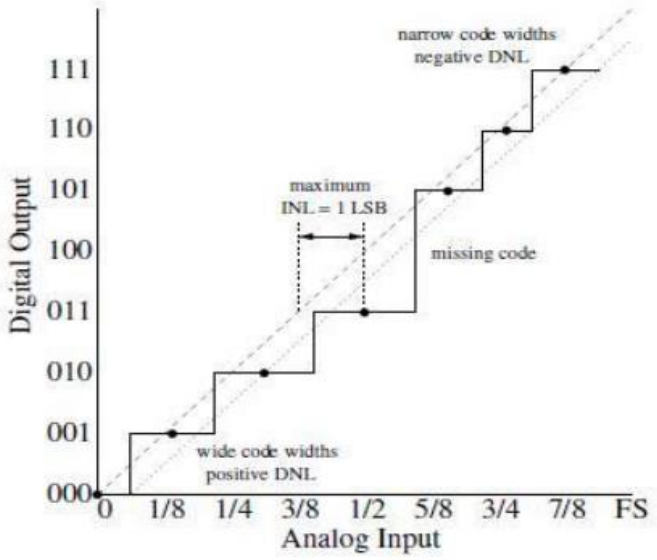


Figure 40: DNL and maximum IN [4]

3.2.4 Missing Code

Missing code occurs in an ADC when there is no digital code generated at the output for a specific input voltage. This can be visualized in Figure 40, which provides an example of a missing code scenario. In the presence of a missing code, the Differential Nonlinearity (DNL) value is equal to -1.

3.3 Dynamic Performance

3.3.1 Signal to Noise Ratio

Signal to Noise ratio (SNR) is the ratio of the input signal power to the total noise power.

$$SNR = 10 \cdot \log_{10} \frac{P_S}{P_N} \tag{2a}$$

In an ideal ADC the only noise source is the quantization error.

$$\begin{aligned} P_S &= V_{\text{in max}}^2 = \left(\frac{2^N \cdot V_{LSB}}{2\sqrt{2}}\right)^2 \\ P_N &= V_{\text{error}}^2 = \left(\frac{V_{LSB}}{\sqrt{12}}\right)^2 \end{aligned} \tag{2b}$$

By inserting P_S and P_N into Equation above SNR of an ideal ADC is expressed as below:

$$SNR = 20.\log_{10} \frac{\frac{2^N \cdot V_{LSB}}{2\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}} = 6.02\text{N} + 1.76 \tag{2c}$$

3.3.2 Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is a measurement that quantifies the ratio between the input signal and the highest peak of any undesired spurs or harmonic distortion tones. Mathematically, SFDR can be expressed using Equation 3.

$$SFDR = 20.log_{10} \frac{V_{Signal}}{V_{Spurious}} \tag{3}$$

3.3.3 Signal to Noise and Distortion Ratio

The Signal to Noise and Distortion Ratio (SINAD) represents the ratio of the input signal to the combined sum of the total noise and harmonics. Mathematically, the SINAD can be expressed using Equation 4.

$$SINAD = 20.log_{10} \frac{V_{Signal}}{V_{Noise}+V_{HD}} \tag{4}$$

3.3.4 Effective Number of Bits

The Effective Number of Bits (ENOB) is a metric derived from the SINAD value. ENOB is often castoff as a more convenient representation of SINAD, as it expresses the SINAD measurement in terms of the number of bits. ENOB can be calculated using the equations mentioned above.

$$ENOB = \frac{(SINAD - 1.76)dB}{6.02dB} \quad (5)$$

3.4.1 Bootstrapped Sample-And-Hold Circuit

The sample-and-hold circuit is an essential component that captures and maintains the value of an analog signal for a specific duration. In typical circuits, the switch used in this circuit can be implemented using an NMOS pass gate, a PMOS pass gate, or a CMOS transmission gate, as depicted in Figure 41. However, these switches possess certain non-ideal characteristics that can impact the quality of the sampled signal.

MOSFET switches operate in the triode region when they are turned "ON," resulting in a non-zero on-resistance (RON) that varies with the input signal, as shown in Equation 12. Another effect dependent on the input signal is the injection of charge from the inversion layer into the load capacitor when the switch is turned off. This injected charge (QCH) can be calculated using Equation 13. Additionally, clock feedthrough occurs due to the presence of parasitic capacitances between the switch's gate and the output node. The switching activity of the clock generates a voltage disturbance, as described in Equation 14.

. Fig. 42 illustrates the effect of these non-idealities in MOSFET switches [7].

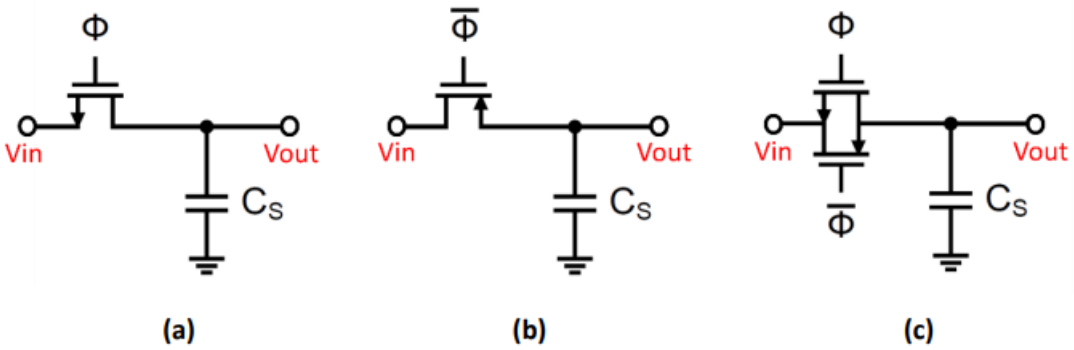


Figure 41. Basic sampling circuits (a) NMOS switch, (b) PMOS switch, (c) CMOS Transmission gate

$$R_{ON} = \frac{1}{\mu_n \cdot C_{OX} \cdot W/l_L \cdot (V_{GS} - V_{TH})} = \frac{1}{\mu_n \cdot C_{OX} \cdot W/_L \cdot ((V_{DD} - V_{IN}) - V_{TH})}$$
$$Q_{CH} = W \cdot L \cdot C_{OX} \cdot (V_{GS} - V_{TH}) = W \cdot L \cdot C_{OX} \cdot \left((V_{DD} - V_{IN}) - V_{TH}\right) \quad (5.1)$$
$$\Delta V_{OUT} = V_{CLK} \cdot \frac{W \cdot C_{OV}}{W \cdot C_{OV} + C_S}$$

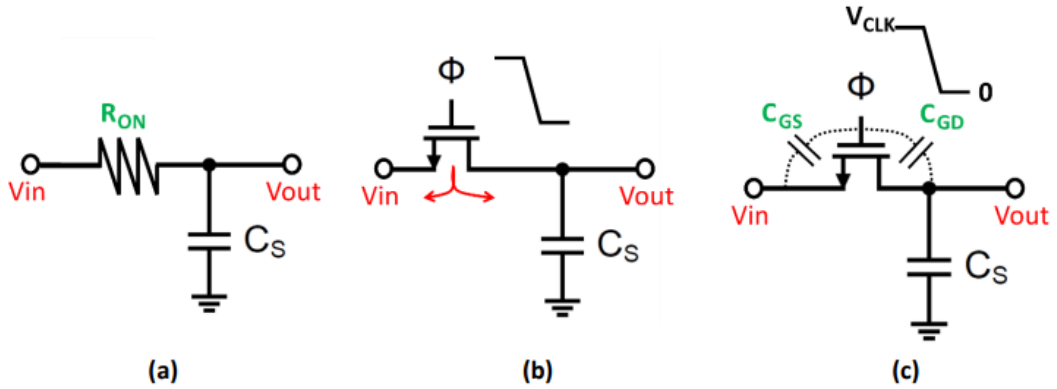


Figure 42. Non-idealities in MOSFET switches (a) input-dependent R_{ON}, (b) Charge injection, (c) Clock feedthrough

The bootstrapped switch help mitigate some of these non-idealities by keeping the V_{GS} of the switch fixed during the sampling phase. In the basic illustration in Fig. 16 (a), Φ2 switches are ON during the hold phase, turning the main switch MNSW completely off by connecting its gate to ground and charging the capacitor COFFSET to a voltage of $V_C = V_{DD} – V_{SS}$ [8]. During the sampling phase, Φ1 switches are ON while Φ2 switches are OFF, causing the capacitor to act as a constant battery fixing V_{GS} to be equal to V_C. Fig. 43 (b) shows how the gate voltage Vg and the source voltage Vs of MNSW are bootstrapped allowing them to change together. Fixing V_{GS} suppresses the distortion due to dependence of R_{ON} and Q_{CH} on the input signal. Also, the width W of MNSW does not need to be large to further reduce R_{ON}'s effect, which in turn helps reducing clock feedthrough as well since the parasitic caps are smaller with smaller W.

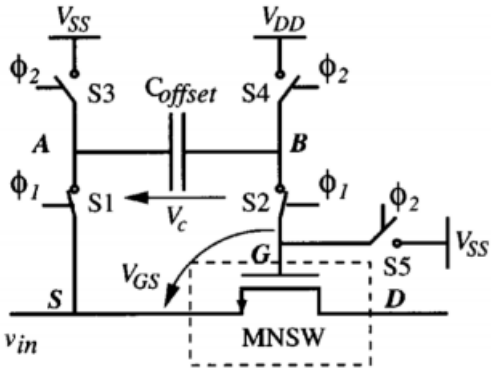


Figure 43: Basic bootstrapedswitch[8]

3.4.2 Double Bootstrap circuit

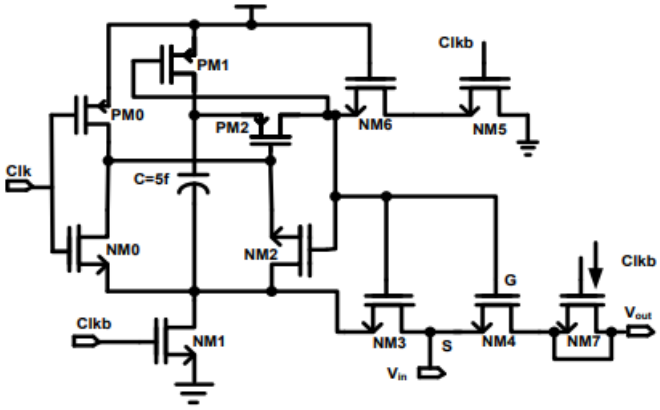


Figure 44: The double bootstrap circuit [8]

The proposed design includes a dummy switch connected at the output of the bootstrap switch, as shown in Figure 44. When Clkb is in a high state, NM1 is turned "ON" to store the voltage Vdd in capacitor C using PM1 and NM1. This capacitor serves as a storage capacitor between the gate voltage Vgs of MOSFET NM4. MOSFETs PM2 and NM3 are used to isolate capacitor C from NM4 during the charging process.

When Clk is in a high state, NM0 is turned "ON," pulling down the gate voltage of M2 and turning PM2 "ON." This enables the charge stored in capacitor C to flow into the gate of MOSFET NM4. NM3 is employed to maintain the gate voltage of NM4 at the supply voltage Vdd, thereby keeping Vgs of NM4 constant. Specifically, when the input voltage Vgs of NM4 is Vdd, the gate voltage will be 2Vdd.

To prevent non-linearity errors, a dummy switch is connected between the bootstrap switch and the output in this sample and hold circuit. The clock booster outputs Q1 and Q2 are connected to Clk and Clkb of the proposed bootstrap circuit to control the output voltage swing.

When NM4 transitions to the OFF state, half of the channel charge moves towards switch NM7, while the other half moves towards the input Vin. The channel charge per unit area of the inverted channel can be expressed as;

$$Q_1'(y) = C'ox.(VGS - VTHN) \quad (6)$$

The total charge in the channel is then multiplied by the area of the channel thus giving;

$$Q_1(y) = C'ox.\ W.\ L.\ (VGS - VTHN) \quad (7)$$

Therefore, the change in voltage across the Cload of the NMOS switch is;

$$\Delta V_{load} = -\frac{C'ox.W.L.(VDD-Vin-VTHN)}{2Cload} \quad (8)$$

The clock swings between Vdd and GND and by substituting the Vth, then V_{load} is;

$$\Delta V_{load} = \frac{C'ox\ .W.L.\left(VDD-Vin-\left[VTHN0+\gamma\sqrt{|2Vfp|+Vin}\right]\right)}{2Cload} - \frac{\gamma\sqrt{|2Vfp|}}{2Cload} \quad (9)$$

To mitigate the non-linear voltage change across Cload caused by the threshold voltage, a solution involves connecting an NMOS switch with the source and drain shorted. By short-circuiting the source and drain of the MOSFET NM7, a channel can still be established by applying sufficient voltage at the gate control. This arrangement ensures that the charge injected by NM4 is balanced by the charge induced by NM7. When NM7 is in the OFF state, the total charge is induced in both directions. Since NM7 has its source and drain shorted and Vin represents a low impedance node, the total charge is injected into NM4, aligning with the input voltage Vin. Consequently, the non-linearity errors stemming from clock feedthrough and charge injection are minimized. As a result, the proposed bootstrap design, along with the inclusion of a dummy switch in the full differential structure of the sample and hold architecture, demonstrates improved linearity.

3.5 Capacitive DAC

3.5.1 Single-ended capacitive DAC

Considering a 3-bit SAR ADC, shown in figure 44. The common mode voltage V_{CM} is assumed to be zero for ease of calculation.

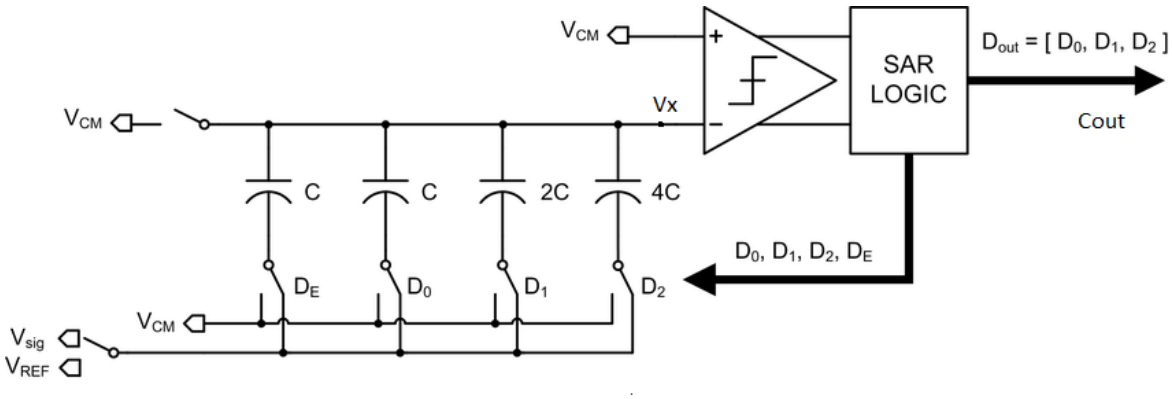


Figure 44: Capacitive DAC for a 3-bit SAR ADC[108]

At the start of the conversion operation, the input signal is sampled to the bottom plates of the capacitors using the D switches, while the upper plate is connected to V_{CM}. The total charge stored on the capacitor is equal to V_{IN}multiplied by the sum of the capacitors. The voltage and the charge at the top plates V_x are shown in the equation 10 and 11.

During sampling phase:

$$V_X = V_{CM} = 0 \qquad (10)$$

$$Q_X = -V_{\text{sig}} \,.\, 8C \qquad (11)$$

After the sampling phase the top plate of the capacitors is disconnected from V_{CM}, while the bottom plate is disconnected from V_{IN} and is charged according to the digital code from the SAR logic. In the first comparison the MSB is set to 1 making the DAC code 100 initially. With the charge distribution and voltage division, V_X changes as shown in equation 13 and

compared to V_{CM}. This is equivalent to V_{IN} being compared to ½ Vref (V_X<0), the comparator outputs a 1, otherwise the comparator gives a 0.

Comparison 1 (DAC=100):

$$\Delta V = \frac{4\,C}{4C + 2C + C + C} \tag{12}$$

$$V_X = -V_{IN} + \Delta V = -V_{IN} + \frac{1}{2}(V_{REF}) \tag{13}$$

In the next conversion, the MSB will take the value of the comparators output D2 and the MSB-1 bit is set to 1. V_{IN} now is compared to either the upperhalf of V_{REF} if D2 = 1 or the lower half of V_{REF} id D2 = 0. After this comparison, the MSB-1 bit takes the value of the comparator D1 and MSB-2 bit is set to 1. After N=3 comparisons, the SAR ADC outputs D2D1D0 as the final binary code that translates to the voltage level VDAC given in equation 16. Figure 45. shows the change in the node voltages of the capacitors in each stage of the conversion process. The binary search process is shown in Fig.46. The binary tree in Fig.47. shows the all the possible outcomes of this 3-bit SAR system. The stages of this binary tree can be extended to N stages for an N-bit SAR ADC.

Comparison 2 (DAC=D210):

$$V_{DAC} = \frac{(D2\,.4C) + 2C}{4C + 2C + C + C} \tag{14}$$

$$V_X = -V_{IN} + V_{DAC} = -V_{IN} + \frac{D2}{2}V_{REF} + \frac{1}{4}V_{REF} \tag{15}$$

Comparison 3 (DAC=D2D11):

$$V_{DAC} = \frac{(D2\,.4C) + (D1\,.2C) + 1C}{4C + 2C + C + C} \tag{16}$$

$$V_X = -V_{IN} + V_{DAC} = -VIN + \frac{D2}{2}V_{REF} + \frac{D1}{4}V_{REF} + \frac{1}{8}V_{REF} \tag{17}$$

Final output (DAC=D2D1D0) is equivalent to:

$$V_{DAC} = \frac{D2}{2}V_{REF} + \frac{D1}{4}V_{REF} + \frac{D0}{8}V_{REF} \tag{18}$$

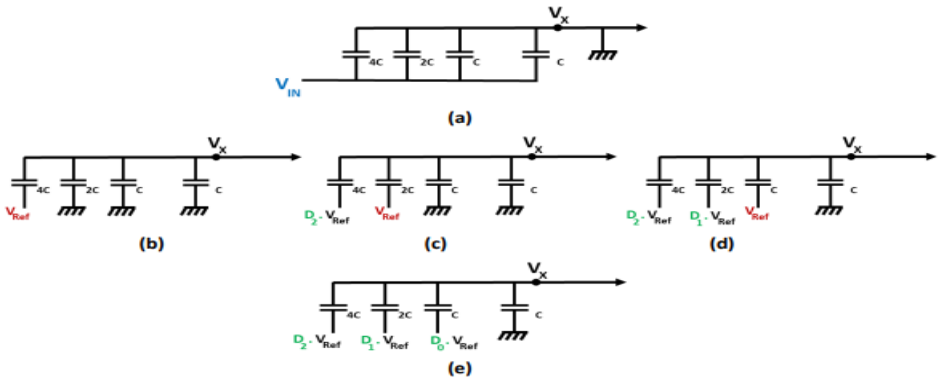


Figure 45: Node voltages of the DAC capacitors for each stage (a) Sampling phase, (b) Comparison 1, (c) Comparison 2, (d) Comparison 3, (e) Final binary output

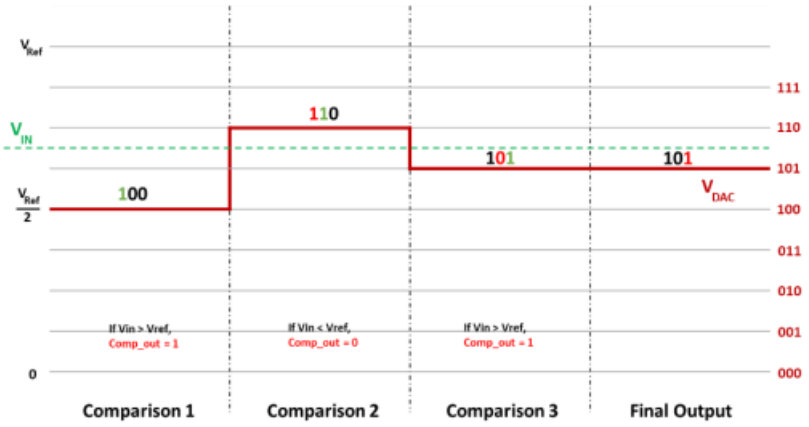


Figure 46: Binary search process in the 3-bit SAR system

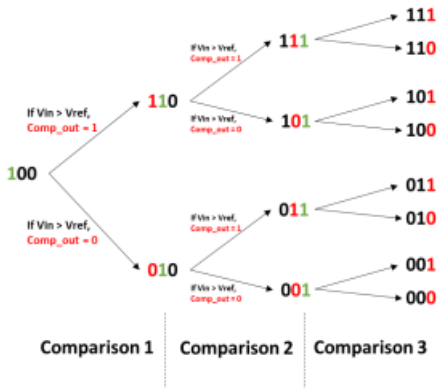


Figure 47: Binary tree showing all the possible outputs of a 3-bit SAR ADC

3.5.2 Differential SAR Architecture

The idea presented in the previous section can be extended to a differential configuration. Figure 48. shows an 8-bit differential capacitive DAC. In the differential DAC, negative and the positive references are used as defined in equations 10 and 11, respectively. The 2 input nodes to the comparator are compared in each iteration, so if ($V_{XP} - V_{XN}$) > 0, then the comparator will output a 1, otherwise, it produces a 0. The differential configuration has many advantages over the single-ended configuration like better common-mode rejection ratio (CMRR), the reduction of even harmonic distortion, and the doubling of input voltage range, but at the expense of larger layout area since most of the components are doubled for the differential configuration.

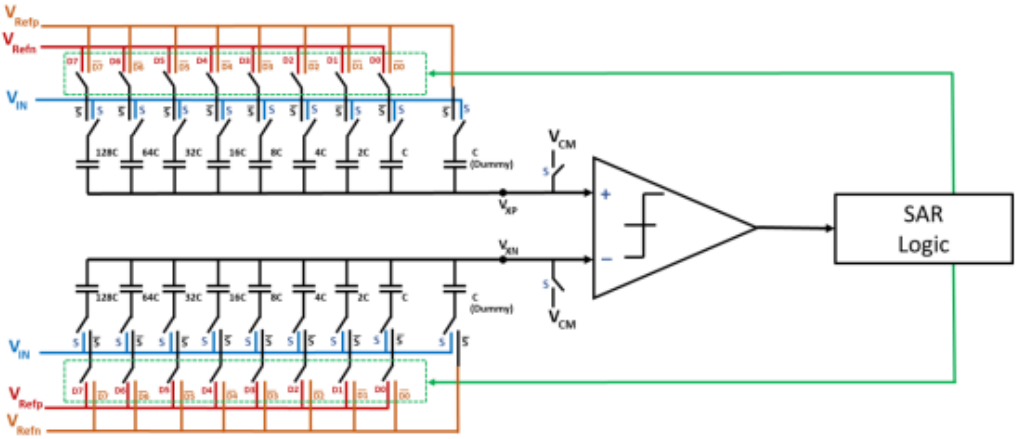


Figure 48: Differential capacitive DAC of an 8-bit SAR ADC

$$V_{Refn} = V_{CM} - \frac{VRef}{2} \tag{19}$$

$$V_{Refp} = V_{CM} + \frac{VRef}{2} \tag{20}$$

3.5.3 Split binary-weighted capacitive array

SAR ADCs rely on the utilization of the binary search algorithm, which can be implemented through the charge redistribution concept involving capacitors arranged in a binary-weighted pattern. This concept was initially introduced by McCreary and Gray in 1975. Figure 49 provides an illustration of the commonly used DAC implementation in SAR ADCs. In the diagram, N represents the resolution of the Analog-to-Digital Converter (ADC), where vrefp denotes the high reference voltage node (typically VDD), vrefn represents the low reference voltage node (typically ground), and Cu represents the capacitance value of the unit capacitor. During the reset phase, the bottom plates of all capacitors are connected to vrefn, while the top plates are connected to a reset voltage (in this case, vrefn). In the conversion phase, each bottom plate has the option to either remain connected to vrefn or switch to vrefp, resulting in different voltage levels at vdac depending on the configuration of the switches. The switches are controlled by signals si, where si = 0 connects the capacitor to vrefn, and si = 1 connects it to vrefp.Therefore, the voltage at vdac can be expressed as the sum of the product of each switch Si and the corresponding voltage increment ((VREFP - VREFN)/(2N-i)) over the range of i from 0 to N-1.

$$V_{DAC} = \sum_{i=0}^{N-1} \mathrm{Si} \cdot \left(\frac{VREFP - VREFN}{2N - i} \right) \tag{21}$$

While the binary-weighted capacitor array topology has been widely adopted in mixed-signal IC design, it poses challenges in terms of cost and physical implementation as the resolution (N) of the ADC increases. The number of elements in the capacitor array grows exponentially

with N, making the circuit costly and complex to fabricate, even when using the smallest available device in the chosen technology.

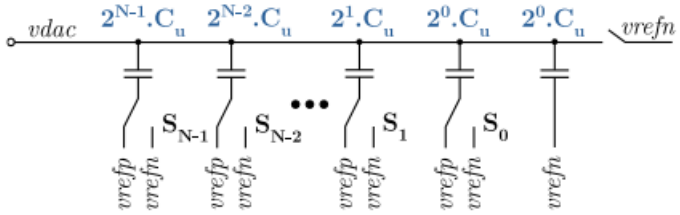


Figure 49: Binary-weighted capacitive array

As depicted in Figure 50, in order to achieve a reduction in the size of the capacitor array, the split binary-weighted capacitive array architecture employed with a bridge capacitor Cbridge. This architecture splits the capacitive DAC into two halves while maintaining the binary-weighted arrangement. A sub-DAC consists of J elements (capacitor plus switch), and a main DAC consists of M elements. The series combination of Cbridge and the sub-DAC provides capacitance values that are referenced by the main DAC, ranging from 2^{-J}*Cu up to Cu, depending on the binary code. To achieve this, the bottom plates of Cbridge and the capacitor array of the sub-DAC, which are connected together, must have a combined capacitance value of Cu. However, in general, this results in a value of Cbridge that is not an exact integer multiple of Cu.

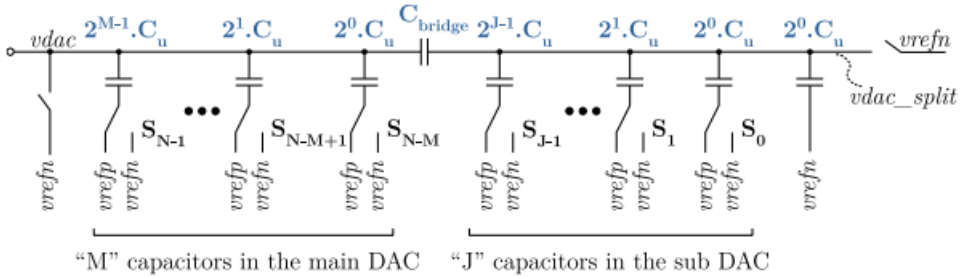


Figure 50: The array of Split capacitor

A practical realization of the split technique is shown in Figure 51.

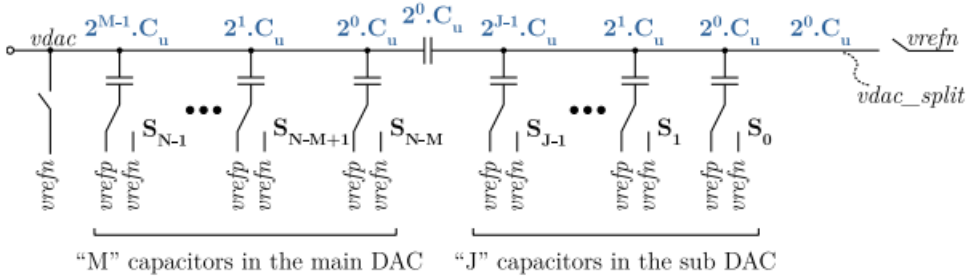


Figure 51: Practical implementation of split capacitor Array

In this particular design, Cbridge is replaced by Cu, and the capacitor corresponding to least significant bit (LSB) of the sub DAC (the rightmost capacitor) is eliminated to compensate for the voltage scaling. This modification is aimed at avoiding the use of a fractional capacitance

value, which in turn improves the layout and the matching of the capacitor array. However, it should be noted that this change leads to an increase in gain error. For low-power applications, the value of Cu is chosen to be as small as possible. The main limitations on its value are the thermal noise introduced by the switches and the mismatch between capacitors. The thermal noise, as discussed in subsection 3.2.3, imposes a minimum value of Cu to ensure that the KTC noise in the sample and hold circuits, with a hold capacitor of 2^M * Cu (equivalent DAC capacitance), is less than the quantization noise of the converter. The mismatch limitation occurs due to the inherent variability in the fabrication process.

Actual capacitance of the fabricated CU device often deviates from its nominal value, resulting in DNL (differential nonlinearity) and INL (integral nonlinearity) errors. The work conducted indicates that in the split binary-weighted capacitive array architecture, the mismatch in the main DAC is the primary factor contributing to the worst-case DNL error. However, an analysis of INL is not performed as the DNL error is considered more significant. The worst-case standard deviation of DNL is determined by factors such as:

$$\sigma_{DNL,MAX} = \left(\left(\sqrt{2M-1}\right)\left(\frac{\sigma u}{Cu}\right)\right) LSB', \qquad (21a)$$

where LSB' = $V_{REF}/2^M$.

When analysing the effective fabrication characteristics of Metal-Insulator-Metal (MIM) capacitors to estimate the yield, certain parameters can be obtained through direct measurement or calculation. In the case of MIM capacitors, these parameters are interrelated as follows:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K\sigma}{\sqrt{AC}}$$

$$C = K_C \cdot A_C \qquad (22)$$

here K_C is the capacitor density,

A_C is the capacitor area, K_σ is the matching coefficient and

$\sigma(\Delta C/C)$ is the standard deviation of the difference of two identical capacitors, normalized to their absolute value C.

Given that the standard deviation of a single capacitor is smaller than the standard deviation of the difference between two capacitors by a factor of √2, we can express this as follows:

$$\frac{\sigma_u}{C_U} = \frac{K_\sigma}{\sqrt{2}\sqrt{AC}}. \qquad (23)$$

where σ_u stands for standard deviation of the value of C_u. Hence, the minimum value of Cu due to mismatch restrictions is valued by combining the previous equations with the limitation $3\sigma_{DNL,MAX} < 1/2LSB$ to guarantee monotonicity, leading to

$$C \geq 9 \cdot (2^M - 1) \cdot 2^{2(N-M)} \cdot K_\sigma^2 \cdot K_C \qquad (24)$$

Note that this limitation can be relaxed by half when the circuit is made differential, because the signal range is doubled although the mismatch error is only amplified by a factor of √2.

3.6 Comparator

3.6.1 Two Stage Dynamic Comparator

This comparator is fast and energy efficient. It has lesser input referred offset voltage. An sample of two-stage comparator is shown in Figure 52.

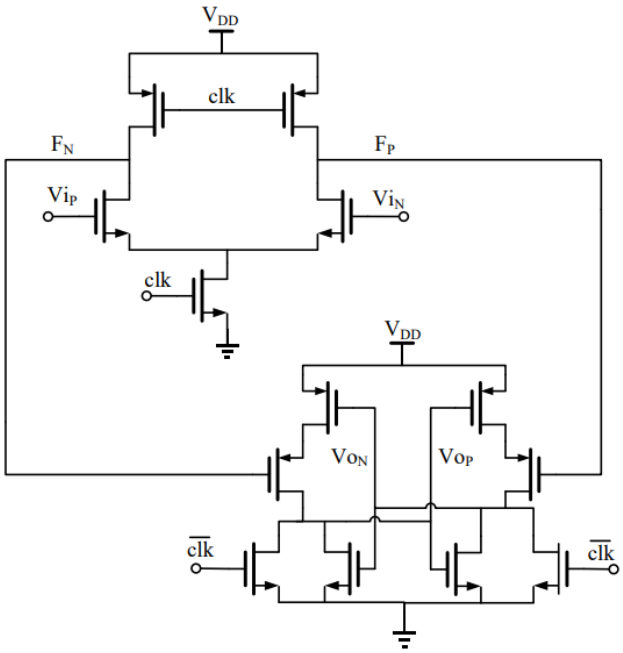


Figure 52: Schematic of Comparator

The single-stage dynamic comparator is made of two distinct stages: a voltage amplifier and a latch. During the reset phase, when the clock signal is low, the voltage amplifier stage charges the F nodes to VDD using PMOS transistors, while simultaneously disabling the latch stage. At this stage, the output nodes are reset to zero through the NMOS switches in the latch stage. This architecture offers a combination of power efficiency and high speed, primarily due to the low capacitance at the F nodes, which is mainly caused by the drain diffusion capacitances of the NMOS and PMOS transistors connected to these nodes. Upon the transition of the clock signal to a high state during the regeneration phase, the tail transistor is activated, initiating amplification in the voltage amplifier stage. The F nodes begin to discharge through the differential input pair transistors within the voltage amplifier stage. The rate of discharge of these nodes is directly proportional to the input voltage. Once either of the output nodes (F nodes) of the voltage amplifier stage reaches a level close to the threshold voltage (Vth) of the input transistors in the latch stage, these transistors are switched on, leading to the onset of amplification in the latch stage. Consequently, the output voltage gradually increases, triggering a positive feedback system that generates high and low voltage levels during the regeneration phase.

3.6.2 Equivalent Input Noise of the First Stage

The performance of the comparator, particularly its noise characteristics and energy efficiency, is heavily influenced by the voltage amplification in the first stage. The primary source of noise

in the first stage is the input pair. The thermal noise of a single MOS transistor can be approximated by an equivalent noise resistor .$R_{\mathrm{n,MOST}}$ at its gate

$$R_{n,\mathrm{MOST}} \approx \frac{\gamma}{gm_{\mathrm{MOST}}} \tag{25}$$

here the noise excess factor γ is almost 1. The equivalent noise resistor of each input transistor appears in series with the DAC voltage. The equivalent noise resistor of the input pair $R_{\mathrm{n,FS}}$ is given by

$$R_{n,FS} \approx \frac{2}{gm_{\mathrm{MOST}}} \tag{26}$$

The first stage of the comparator integrates the input signal and the noise from the equivalent noise resistor. The input-equivalent integrated noise is approximated by

$$\sigma_{\mathrm{v}} \approx \sqrt{4 \cdot k \cdot T \cdot R_{n,FS} \cdot \mathrm{NBW}} \approx \sqrt{4 \cdot k \cdot T \cdot \frac{2}{gm_{\mathrm{MOST}}} \cdot \mathrm{NBW}}. \tag{27}$$

The noise bandwidth (NBW) for noise integrated over integration time T_{int} is

$$\mathrm{NBW} = \frac{1}{2 \cdot T_{\mathrm{int}}} \tag{28}$$

A more comprehensive exploration of narrow-bandwidth (NBW) in amplifiers is presented in [12]. Integration is examined as a specific scenario, particularly in the context of an amplifier that has not yet reached a settled state, yielding the same mathematical expression.

In the second stage, sampling occurs on the output voltage of the first stage once the common mode voltage on nodes FP and FN has experienced an approximate change of the input pair's threshold voltage, $V_{\mathrm{threshold.}}$. The current through every input transistor in the first stage I_{MOST} is integrated on the capacitances

C_{FP} and C_{FN} at nodes FP and FN. The integration time T_{int} can be approximated by

$$T_{\mathrm{int}} \approx \frac{V_{\mathrm{threshold}} \cdot C_{\mathrm{FP}}}{I_{\mathrm{MOST}}} \approx \frac{V_{\mathrm{thresbold}} \cdot C_{\mathrm{FN}}}{I_{\mathrm{MOST}}}. \tag{29}$$

Inserting (27) and (28) into (29) gives

$$\sigma_{\mathrm{V}} \approx \sqrt{4 \cdot k \cdot T \cdot \frac{1}{V_{\mathrm{threshold}} \cdot C_{\mathrm{FP}}} \cdot \frac{I_{\mathrm{MOST}}}{gm_{\mathrm{MOST}}}}. \tag{30}$$

To achieve energy-efficient amplification, the input pair is biased in weak inversion. The transconductance of a MOS transistor operating in weak inversion is dependent on the subthreshold slope. Based on simulations conducted for the 65nm process, the transconductance can be approximated as follows:

$$gm_{\mathrm{MOST}} \approx \frac{I_{\mathrm{MOST}}}{2 \cdot V_{\mathrm{thermal}}} \tag{31}$$

where V_{thermal} is

$$V_{\mathrm{thermal}} = \frac{k \cdot T}{q} \tag{32}$$

In a SAR ADC based on a charge-redistribution DAC, the thermal noise from the DAC switches sampled by the comparator can potentially also be significant. The equivalent noise resistor of the DAC $R_{\mathrm{n,DAC}}$ is determined by the on-resistances of the switches. The first stage of the comparator is relatively slow because it is biased in weak inversion. This makes the NBW relatively small and at the same time its equivalent noise resistor $R_{\mathrm{n,FS}}$ relatively large, therefore

$$R_{\mathrm{n,FS}} \gg R_{\mathrm{n,DAC}} \tag{33}$$

As a consequence $R_{\mathrm{n,DAC}}$ contributes relatively little noise. Inserting into gives

$$\sigma_{\mathrm{V}} \approx \sqrt{\frac{k \cdot T}{C_{\mathrm{FP}}}} \cdot \sqrt{8 \cdot \frac{V_{\mathrm{thermal}}}{V_{\mathrm{threshold}}}}. \tag{34}$$

For example at $T = 300\mathrm{K}$ with $C_{\mathrm{FP}} = 10\mathrm{fF}$ and $V_{\mathrm{threshold}} = 0.4\mathrm{V}$, the value of σ_{V} is around 0.5 mV. Based on a required maximum noise level, the essential minimum value of C_{FP} and C_{FN} can be approximated by

$$C_{\mathrm{FP}} = C_{\mathrm{FN}} \geq \frac{k \cdot T}{\sigma_{\mathrm{V}}^2} \cdot 8 \cdot \frac{V_{\mathrm{thermal}}}{V_{\mathrm{threshold}}} \tag{35}$$

A level of 0.5 mV is considered appropriate as it aligns the thermal noise of the comparator with the quantization noise of the ADC, placing them within the same magnitude. Here comparator C_{FP} and C_{FN}mostly consist of parasitic MOST capacitances and are somewhat larger than 10 fF each. The energy dissipation of the first stage depends mostly on $C_{\mathrm{FP}}$and C_{FN}being discharged and charged for every comparison.

3.7 SAR logic

The proposed SAR logic shown in Figure 52 is based on the SAR logic used for a synchronous SAR ADC [109]. The SAR logic block consists of 2 rows of D-flipflops, the sequencer register and the code register. The sequencer register keeps track of the sequence by keeping the output of one flipflop (FF) only equals to 1, while the outputs of the rest of the flipflops equal to 0. This 1 (or hot code) moves from one FF to the next at each rising edge of the "clk_SAR" (at each new iteration) and circulates through the register like how a one-hot-code ring counter operates. The hot code sets the bit being compared to 1, by triggering the "set" input of the corresponding FF in the code register. When the "set" of a FF in the code is triggered, 18 it outputs a 1 for its corresponding bit and also triggers the clock for the previous FF so that the previous bit would take the value of the comparator's decision. At the end of the end of the conversion process, the code register holds the final DAC code and an EOC signals the output stage to take that code as the result of the ADC conversion. Figure53 shows the schematics of the proposed SAR logic. The state table of the SAR logic block showing the whole 8-bit conversion process is presented in Table 9. The clock driving this block is "clk_SAR" coming from the internal clock generator, and the reset pin of this block is connected to "clk_sample" so that the outputs of all the FFs are reset during the sampling phase. For the 8-bit system, there are 8 main FFs in each of the sequencer and the code registers, in addition to 1 extra FF at beginning of the sequencer register to load the hot code during the sampling phase, and 2 extra

FFs at the end of the registers to generate the EOC signal along with the final output code. The output of the comparator is connected to the D input of the main FFs of the code register. Since the capacitive DAC operates differentially, both the complementary outputs of the FFs are sent to the DAC.

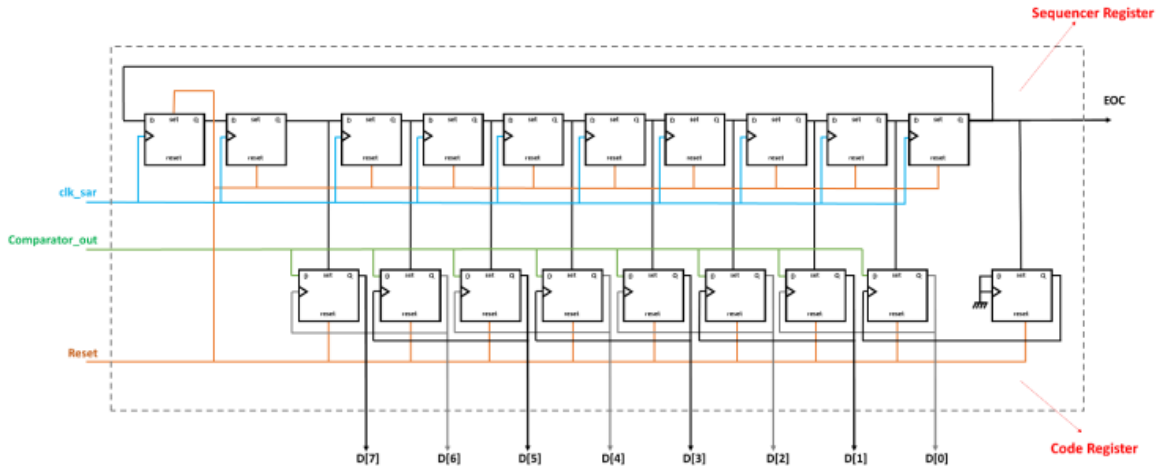


Figure 53: Block diagram of the SAR Logic

Table 9:SAR Logic States Table

		Sequencer Register Outputs										Code Register Outputs									Comparator Output
		DFF_init	DFF7	DFF6	DFF5	DFF4	DFF3	DFF2	DFF1	DFF0	DFF_end	DFFc7	DFFc6	DFFc5	DFFc4	DFFc3	DFFc2	DFFc1	DFFc0	DFFc_end	Comp_out
0	Sampling	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X
1	Comparison 1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	B7
2	Comparison 2	0	0	1	0	0	0	0	0	0	0	B7	1	0	0	0	0	0	0	0	B6
3	Comparison 3	0	0	0	1	0	0	0	0	0	0	B7	B6	1	0	0	0	0	0	0	B5
4	Comparison 4	0	0	0	0	1	0	0	0	0	0	B7	B6	B5	1	0	0	0	0	0	B4
5	Comparison 5	0	0	0	0	0	1	0	0	0	0	B7	B6	B5	B4	1	0	0	0	0	B3
6	Comparison 6	0	0	0	0	0	0	1	0	0	0	B7	B6	B5	B4	B3	1	0	0	0	B2
7	Comparison 7	0	0	0	0	0	0	0	1	0	0	B7	B6	B5	B4	B3	B2	1	0	0	B1
8	Comparison 8	0	0	0	0	0	0	0	0	1	0	B7	B6	B5	B4	B3	B2	B1	1	0	B0
9	Final Output	0	0	0	0	0	0	0	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0	1	X
											EOC										

3.8 Output DAC

The ideal output DAC used for evaluation. This block consists of 8 binary-weighted ideal voltage-controlled voltage sources (VCVS). They are stacked on top of each other to be summed together to represent the analog output given by equation 36. The final VCVS at the right is to correct the normalized analog output by multiplying by the right gain equal to the peak-to-peak swing of the input signal and shift the minimum level to VRefn of the system.

$$VOUT = \frac{1}{2^8}.(D7.2^7 + D6.2^6 + D5.2^5 + D4.2^4 + D3.2^3 + D2.2^2 + D1.2^1 + D0.2^0) \qquad (36)$$

3.9 Specifications for the Design

If the neuromorphic chip is specifically designed for vision applications, such as image processing or computer vision tasks, the ADC specifications may need to be tailored accordingly. Here are some additional considerations for the ADC specifications in a neuromorphic vision chip:

1. **Resolution:** Since image processing often requires precise representation of pixel values, a higher resolution ADC may be desirable. Considering specifications in the range of 10 bits to 16 bits to capture fine details in the images.
2. **Sampling Rate:** The sampling rate should be chosen based on the temporal characteristics of the visual data. Consider higher sampling rates to capture fast-changing scenes or videos, while lower rates may be sufficient for static images. Typical values can range from a few kilosamples per second (KSPS) to several megasamples per second (MSPS).
3. **Power Consumption:** Energy efficiency is crucial for vision applications, especially for portable or battery-operated devices. Aim for low-power ADC designs that minimize power consumption while maintaining the required performance. Target power consumption values should typically be in the range of a few milliwatts (mW) or lower.
4. **Effective Number of Bits (ENOB):** Higher ENOB values are desirable in vision applications to accurately capture image details and maintain the fidelity of visual information. Considering ENOB specifications in the range of 10 bits to 14bits.
5. **Signal-to-Noise Ratio (SNR):** In vision applications, a higher SNR is often desired to preserve image quality and reduce the impact of noise. Aim for SNR values of 60 dB or higher to ensure clear and accurate image representation.
6. **Spurious-Free Dynamic Range (SFDR):** SFDR is important in vision applications to minimize spurious artifacts and maintain image integrity. Target SFDR values of 70 dB or higher to ensure effective rejection of unwanted signals or interference.
7. **Linearity:** To accurately represent the image data, aim for low INL and DNL values. Specify INL values below ±1 LSB and DNL within ±0.5 LSB or better.
8. **Input Range:** The input range should be selected to accommodate the full dynamic range of pixel intensities in the visual data. Consider bipolar input ranges such as ±1 V or ±2 V to handle both positive and negative pixel values.
9. **Voltage Reference:** The voltage reference should provide stable and accurate reference voltages to ensure precise ADC conversions. Specify reference accuracies around 1% of the full-scale range for reliable performance.

These specifications are geared towards a neuromorphic vision chip, considering the specific requirements of vision processing and image analysis. However, it's important to further refine

these specifications based on the precise application and system requirements for the neuromorphic vision chip.

Table 10: Required Specifications

Parameter	Value
Resolution	10 bits
Sampling Rate	20 MS/s
SINAD	<60 dB
SFDR	<60 dB
ENOB	8.5 – 9 bits
Total Power	<1 mW

Chapter 4

Implementation of SAR ADC and Performance Evaluation

4.1 Implementation of SAR ADC

Initially, a proof-of-concept simulation of an 8-bit SAR ADC converter was conducted using VerilogA modeling. Subsequently, each block of the converter was replaced with its transistor-level design. The initial design focused on an 8-bit architecture but was later transitioned to a 10-bit architecture.

In this study, a double bootstrapped sample and hold circuit was implemented for both designs. It was determined that the double bootstrapped switch, discussed in this chapter, outperformed the normal bootstrapped switch described in the previous chapter. Additionally, a two-stage dynamic comparator was chosen over a single-stage comparator for improved performance. The SAR controller, which includes a sequencer and a shift register, was selected along with SAR logic type 1 from Chapter 3 to fulfill the low-power requirements. Lastly, a charge redistribution DAC was utilized.

Moving forward, the subsequent section provides an overview of the design of the D/A converter.

4.2 Design of an 8-Bit SAR ADC in VerilogA

Current section, the VerilogA codes used in the ideal models for the asynchronous SAR ADCs are presented.

4.2.1 Sample-And-Hold Code:

```
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_SampleAndHold(clk,vin,vmin,vout);
parameterreal vtrans=0.55;
parameterrealdelay = 0;
parameter real ttime = 60p;
parameter real clk_threshold = 0.55;          //vdd is 1.1v
input clk,vin,vmin;
output vout;
electrical vout,vin,vmin,clk;
real v;
analog begin
```

```
        // Sampling Phase (+1 is for rising edge, -1 is for falling edge)
        @(cross(V(clk) - clk_threshold, +1))
                v = V(vin);
        V(vout) <+ transition(v,delay,ttime);
end
endmodule
```

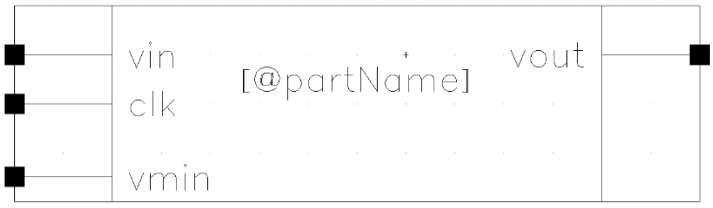


Figure 54: Sample and hold symbol

4.2.2 Clocked Comparator:

```
// VerilogA for ClockedComparator
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_ClockedComparator(dout,vref,vin,clk);
parameter real clk_th=0.55;
parameter real delay = 0;
parameter real ttime = 60p;
input vin,vref,clk;
output out, out_b;
electrical out,out_b,vref,vin,clk;
real d_result, d_result_b;
analog begin
        @(cross(V(clk) - clk_th, +1)) begin
                if(V(vin) > V(vref)) begin
                        d_result = 1;
                        d_result_b = 0;
                end
```

```
            else begin
                d_result = 0;
                d_result_b = 1;
            end
        end
        @(cross(V(clk – clk_th, -1)) begin
            d_result = 0;
            d_result_b = 0;
        end
        V(out) <+ transition(d_result,delay,ttime);
        V(out_b) <+ transition(d_result_b,delay,ttime);
end
endmodule
```

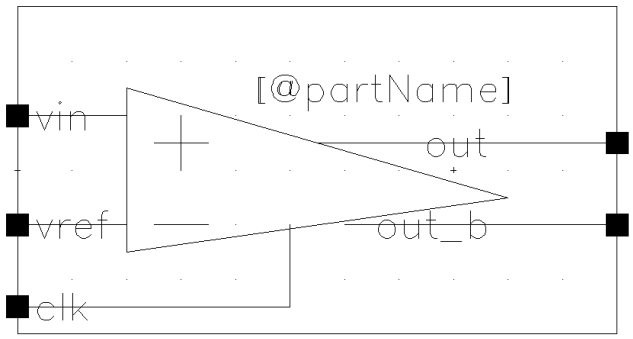


Figure 55: Comparator symbol

4.2.3 Output Register 8- bit

```
// VerilogA for SAR_VerilogA, VerilogA_Register_8bit, veriloga
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_Register_8bit(clk,in0,in1,in2,in3,in4,in5,in6,in7,out0,out1,out2,out3,out4,out5,out6,out7,vdd,vss);
parameter real vtrans=0.55;
parameter real delay = 0;
```

```
parameter real ttime = 1p;
parameter real clk_threshold = 0.5;
inout vdd,vss;
input clk,in0,in1,in2,in3,in4,in5,in6,in7;
output out0,out1,out2,out3,out4,out5,out6,out7;
electrical clk,in0,in1,in2,in3,in4,in5,in6,in7,out0,out1,out2,out3,out4,out5,out6,out7,vdd,vss;
real d_0,d_1,d_2,d_3,d_4,d_5,d_6,d_7;
analog begin
        @(cross(V(clk) - clk_threshold, +1))
        begin
                d_7 = V(in7);
                d_6 = V(in6);
                d_5 = V(in5);
                d_4 = V(in4);
                d_3 = V(in3);
                d_2 = V(in2);
                d_1 = V(in1);
                d_0 = V(in0);
        end
        V(out7) <+ transition(d_7,delay,ttime);
        V(out6) <+ transition(d_6,delay,ttime);
        V(out5) <+ transition(d_5,delay,ttime);
        V(out4) <+ transition(d_4,delay,ttime);
        V(out3) <+ transition(d_3,delay,ttime);
        V(out2) <+ transition(d_2,delay,ttime);
        V(out1) <+ transition(d_1,delay,ttime);
        V(out0) <+ transition(d_0,delay,ttime);
end
endmodule
```

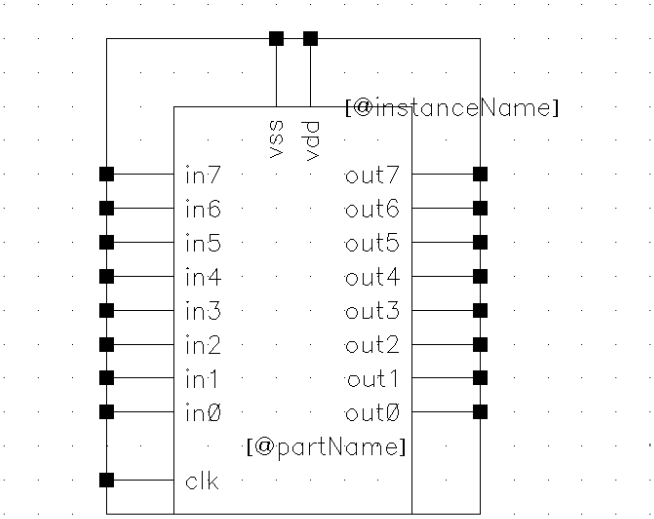


Figure 56: SAR Output Register

4.2.4 DAC (8bit)

```
// VerilogA for VerilogA_DAC_8bit
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_DAC_8bit(d0,d1,d2,d3,d4,d5,d6,d7,vout,vdd,vss,vmin,vmax);
parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 1p;
inout vdd,vss;
input d0,d1,d2,d3,d4,d5,d6,d7;
input vmin, vmax;
output vout;
electrical vout,vdd,vss,d0,d1,d2,d3,d4,d5,d6,d7,vmin,vmax;
real result,d_0,d_1,d_2,d_3,d_4,d_5,d_6,d_7;
analog begin
        d_7 = V(d7)*128;
        d_6 = V(d6)*64;
        d_5 = V(d5)*32;
```

```
d_4 = V(d4)*16;
d_3 = V(d3)*8;
d_2 = V(d2)*4;
d_1 = V(d1)*2;
d_0 = V(d0)*1;
result = ((d_7+d_6+d_5+d_4+d_3+d_2+d_1+d_0) *((V(vmax)-V(vmin))/(256))) + V(vmin) ;
V(vout) <+ transition(result,delay,ttime);
end
endmodule
```

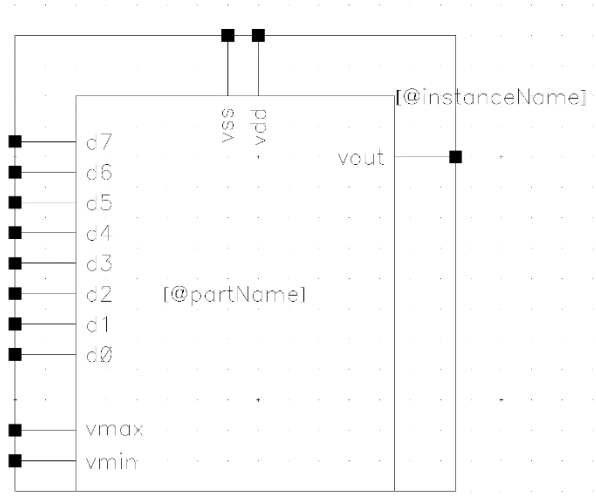


Figure 57: DAC Symbol

4.2.5 D-Flipflop:

```
// VerilogA for SAR_VerilogA, VerilogA_D_FlipFlop, veriloga
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_DFlipFlop(D,clk,Q,Qb,set,reset,vdd,vss);
parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 1p;
parameter real clk_threshold = 0.5;
inout vdd,vss;
```

```
input D,clk,set,reset;
output Q,Qb;
electrical D,clk,Q,Qb,set,reset,vdd,vss;
real d_0,d_0b;
analog begin
        @(cross(V(set) - vtrans, +1)) begin
                d_0 = 1;
                d_0b = 0; end
        @(cross(V(reset) - vtrans, +1)) begin
                d_0 = 0;
                d_0b = 1; end
        @(cross(V(clk) - clk_threshold, +1))
        begin
        //if((V(set) < vtrans) && (V(reset) < vtrans) ) begin
                if(V(D) > vtrans) begin
                d_0 = 1; d_0b = 0; end
                else begin
                d_0 = 0; d_0b = 1; end
        end
        V(Q) <+ transition(d_0,delay,ttime);
        V(Qb) <+ transition(d_0b,delay,ttime);
end
endmodule
```

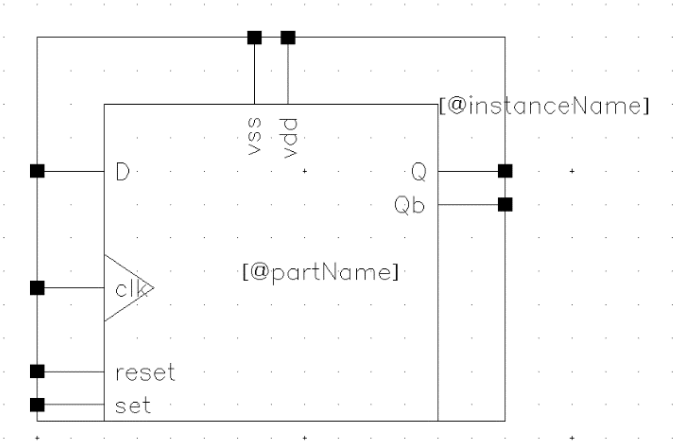


Figure 58: D-FF symbol

4.2.6 Inverter Gate:

```
// VerilogA for SAR_VerilogA_Asynchronous, VerilogA_inv, veriloga

`include"constants.vams"

`include"disciplines.vams"

module VerilogA_inv(A,X);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 60p;

parameter real clk_threshold = 0.5;

input A;

output X;

electrical A,X;

real X_out;

analog begin

        if(V(A) > vtrans) begin

                X_out = 0; end

                else begin

                X_out = 1; end

        V(X) <+ transition(X_out,delay,ttime);

end

endmodule
```

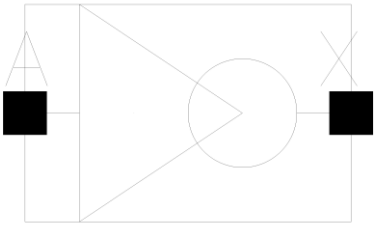


Figure 59: Not Gate Symbol

4.2.7 XOR Gate:

```
// VerilogA for SAR_VerilogA, VerilogA_XOR, veriloga
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_XOR(A,B,X);
parameter real vtrans=0.55;
parameter real delay = 0;
parameter real ttime = 60p;
parameter real clk_threshold = 0.5;
input A,B;
output X;
electrical A,B,X;
real X_out;
analog begin
        if(V(A) == V(B)) begin
                        X_out = 0; end
                else begin
                        X_out = 1; end
         V(X) <+ transition(X_out,delay,ttime);
end
endmodule
```

Figure 60:XOR Gate symbol

4.2.8 AND Gate:

```
// VerilogA for SAR_VerilogA, VerilogA_AND, veriloga

`include"constants.vams"

`include"disciplines.vams"

module VerilogA_AND(A,B,X);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 60p;

parameter real clk_threshold = 0.5;

input A,B;

output X;

electrical A,B,X;

real X_out;

analog begin

        if(V(A) < vtrans) begin

                X_out = 0; end

        else if(V(B) < vtrans) begin

                X_out = 0; end

        else begin

                X_out = 1; end

        V(X) <+ transition(X_out,delay,ttime);

end

endmodule
```

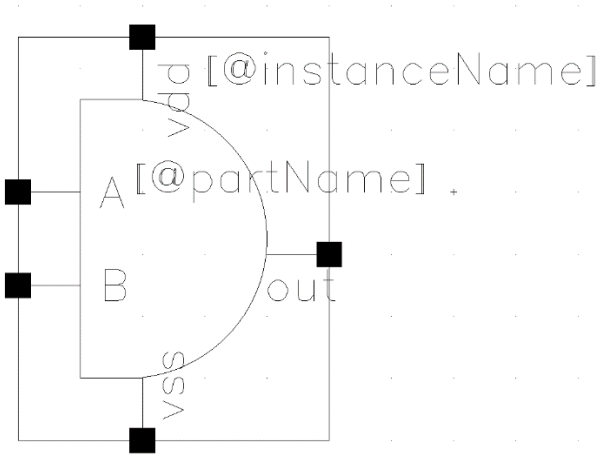


Figure 61: AND Gate Symbol

4.2.9 Multiplexer (2-to-1):

```
// VerilogA for SAR_VerilogA_Asynchronous, VerilogA_2to1Mux, veriloga
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_2to1Mux(in0,in1,select,out,vdd,vss);
parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 60p;
parameter real clk_threshold = 0.55;
inout vdd,vss;
input in0,in1;
output out;
electrical in0,in1,select,out,vdd,vss;
real result;
analog begin
        if(V(select) < vtrans) begin
                result = V(in0); end
        else begin
                result = V(in1); end
        V(out) <+ transition(result,delay,ttime);
```

```
end
endmodule
```

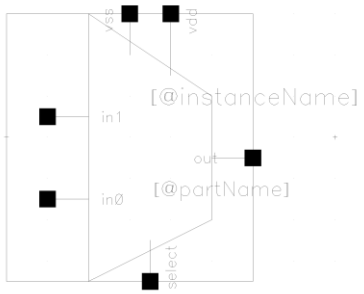


Figure 62: MUX Symbol

4.2.10 Delay Cell (1ns):

```
// VerilogA for SAR_VerilogA_Asynchronous, VerilogA_1ns_delaycell, veriloga
`include"constants.vams"
`include"disciplines.vams"
module VerilogA_1ns_delaycell(inp,outp,vdd,vss);
parameter real vtrans=0.5;
parameter real delay = 1n;
parameter real ttime = 1f;
inout vdd,vss;
input inp;
output outp;
electrical inp,outp,vdd,vss;
real d_out;
analog begin
        @(cross(V(inp) - vtrans, +1))
        begin
                d_out = 1;
        end
        @(cross(V(inp) - vtrans, -1))
        begin
                d_out = 0;
```

```
        end
        V(outp) <+ transition(d_out,delay,ttime);
end
endmodule
```

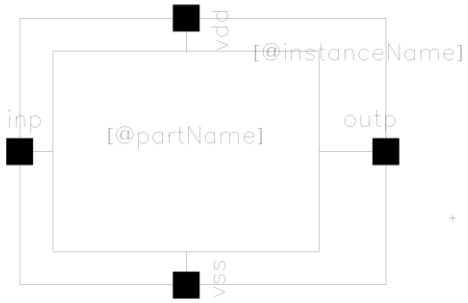


Figure 63: Delay call symbol

4.2.11 Clock Generator using ideal VerilogA blocks:

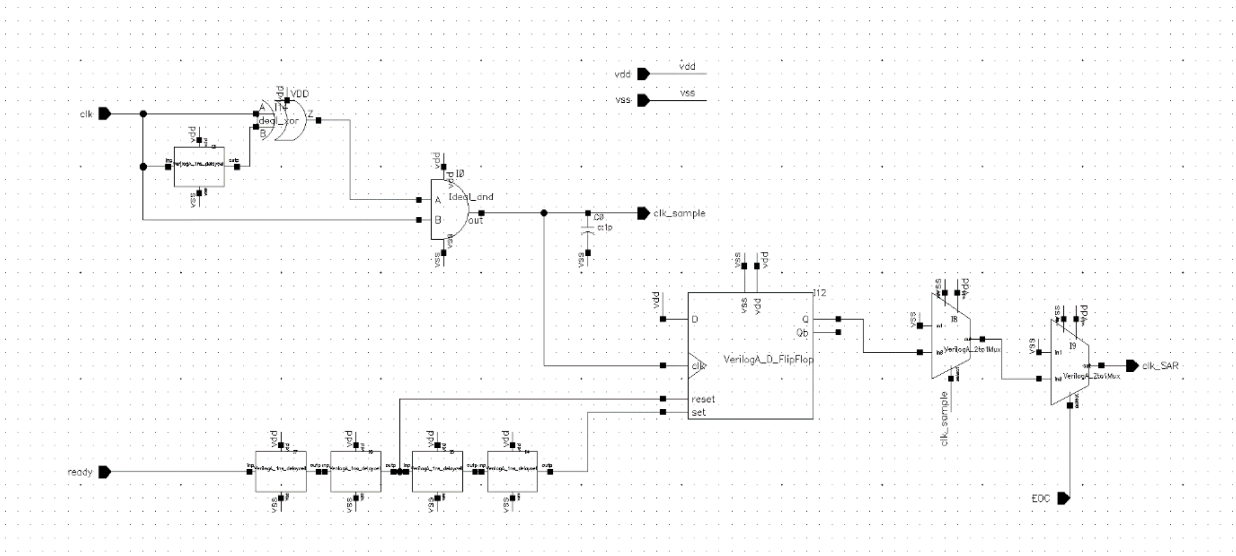


Figure 64: Clock generator circuit

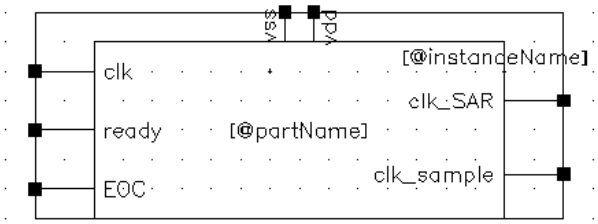


Figure 65: Clock generator block

4.2.12 Complete SAR ADC Block using VerilogA:

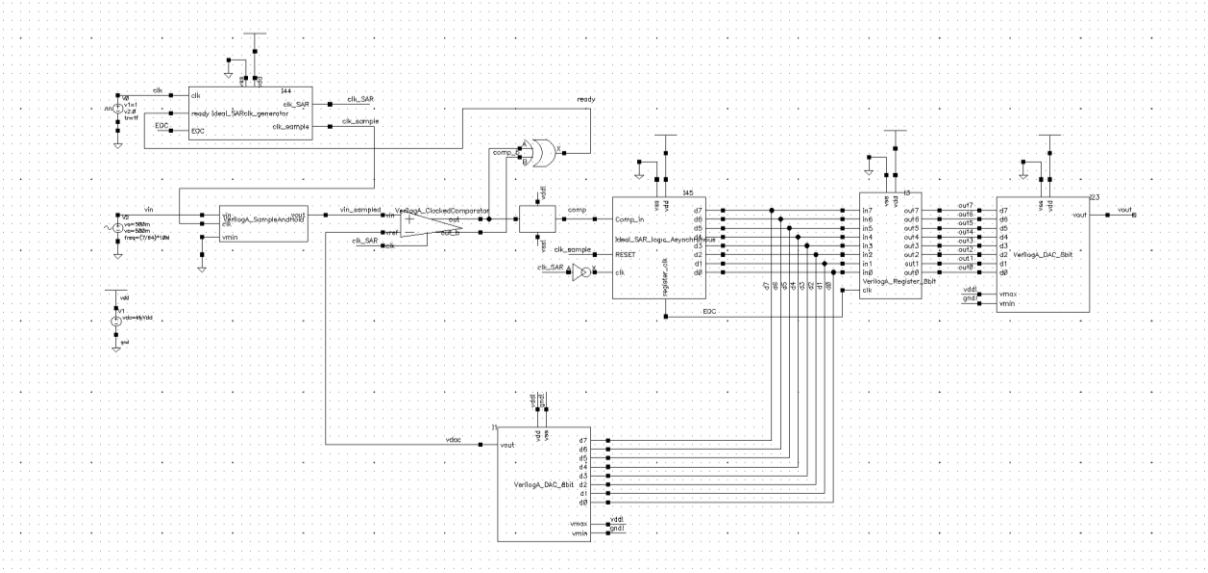


Figure 66: Asynchronous SAR ADC circuit using VerilogA

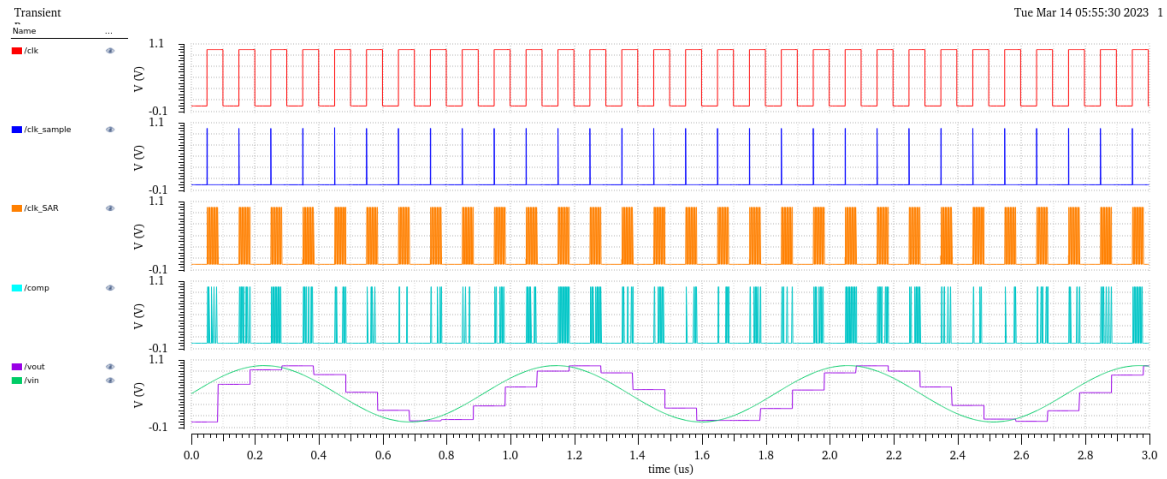


Figure 67: Transient Waveforms of the ideal asynchronous SAR ADC testbench

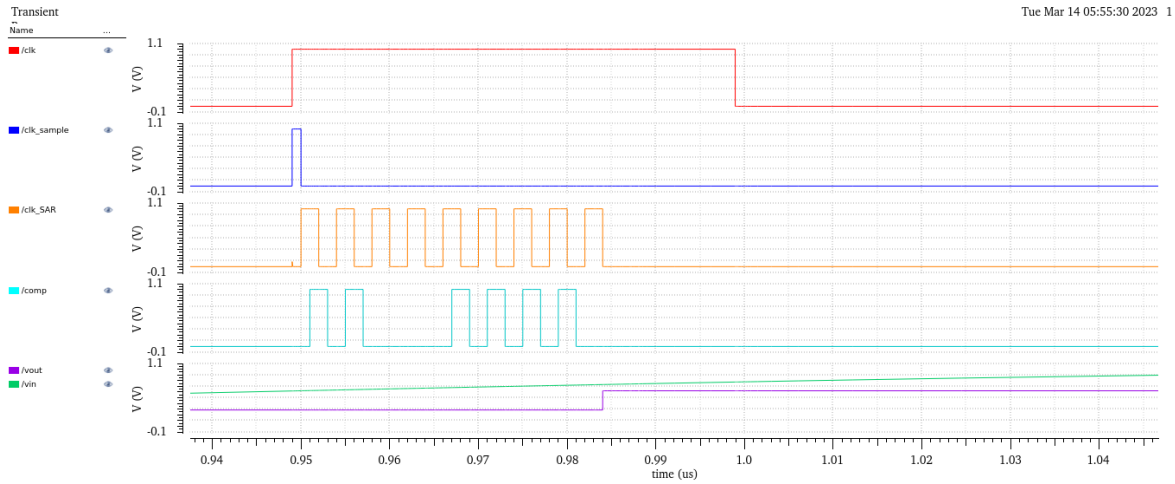


Figure 68: 1 conversion cycle for the asynchronous SAR ADC

4.3 Design of an 8-bit SAR ADC

In this section an 8-bit SAR ADC will be realised with the blocks discussed in the previous chapter. This design is achieved by designing each block and testing the blocks individually then replacing each VerilogA ideal blocks with the blocks designed with UMC 65nm technology. Later a 10-bit SAR ADC will be designed with the required specs and a few improvements.

4.3.1 Internal Clock Generator

The block responsible for providing clock signals to the system is the internal clock generator. It generates two output signals, **"clk_sample"** and **"clk_sar"** which are used during the sample and comparison phases, respectively. The internal clock generator has three inputs: **"clk_ext"** - the system's external clock; **"Ready,"** produced by the comparator to signal the system that it is ready for the next iteration; and **"EOC"** produced by the SAR logic block once all N bits are generated. The external clock's rising edge initiates the conversion cycle, and the internal clock generator controls the rest of the process until "EOC" is generated, indicating the completion of the conversion.

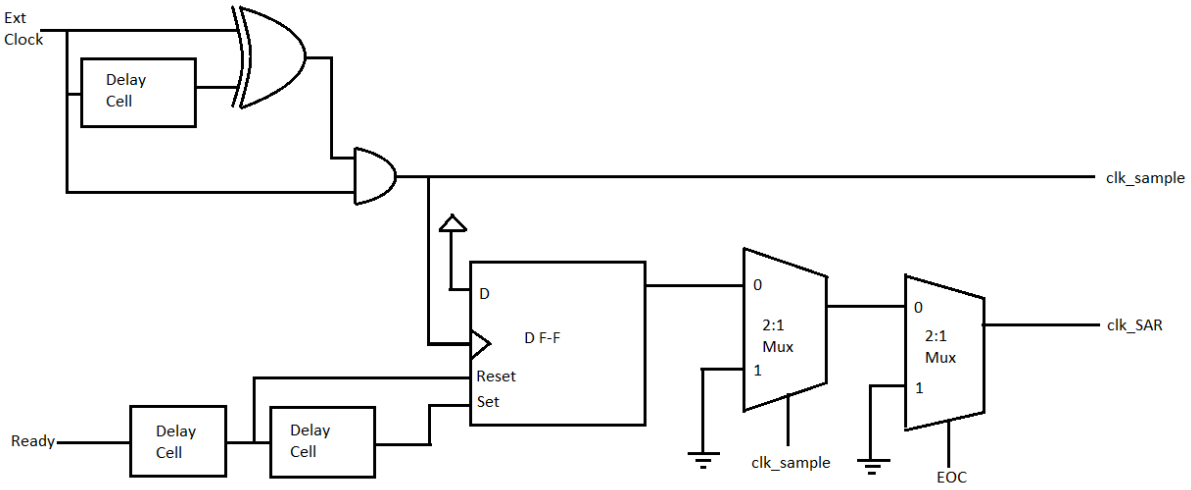


Figure 69: Block diagram of clock generator circuit

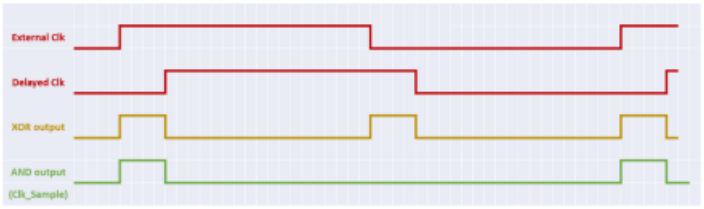


Figure 70: Timing diagram for "clk_sample" generation circuit

The circuit implementation of the internal clock generator is shown in Figure69. Part I is the part that creates the "**clk_sample**" signal. The delay chosen in this section is enough for the S/H circuit to settle when charging the DAC capacitors during the sampling phase. The XOR gate creates a pulse at each transition of the external clock and the AND gate only passes the pulse when "**clk_ext**" is high, as shown in Figure 70. Part II is responsible for toggling

"**clk_SAR**" after the sampling phase is done. The 2-to-1 multiplexers are used to prevent "clk_SAR" from toggling and to stay 0 during the sampling phase (**clk_sample = 1**) or after the conversion is done (**EOC = 1**). The D input of the flipflop is kept high, so that the Q output would initially be high, consequently causing "**clk_SAR**" to go high once the sampling phase ends (clk_sample becomes 0). Part III controls the toggling of "**clk_SAR**" through the set and reset inputs of the flipflop, while ensuring that set and reset are never high at the same time (invalid state). The "**clk_SAR**" going high triggers the reset signal, which pulls "**clk_SAR**" low after a certain delay, and the "Ready" going high triggers the set signal, which pulls "**clk_SAR**" high after a certain delay. The flipflop used is a CMOS, and the rest of the digital gates are CMOS gates, as shown in Figure 72. The implementation of the delay cell is shown in Figure 73.

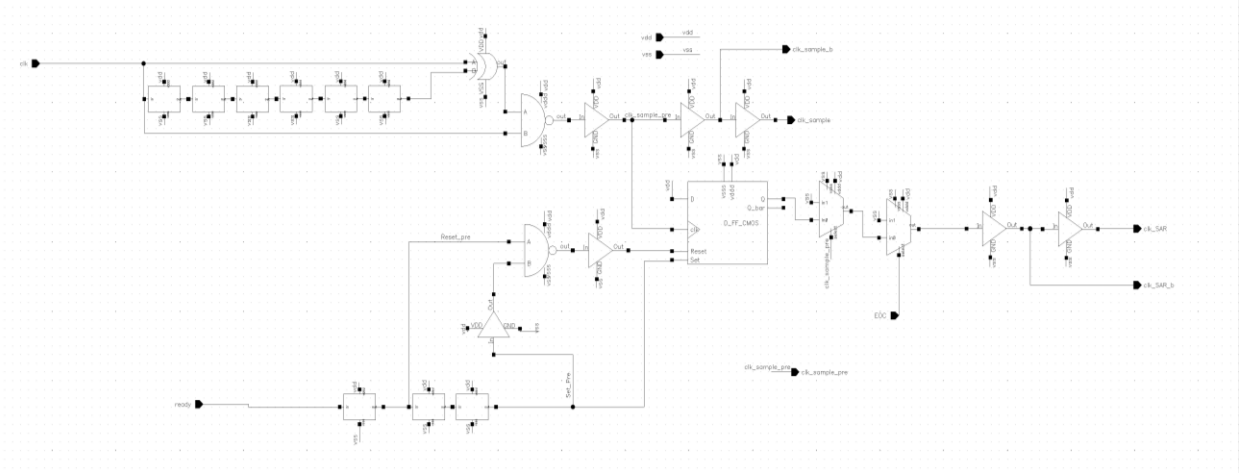
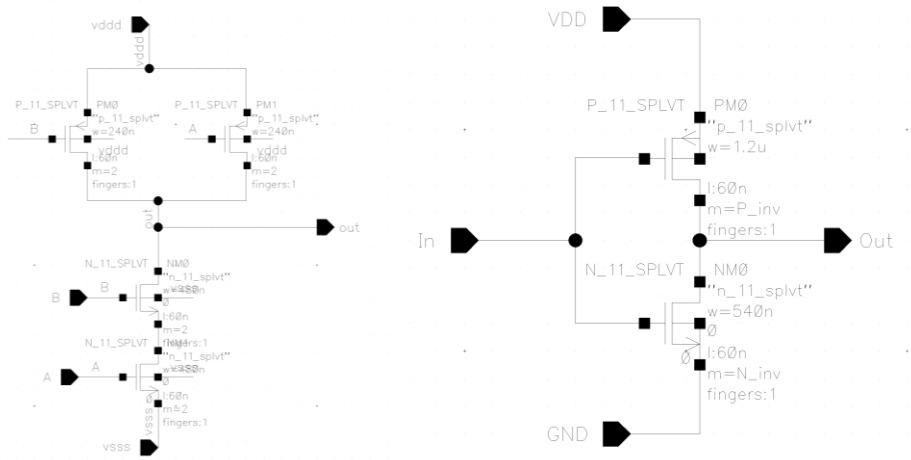
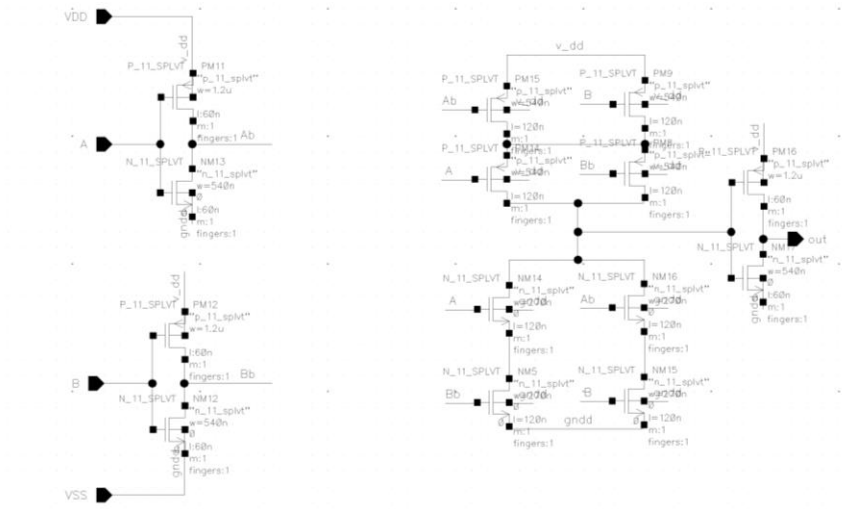


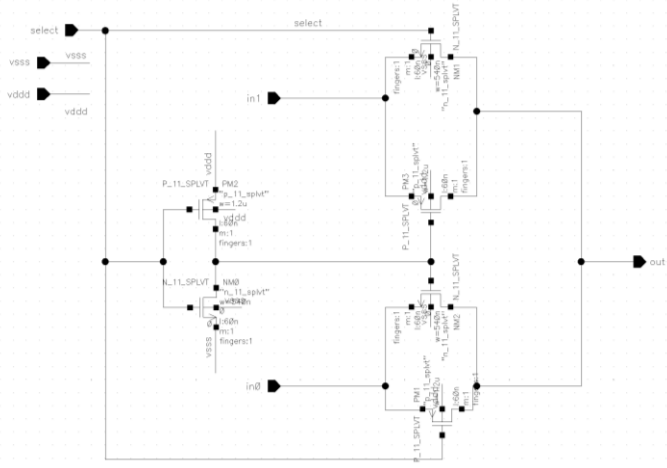
Figure 71: Schematics of the circuit implementation of the internal clock generator



(a) (b)



(c)



(d)

Figure 72: Digital gates used in the internal clock generator block (a) NAND, (b) Inverter, (c) 2-to-1 Mux, (d) XOR

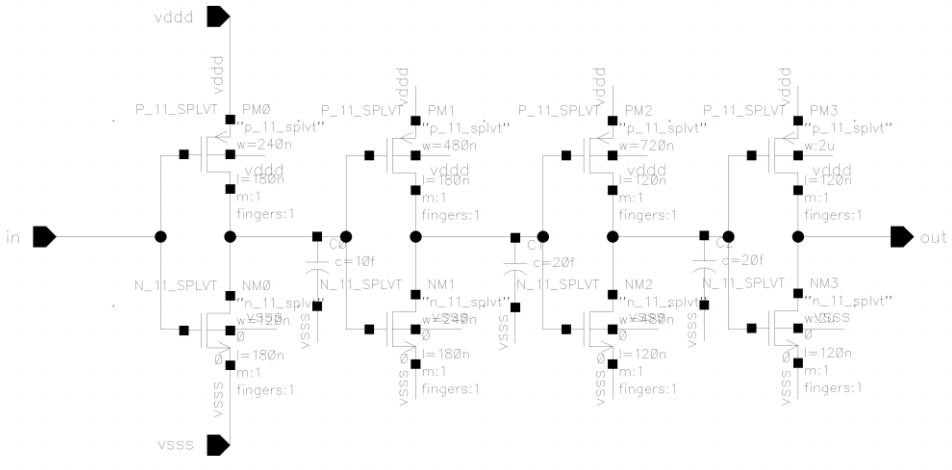


Figure 73:Delay Cell circuit implementation

4.3.2 The bootstrapped Circuit

The bootstrapped circuit is shown in Fig. . The MOSFET devices Mn1, Mp1, Mn2, and Mp2 act as switches that are used to charge the offset capacitor during the hold phase (clk = 0) and to fix the VGS of the main switch MnSW during the sample/track phase (clk = 1). The large VGS ensures that MnSW is completely ON and much greater than the threshold voltage VTH while the source voltage of MnSW is changing. The gate nodes of MnSW and Mp2 are tied because during sampling, Vg and Mp2's source are usually greater than VDD. For Mp2 to be completely off, its gate must be tied to the highest voltage in the circuit, hence tied to Vg. The bulks of the PMOS switches Mp1 and Mp2 are connected to the highest voltage of the circuit which is the positive node of COFFSET. During the hold phase, Mn4 connects Vg to the lowest voltage in the system to ensure complete shut-off of MnSW. Mn3 is added to prevent Mn4 from having a very high VGD when Mn4 is OFF. Since Vg ≥ VDD and the gate voltage of Mn3 is VDD (less than Vg), then Mn3 won't act as a strong pass device and the drain of Mn4 will be limited to a maximum of VDD-VTH. Regarding the value of COFFSET, the bigger it is, the better it can maintain a constant Vc during the sampling phase, but at the expense of larger area. With MpSW added in parallel to MnSW, the clock feedthrough effect is cancelled-out, since they both operate with 2 opposing clocks (clk & clk_b)

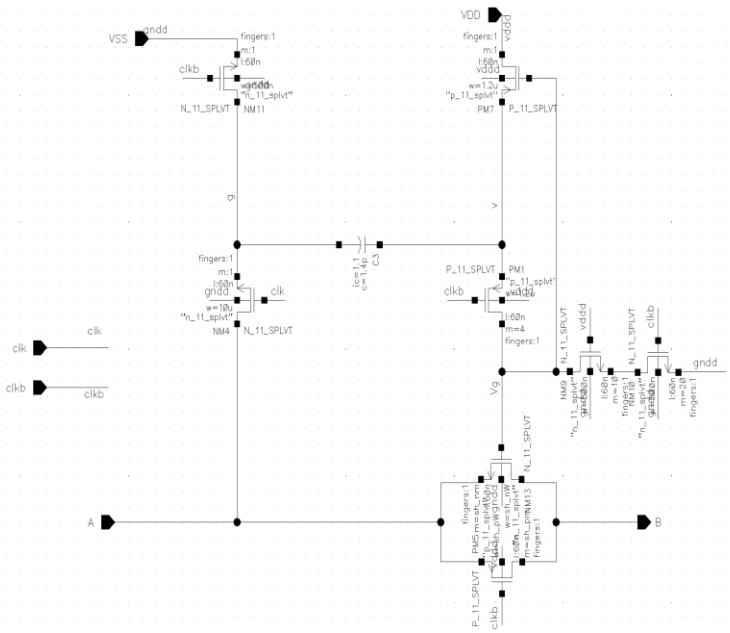


Figure 74: The bootstrapped architecture

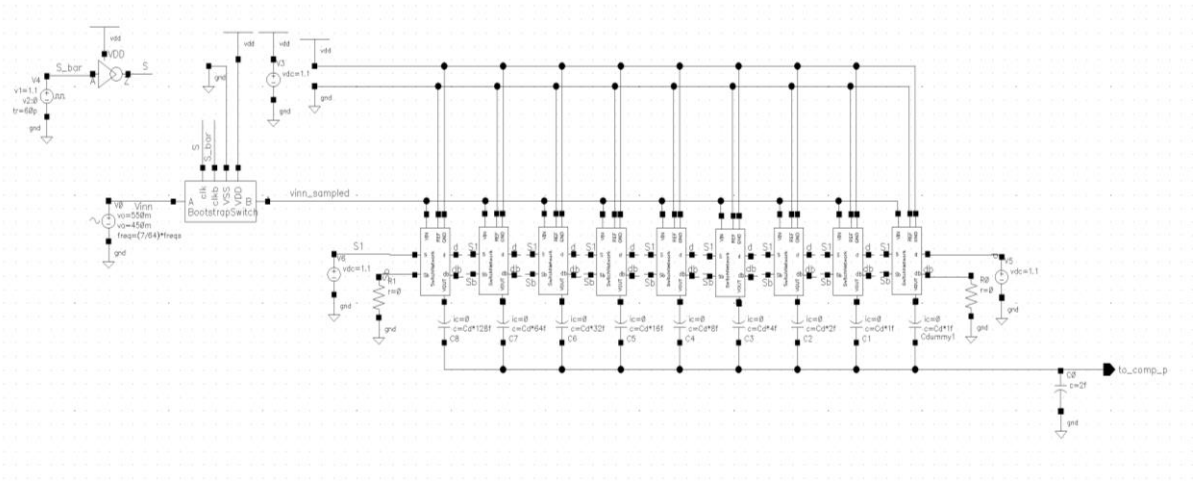


Figure 75: Bootstrapped switch testbench

Design Variables

	Name	Value
1	tg_dac_nW	480n
2	tg_dac_pW	720u
3	tg_dac_pm	15
4	tg_dac_nm	20
5	sh_nW	4.8u
6	sh_nm	10
7	sh_pW	4.8u
8	sh_pm	10
9	Boot_m	20
10	N_inv	1
11	P_inv	1
12	Cd	2
13	freqs	50M

Figure 76: Bootstrapped Switch Design Variables

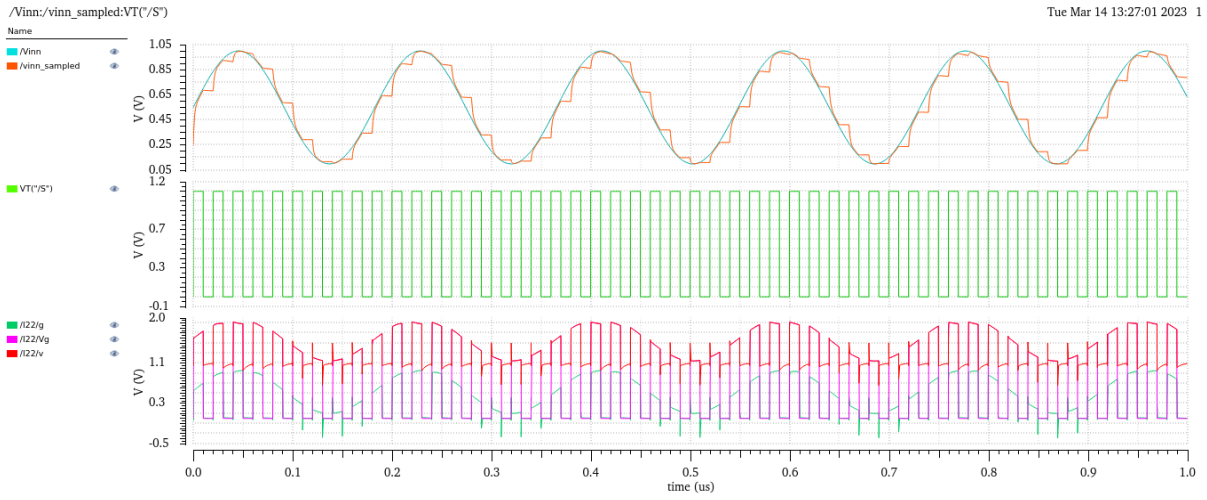


Figure 77: Transient Waveforms of the bootstrapped switch testbench

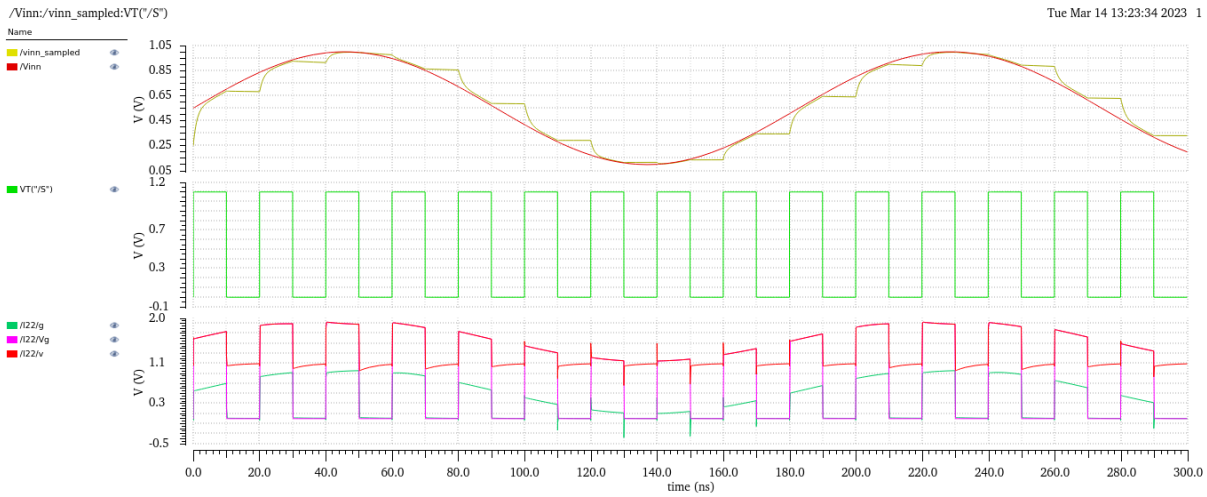


Figure 78: 1 cycle of the input to the bootstrapped switch

4.3.3 The Comparator Circuit

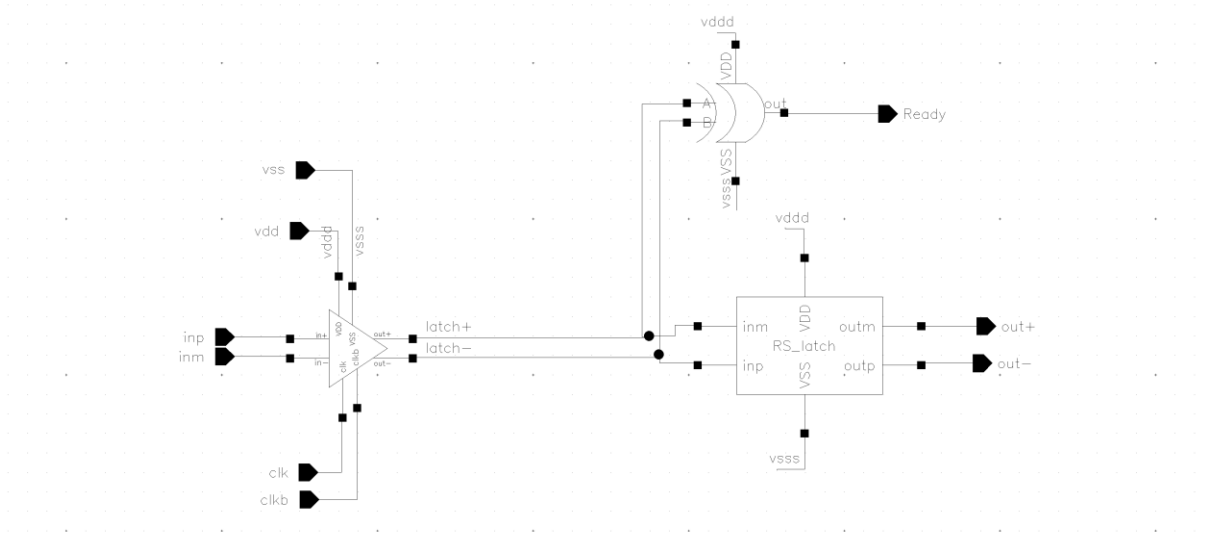


Figure 79:Block Diagram of the Dynamic Comparator

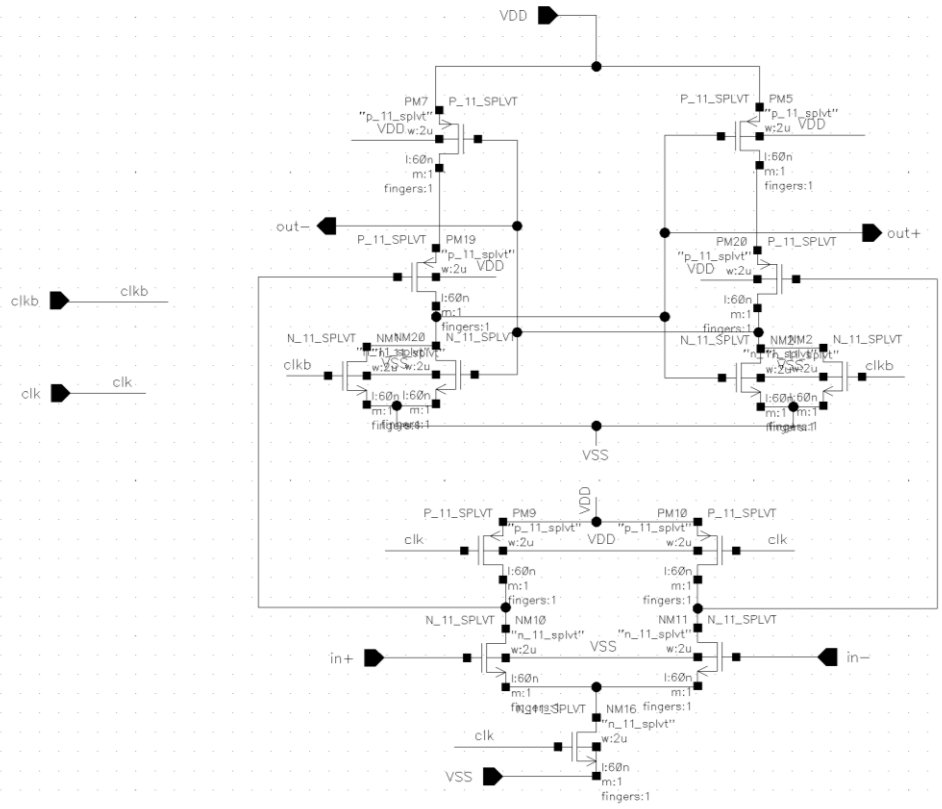


Figure 80: Two Stage Dynamic Comparator

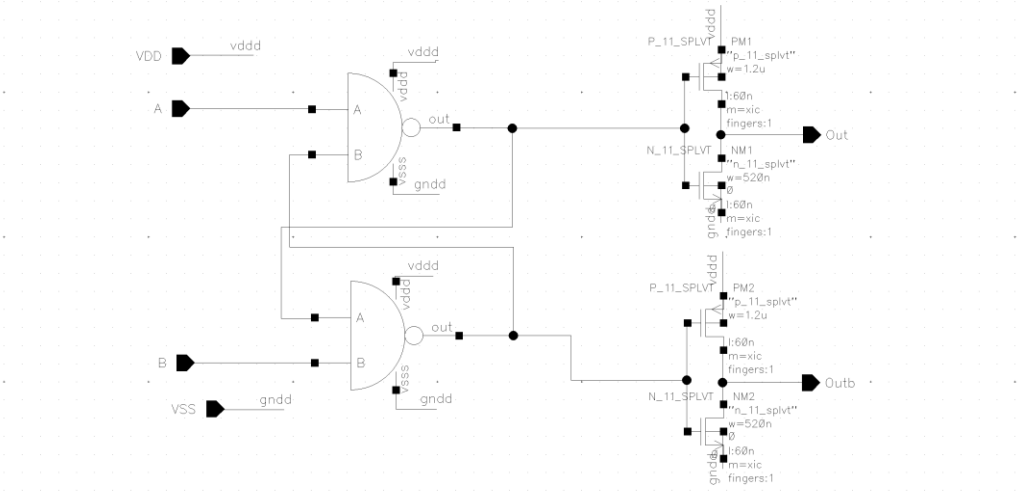


Figure 81: R-S Latch circuit

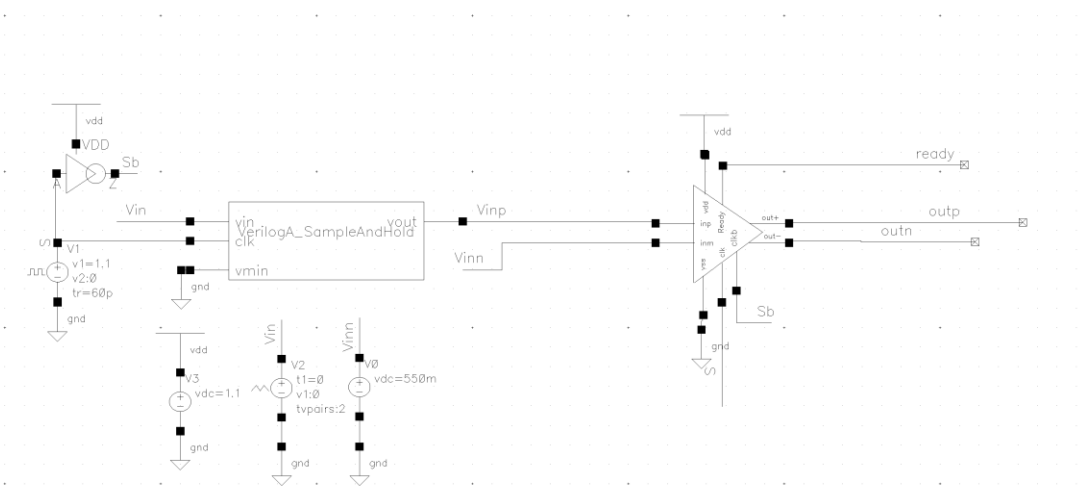


Figure 82: Sample and hold circuit testbench

Design Variables

	Name	Value
1	SR_outp_inv	15
2	SR_nmos	3
3	SR_outn_inv	15
4	freq_dk	400M

Figure 83: Design variables for Comparator

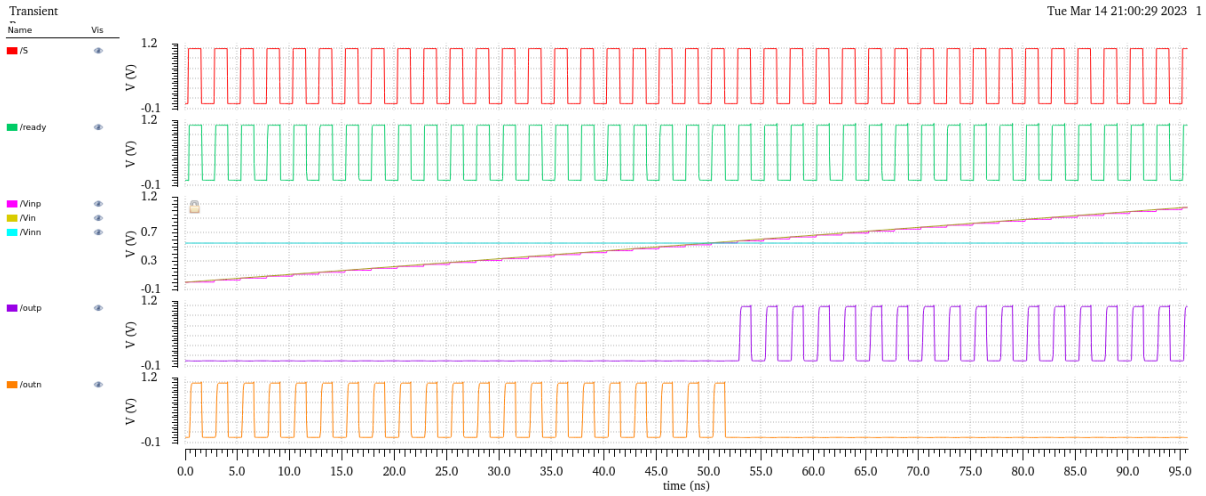


Figure 84: Comparator Test-bench Wave

4.3.4 Capacitive DAC

One of the key parameters that determine the performance of the SAR ADC is the settling time of the capacitive DAC. The testbench in Figure86 is used to determine the effect of changing the value of the unit capacitor and the sizing of the transmission gate switches' devices. The

settling time decreases as the capacitors' values decrease, but that leads to a lower SNR due to higher thermal noise. Another way to decrease the settling time is to make the transmission gate switches less resistive by increasing the W of the switch's transistors but increasing the W too much can lead to significant parasitic capacitance. Figure 87 show the waveforms with faster settling and slower setting times respectively. The delay from "clk_SAR" to the reset input of the FF in part C of the internal clock generator in Figure71 is chosen to be longer than the settling time of the DAC. The proposed system is designed for a 20fF unit capacitance in the DAC and a settling time < 1ns.

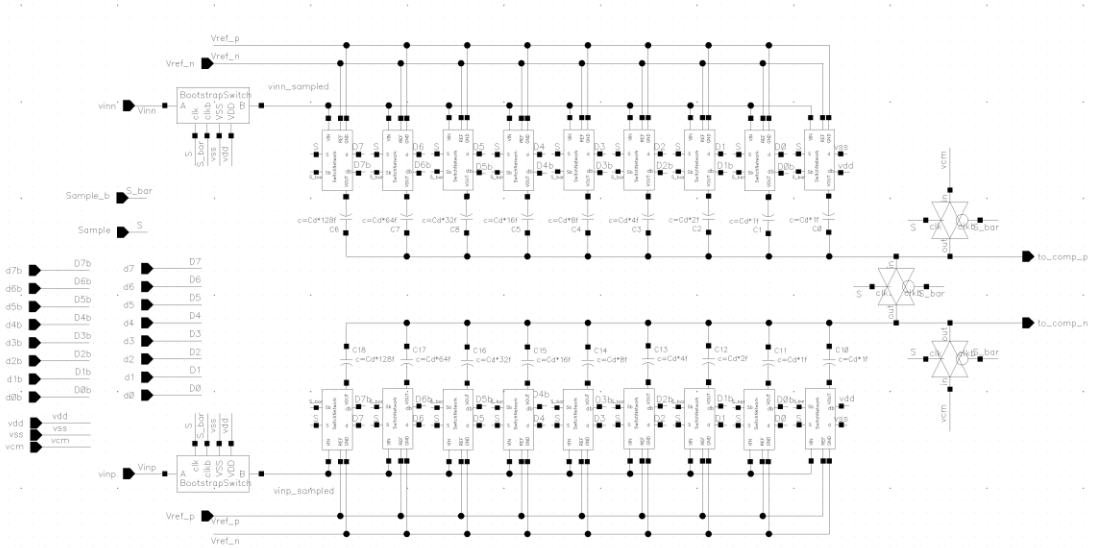


Figure 85: Binary weighted capacitive DAC

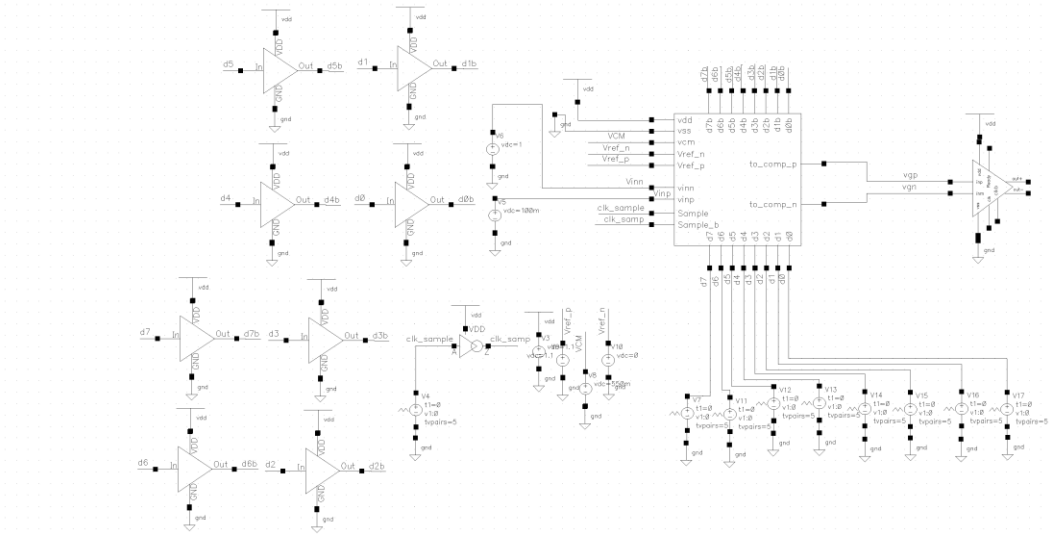


Figure 86: Testbench for the capacitive DAC

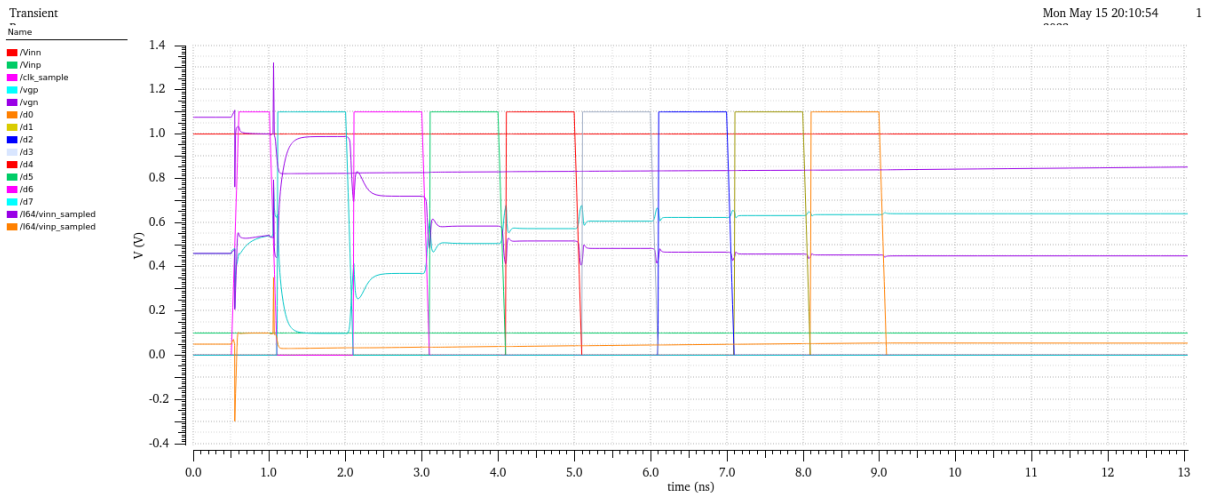


Figure 87: Transient waveforms of the capacitive DAC testbench

4.3.5 SAR Logic

As discussed in section 3.7 the SAR Logic is designed in 8-bit.

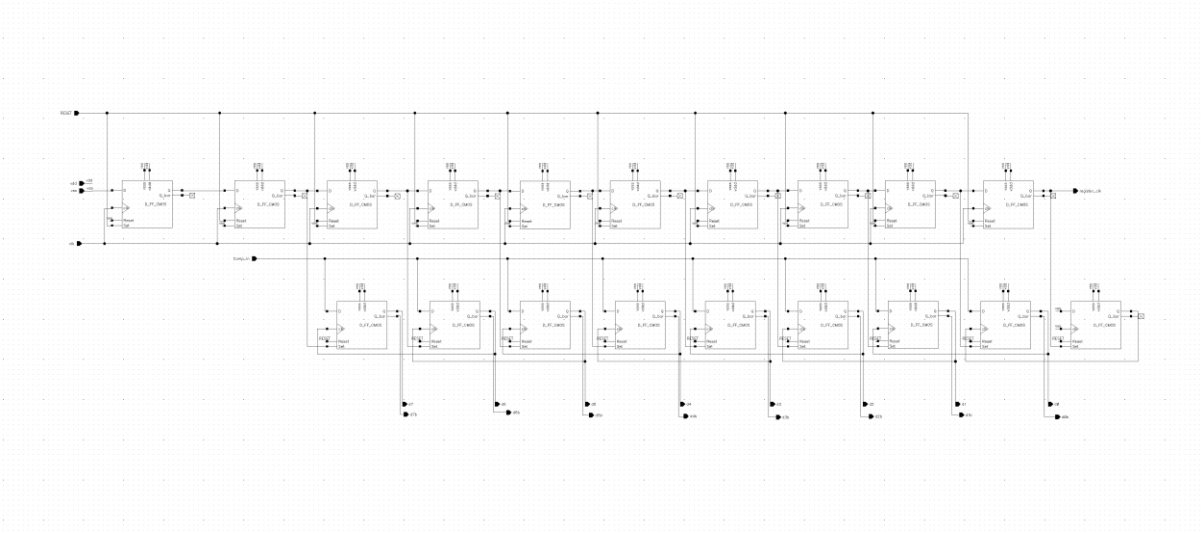


Figure 88: 8-bit SAR Logic schematic

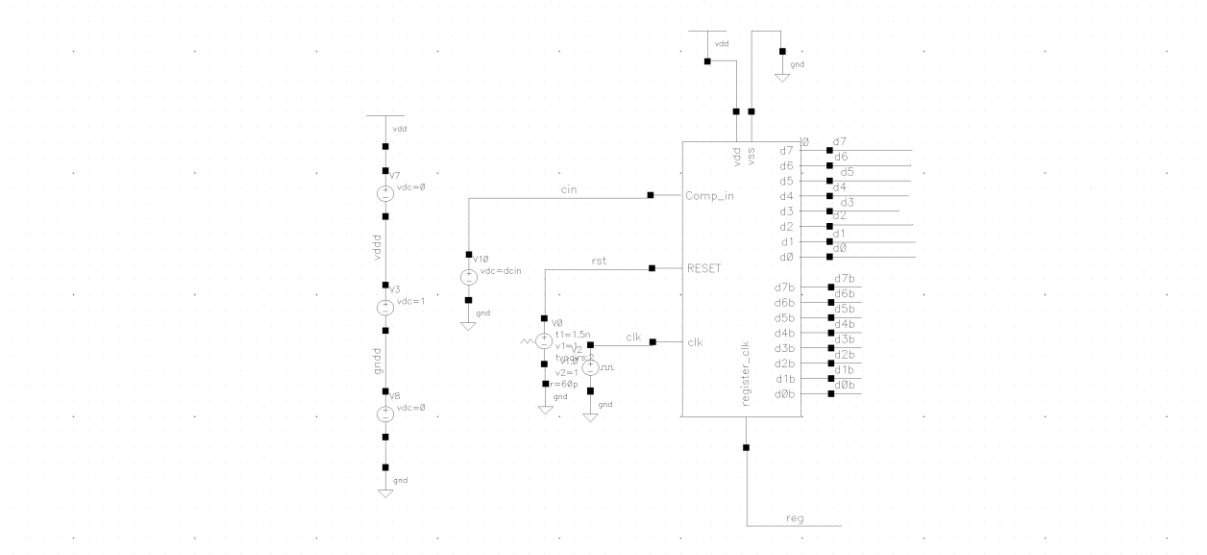


Figure 89: SAR Logic Testbench setup

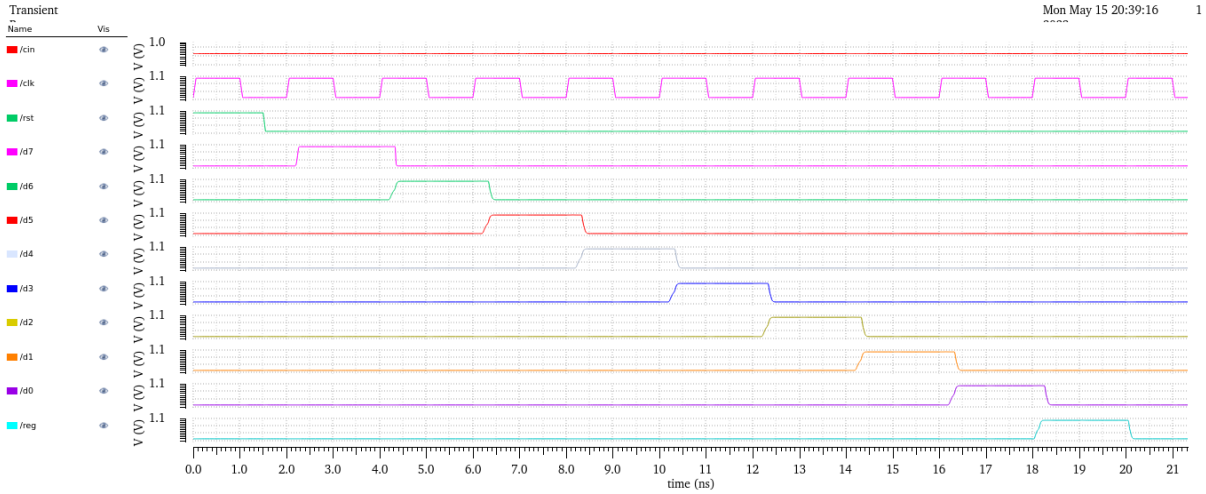


Figure 90(a): Transient waveforms of the capacitive DAC testbench (Cin = 0V)

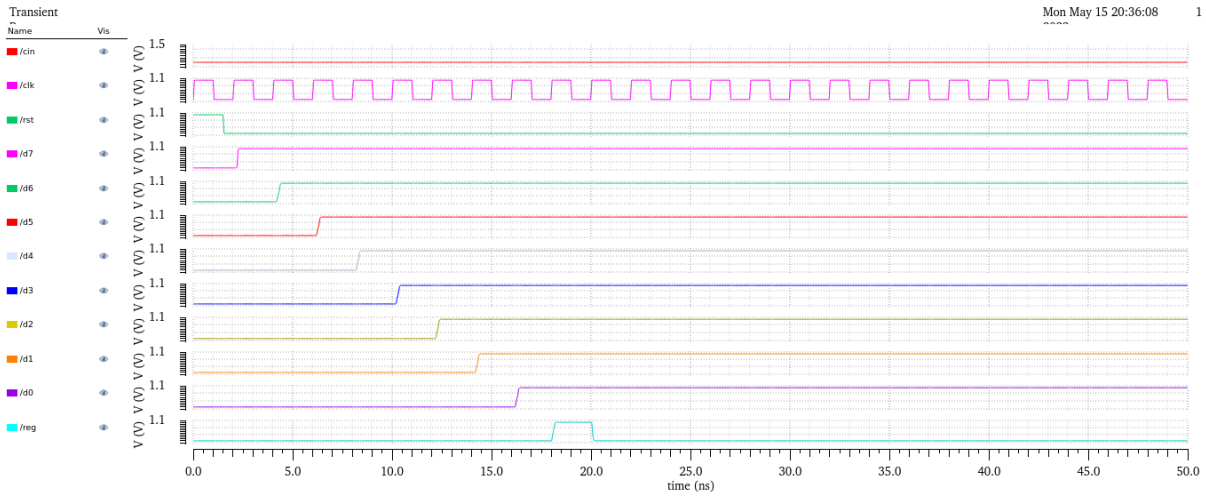


Figure 90(b): Transient waveforms of the capacitive DAC testbench (Cin = 1.1V)

4.3.6 Output Register

The output register's job is to receive the final DAC code at the rising edge of the EOC signal and releases it at the falling edge of EOC which happens at the rising edge of the next external clock cycle. The FFs used in this block are CMOS FFs at shown in Fig. 29. CMOS FFs are used in this block instead of TSPC FFs to ensure rail-to-rail node voltages within the circuit since the EOC signal is a low-frequency signal.

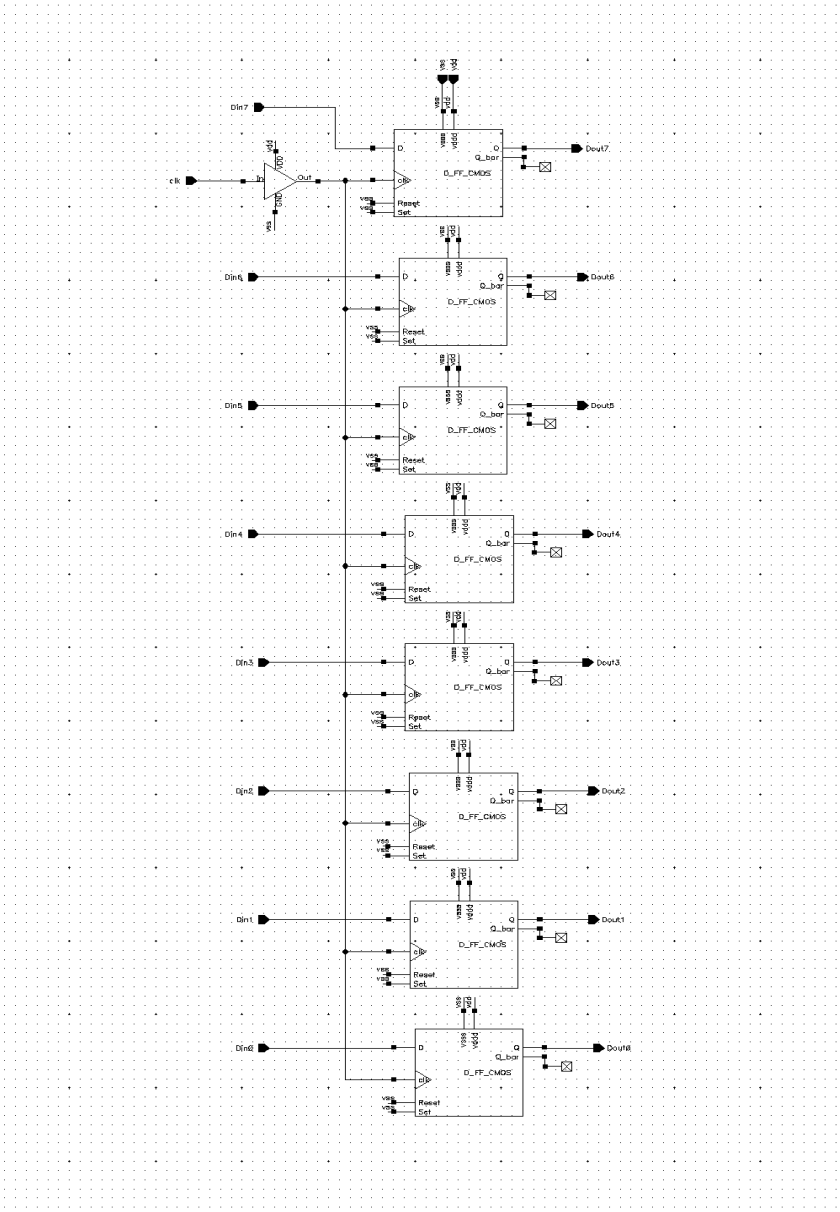


Figure 91: Schematics of the output register

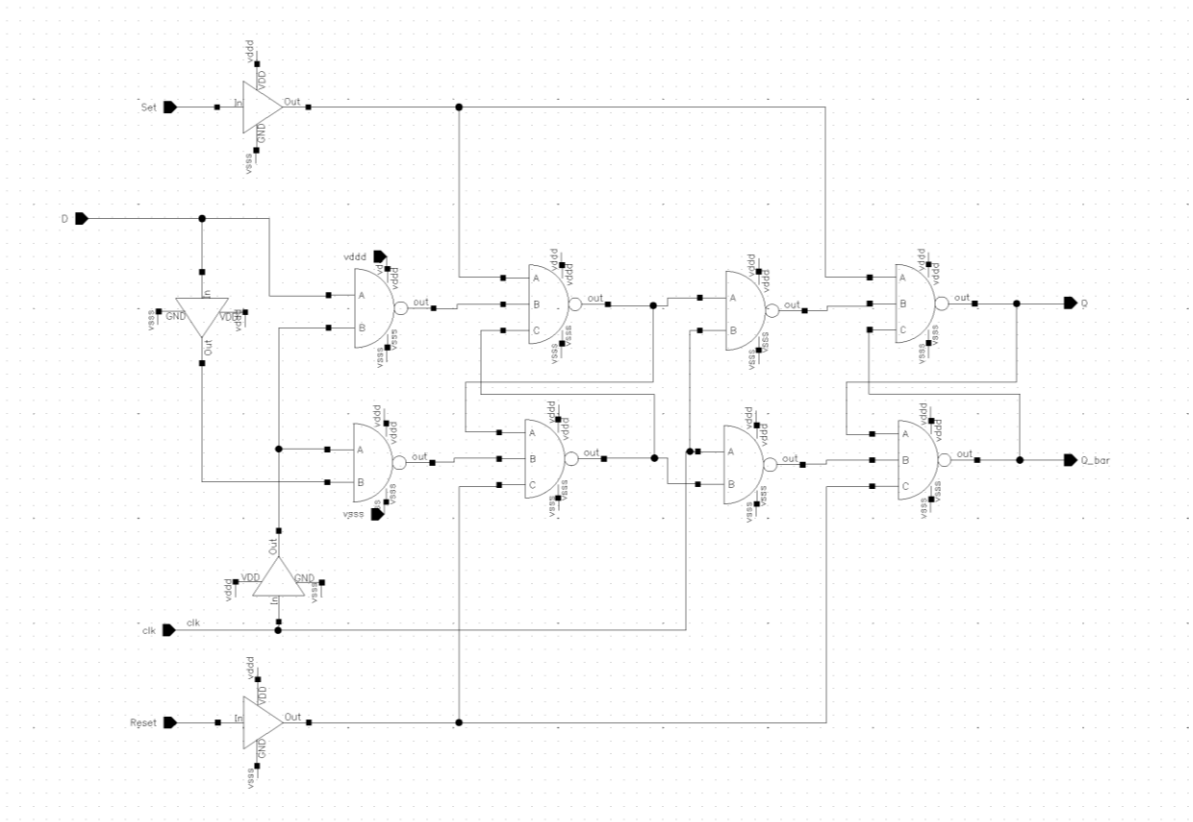


Figure 92: CMOS D-Flip Flop

4.3.7 Whole Asynchronous SAR ADC system

The testbench used to test the whole asynchronous SAR ADC is shown in Figure93, with all the important node voltages probed and plotted in Fig. 94. The stimuli used were an external clock of 20 MHz and inputs “Vinp” and “Vinp” each of frequency 7/64 * 20 MHz and amplitude of 0.6 V (from 0.2 V to 0.8 V), producing an output of 20 MS/sec.

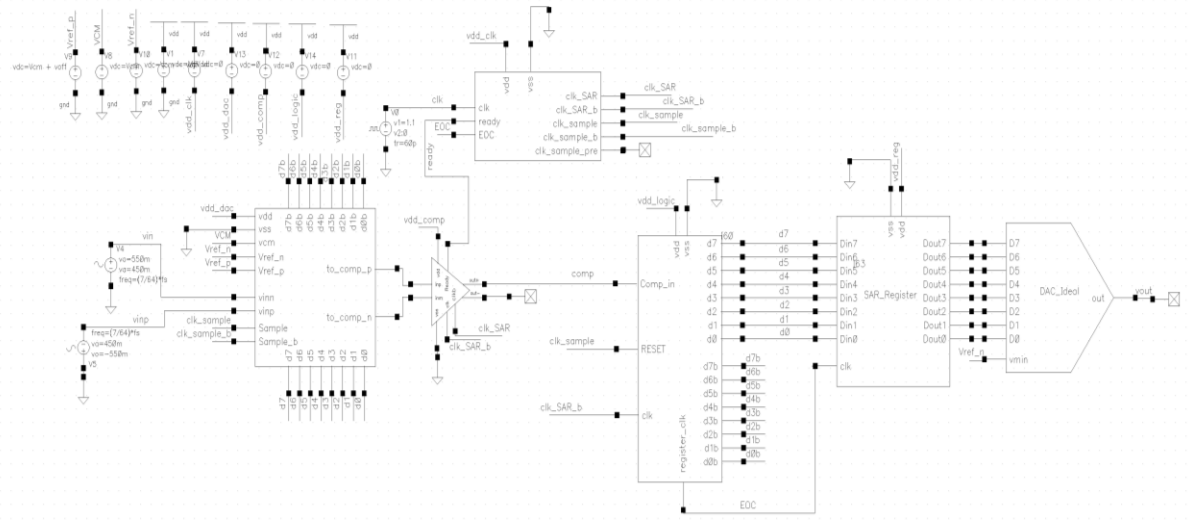


Figure 93: Testbench of the whole asynchronous SAR ADC

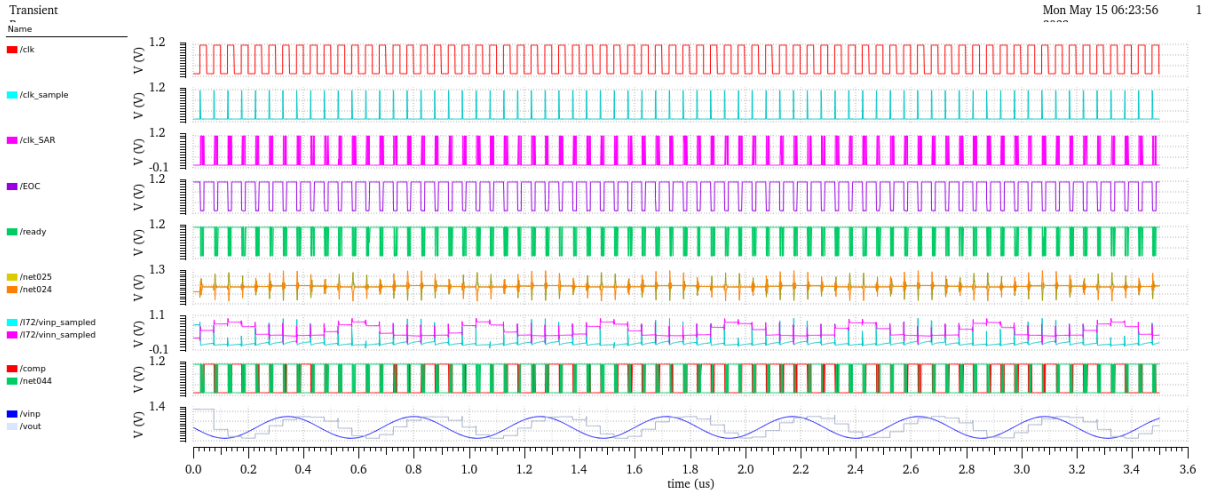


Figure 94: Transient waveforms of the asynchronous SAR ADC testbench

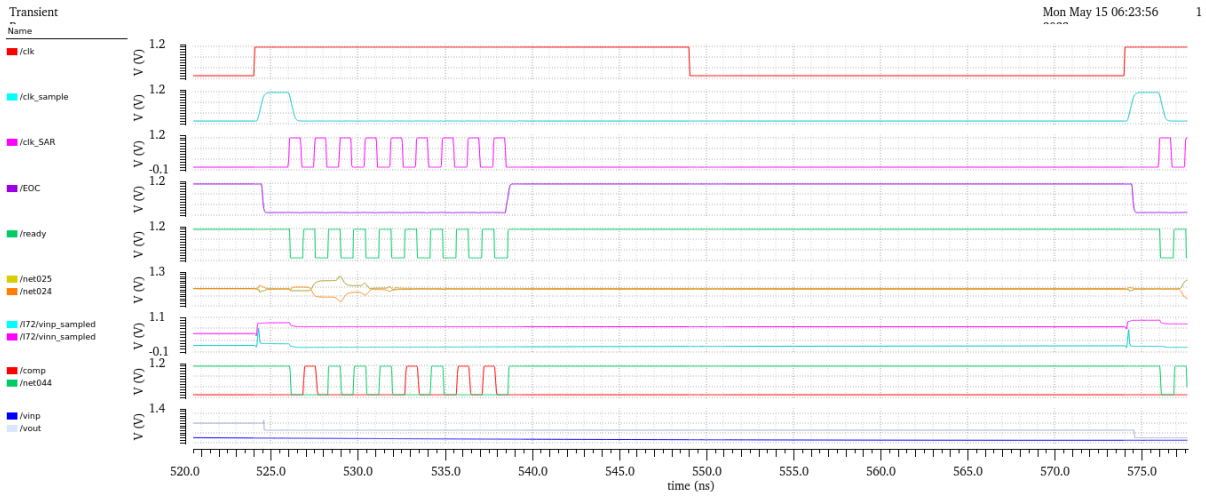


Figure 95: Waveforms of the asynchronous SAR ADC testbench during 1 conversion cycle

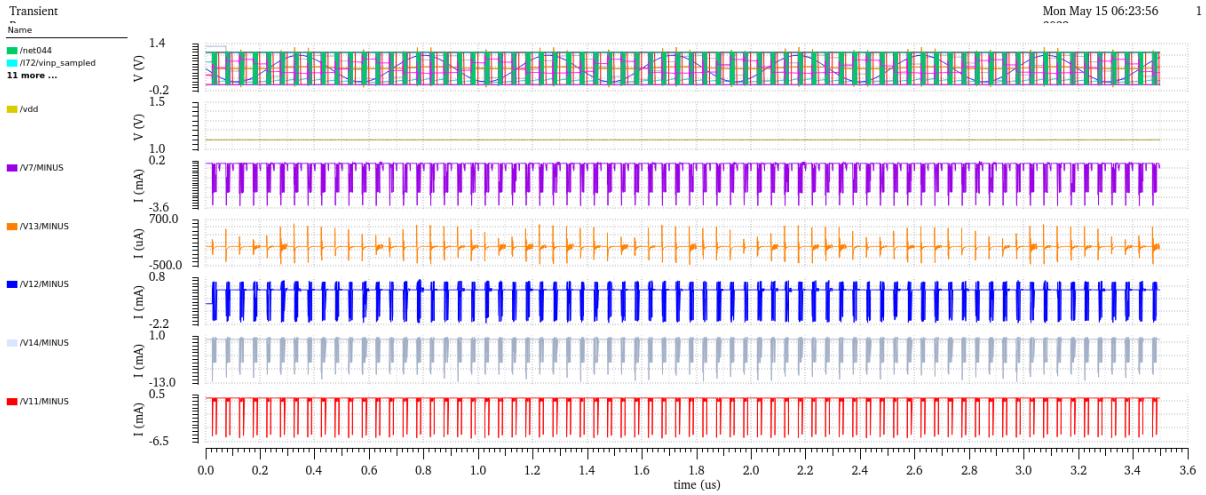


Figure 96: Waveform of the current drawn by each circuit of the SAR ADC

Figure 95 is a zoomed snapshot of the waveforms during 1 conversion cycle. At the rising edge of “clk_external”, a pulse is generated at “clk_sample” in which the sampling of the inputs

occurs. Once “clk_sample” goes low, “clk_SAR” goes high causing the code from the SAR logic block to redistribute the charges in the capacitive DAC, changing the input nodes to the comparator “vgp” and “vgn”. At the falling edge of “clk_SAR”, the DAC would have settled already, and the comparator is activated(regeneration phase). When the outputs of the two stage comparator latch “latch+” and “latch–” give opposite rail-to-rail output levels (a strong high and a strong low), the “ready” signal goes high which triggers “clk_SAR” to go up high after a certain delay. After 8 cycles of “clk_SAR”, the EOC signal or “register_clk” signals the output register to output the result of the conversion process, which is the final digital code from the SAR logic block. To measure the performance, the digital output is converted to its analog equivalence and the FFT is taken for this analog output.

The stimuli and the measurement parameters are determined from the external clock frequency of the system as follows:

$fCLK$ = 20 MHz For $FFTofN$ = 64, $andto$ $have$ 1 $input$ $cycle$ $every$ 7 $sample$ $cycles$, $then$:

fIN = 7/64 x 20 = 2.1875 MHz

$Tsampling$ = 1/$fsampling$ = 50 ns

$Then$, the $simulation$ $time$ to $capture$ 64 $sampling$ $cycles$ or 7 $inputcycles$: $Tsimulation$ = 64 x 50 ns = 3200 ns

And $Adding$ 150 ns as an $intialization$ $time$, $then$ the $measurement$ $time$ $taken$ is: $Tmeasurement$: 150ns → 3350 ns

The spectrum of the final output of the asynchronous SAR ADC testbench, from which the key dynamic ADC performance metrics are measured, is shown in Figure 97. The signal-to-noise-and-distortionratio (SINAD) is calculated from the signal-to-noise ratio (SNR) and the total harmonic distortion (THD) as in equation (). Since the THD is neglected in this setup, the SINAD and SNR are considered the same. The theoretical SNR for an N-bit ADC driven by a full-scale sine wave and that only considers the quantization noise is given by equation (). Using the equation of SNR, the effective number of bits (ENOB) can be obtained from equation (). The ENOB represents the actual resolution of the ADC after taking the noise and the distortion of the system into consideration. As a measure of the strength of the desired signal compared to the worst spur in the output spectrum, the spurious-free dynamic range (SFDR) is also found [16].

$$SINAD\ (indBs) = 10\log\left(\frac{PSignal}{Pnoise + Pdistortion}\right) = -10\log\left(10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right) \quad (37)$$

$$SNR\ (indBs) = 10\log\left(\frac{PSignal}{Pnoise}\right) = 6.02\ N + 1.76 \quad (38)$$

$$THD\ (indBs) = 10\log\left(\frac{PSignal}{Pdistortion}\right) \quad (39)$$

$$ENOB\ (inBits) = SINAD - 1.76\ 6.02 \quad (40)$$

These key metrics and parameters of the system are displayed in Table 11. The figure-of-merit (FOM) of the system is defined by equation (41). The aim of the design is to decrease the FOM, which mainly involves decreasing the total power consumption and improving the ENOB. The power is improved by using circuits that consume no static power like the two stage dynamic comparator, while theENOB is improved by using techniques like bootstrapped switching and highly sensitive strongarm latch design. The achieved FOM from the proposed SAR ADC is 1.534 fJ/conversion-step which is comparable to earlier asynchronous SAR ADC designs, as shown in Ref [108].

$$FOM = \frac{Ptotal}{2^{ENOB}.fs} \quad (41)$$

Table 12: Performance Summary

Parameter	Value
Technology	UMC 65 nm CMOS
Power Supply	1.1 V
Resolution	8 bits
Sampling Rate	20 MS/s
Common-Mode Voltage	0.55 V
Differential Input Range	1.1 V
Sampling Unit Cap	20 fF
SINAD	45.852 dB
SFDR	46.152 dB
ENOB	7.6 bits
Total Power	510uW

Table 12shows how the total power is divided among the different blocks. Most of the power consumption come from the digital blocks, with the delay cells being the biggest contributor to the high power. The power of the digital circuits usually scales down well with supply, since the dynamic power is directly proportional to VDD 2 as shown in equation (42). This allows the proposed asynchronous SAR ADC to have the potential to offer more power reduction in future design work.

$$Pdynamic = \alpha . C_L . V_{DD}{}^2 . fclk \quad (42)$$

Table 13: Power Consumption Per Block

Block	Power
Internal Clock Generator (including delay cells)	161 uW
SAR Logic	287.2 uW
Comparator	53.6 uW
DAC + Switches	9.09 uW
Total Power	510 uW

4.4 Design of 10-bit SAR ADC

4.4.1 Clock Generator Circuit

The same clock generator circuit (as designed in this chapter in section 4.3.1) is implemented in this design as well.

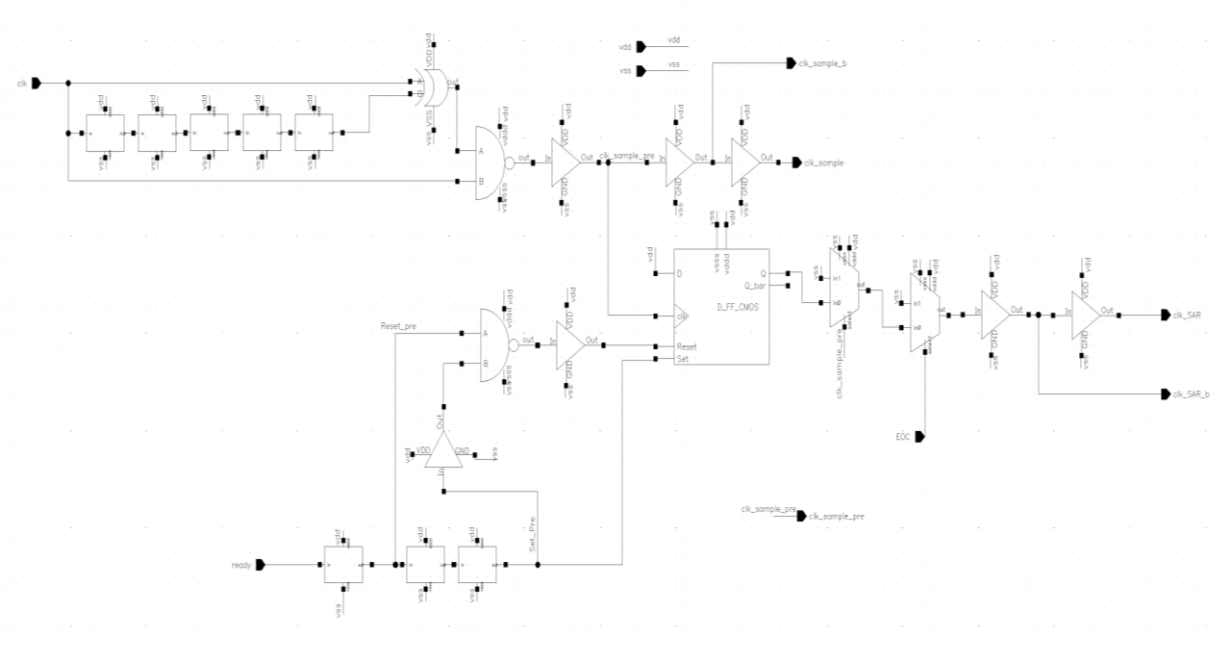


Figure 97: Block Diagram of Clock Generator

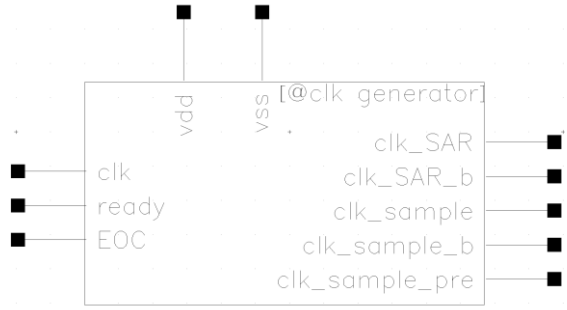


Figure 98: Clock Generator Symbol

4.4.2 Double Bootstrapped Switch

As discussed in Chapter 3 Section 3.4.2 the double bootstrapped switch is implemented in this section.One notable advantage of the Double Bootstrapped Switch is its ability to improve overall system efficiency by reducing the voltage drop across the switch. This, in turn, minimizes power losses and enhances the energy conversion process. Additionally, the elimination of external diodes simplifies the circuit design and reduces component count, contributing to cost savings and improved reliability.

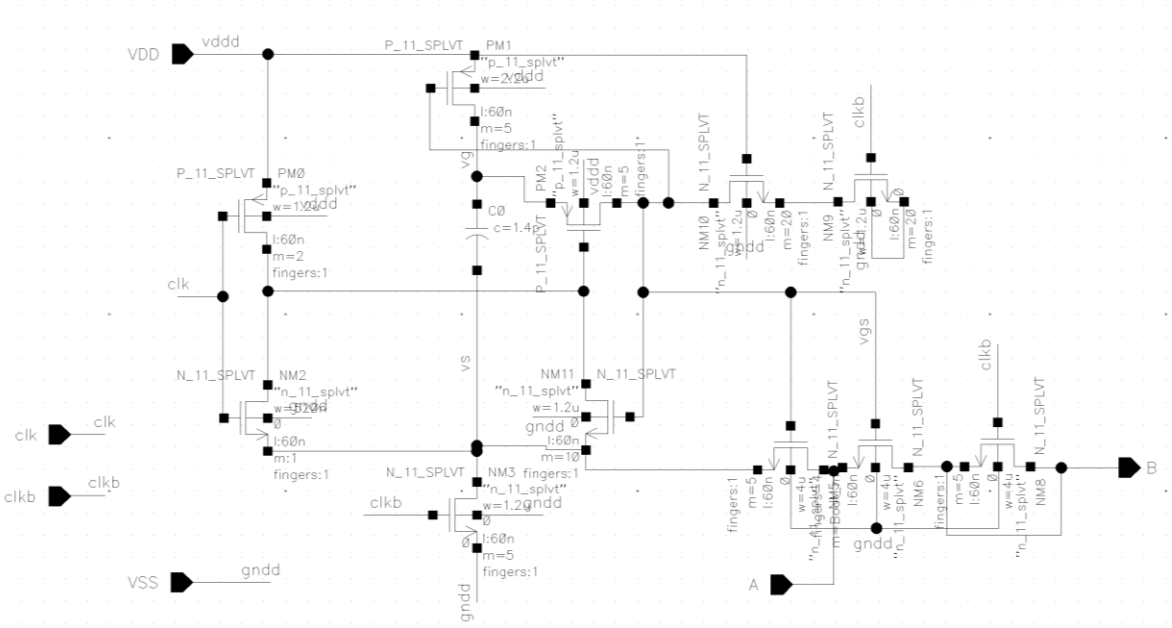


Figure 99: Circuit Diagram of Double bootstrapped switch

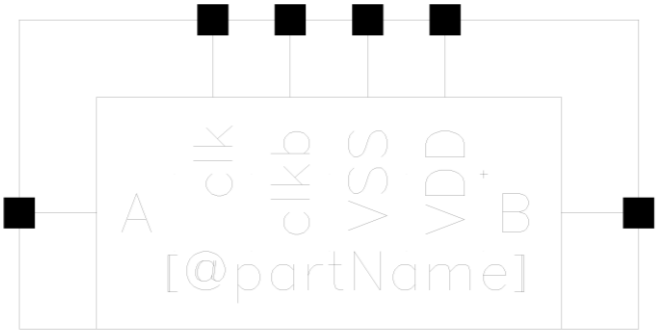
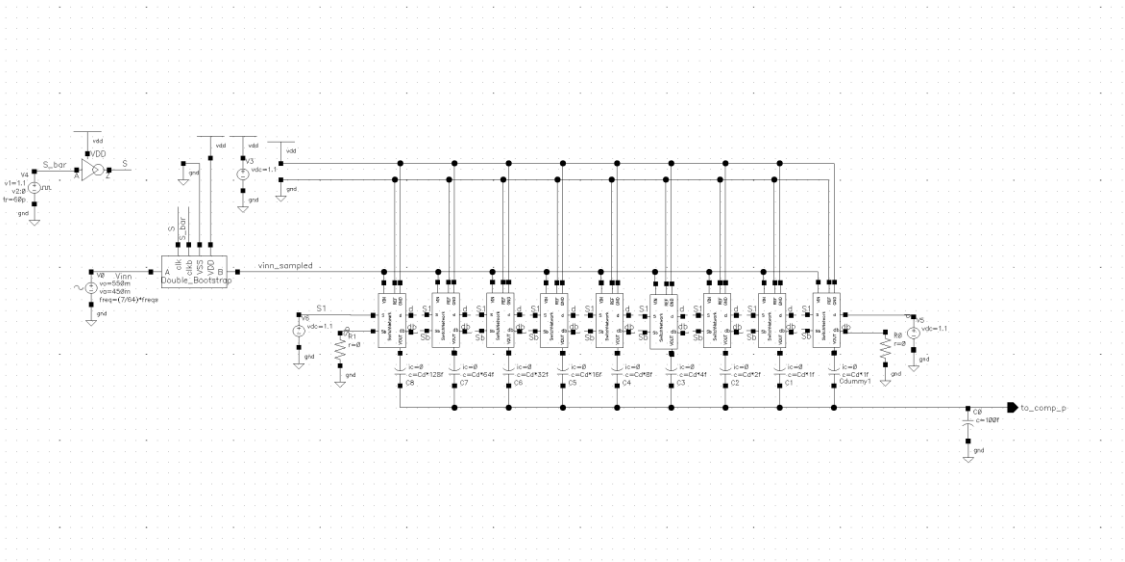
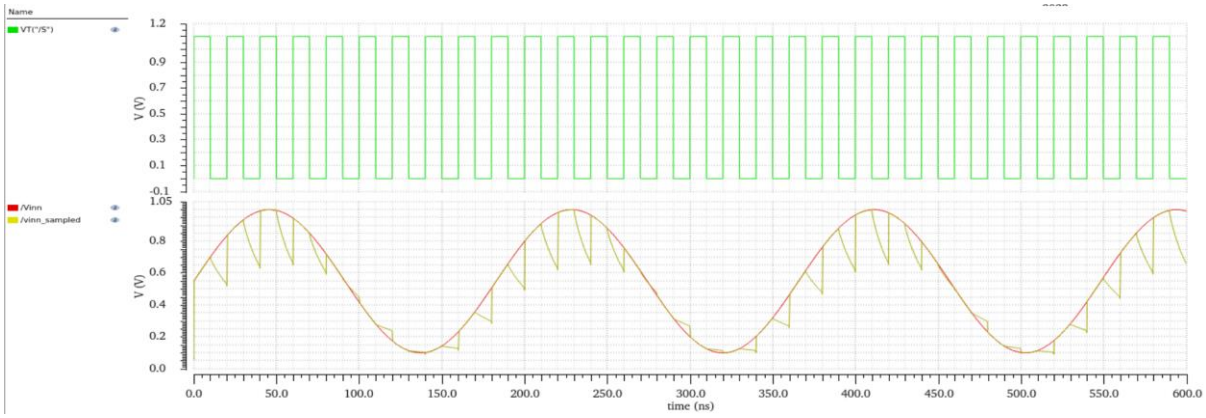


Figure 100:Block Diagram of Bootstrapped Switch



101(a)



101(b)

Figure 101: Bootstrapped Switch testbench setup. (a) Circuit (b) Waveform

4.4.3 Split Capacitive DAC

As discussed in section 3.5.3 a split capacitor DAC is designed in this section. The bridge capacitor is chosen to be fractional and the unit capacitor is selected to be 71.2fF.

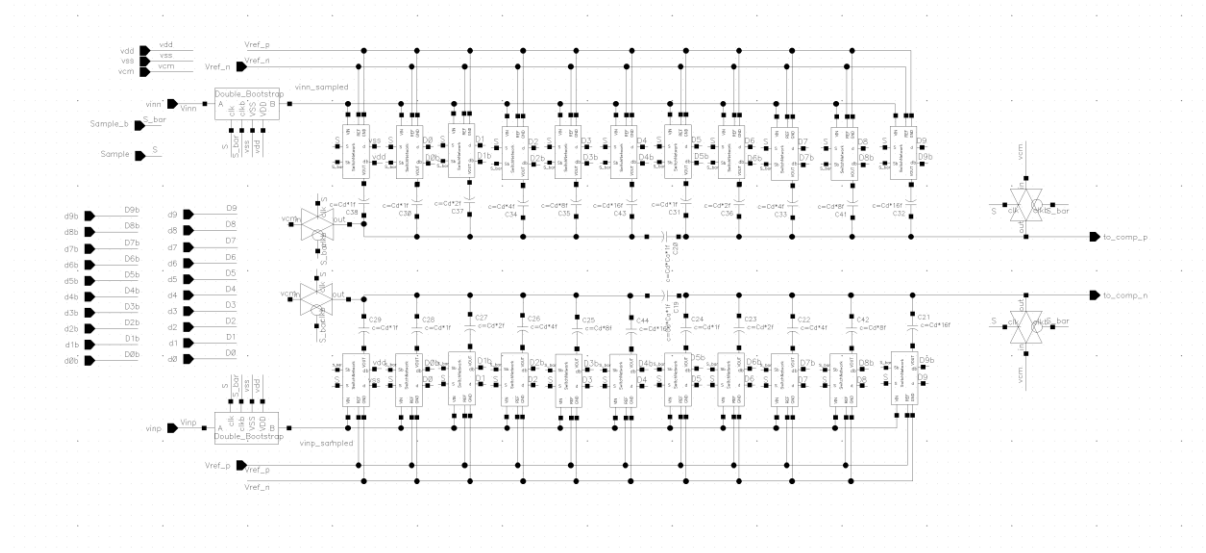


Figure 102: Circuit Diagram of Split-Capacitor DAC

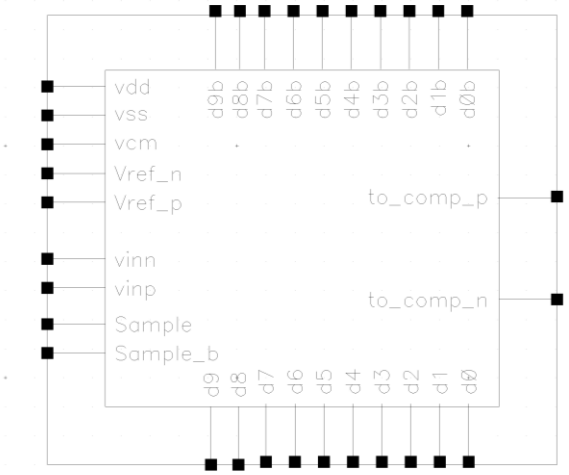


Figure 103: Block Diagram of DAC

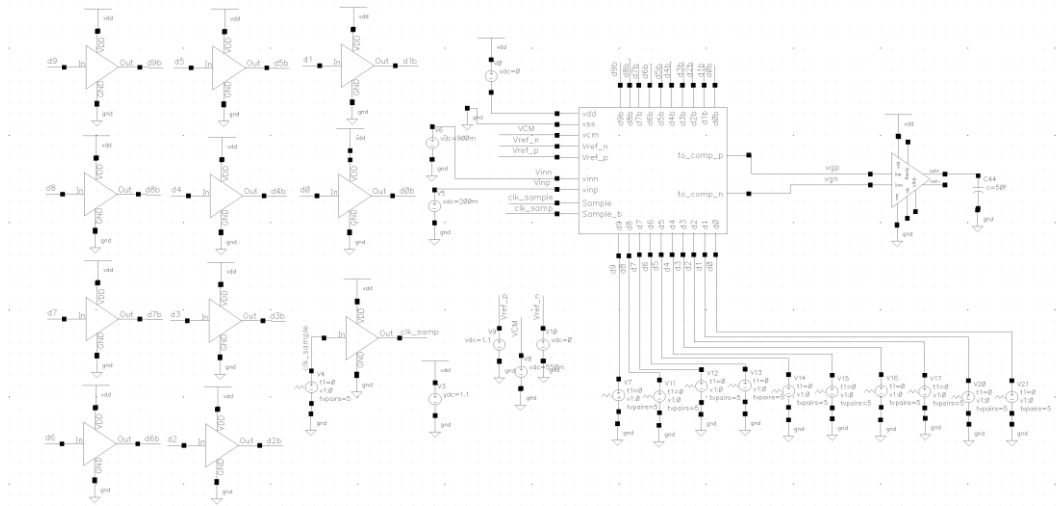


Figure 104: Testbench Setup for DAC

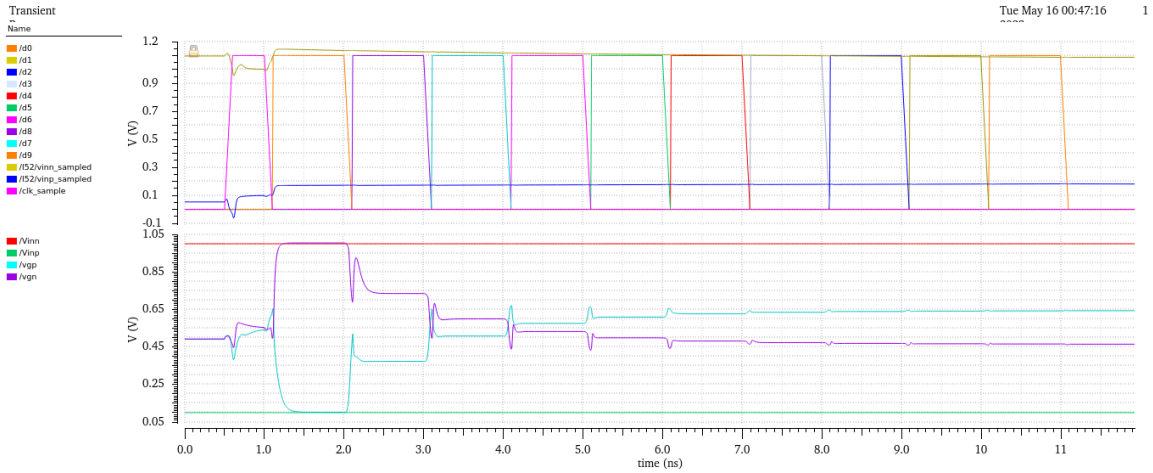


Figure 105: Transient waveforms of the capacitive DAC testbench

4.4.4 SAR Logic

The previous SAR Logic block is used only two more D-Flip flops are added to increase the bits from 8 to 10. The new circuit is given in Figure and the testbench result of the circuit is given thereafter.

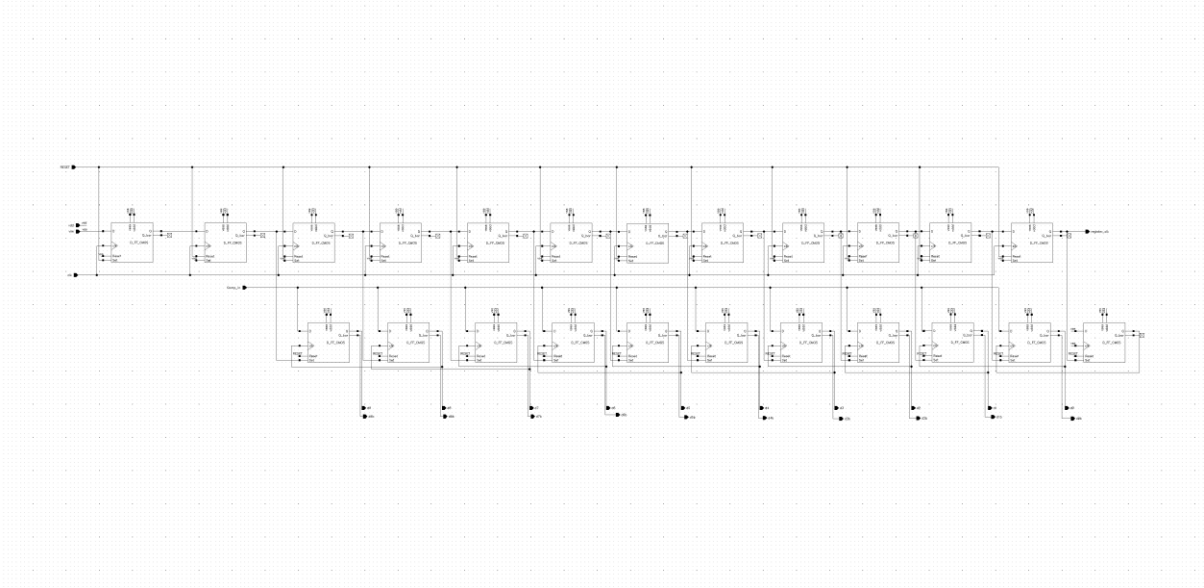


Figure 106: 10-bit SAR Logic schematic

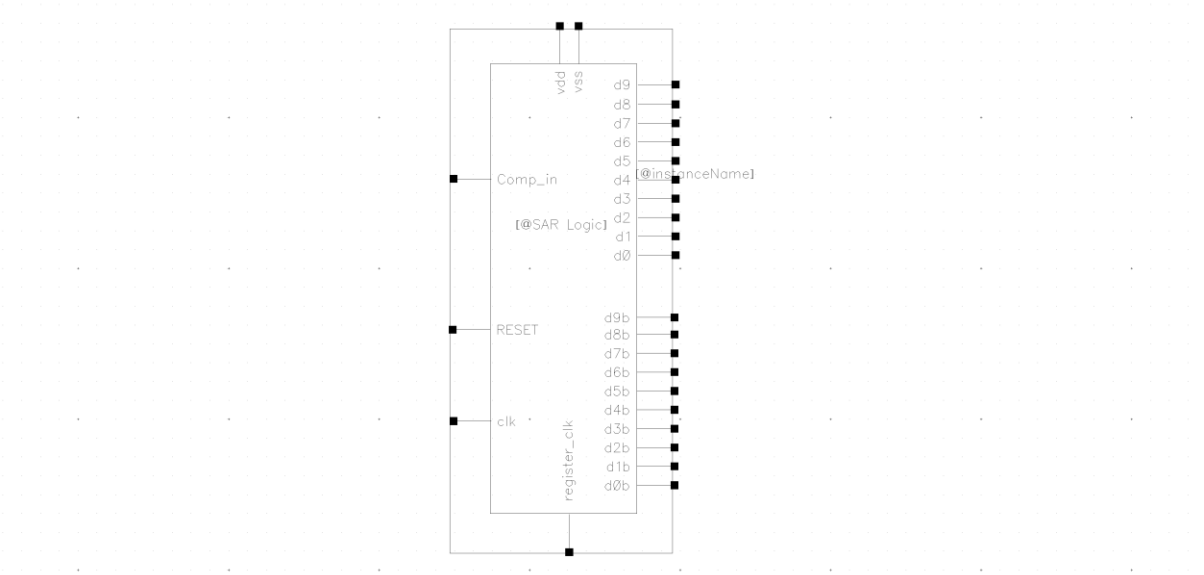


Figure 107: SAR Logic Symbol

4.4.5 Output Register

The previous SAR Register block is used only two more D-Flip flops are added to increase the bits from 8 to 10. The new circuit is given in Figure

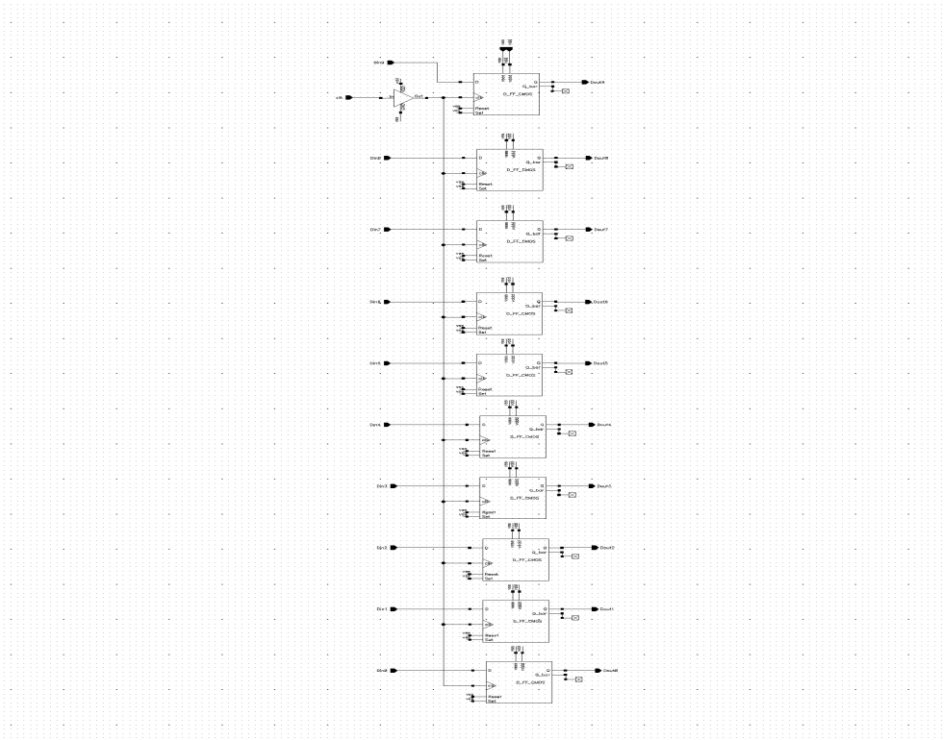


Figure 108:SAR Output Register

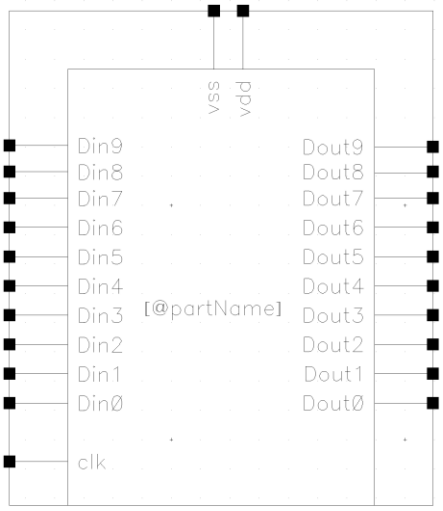


Figure 109: SAR Register Symbol

4.4.6 Ideal Output DAC

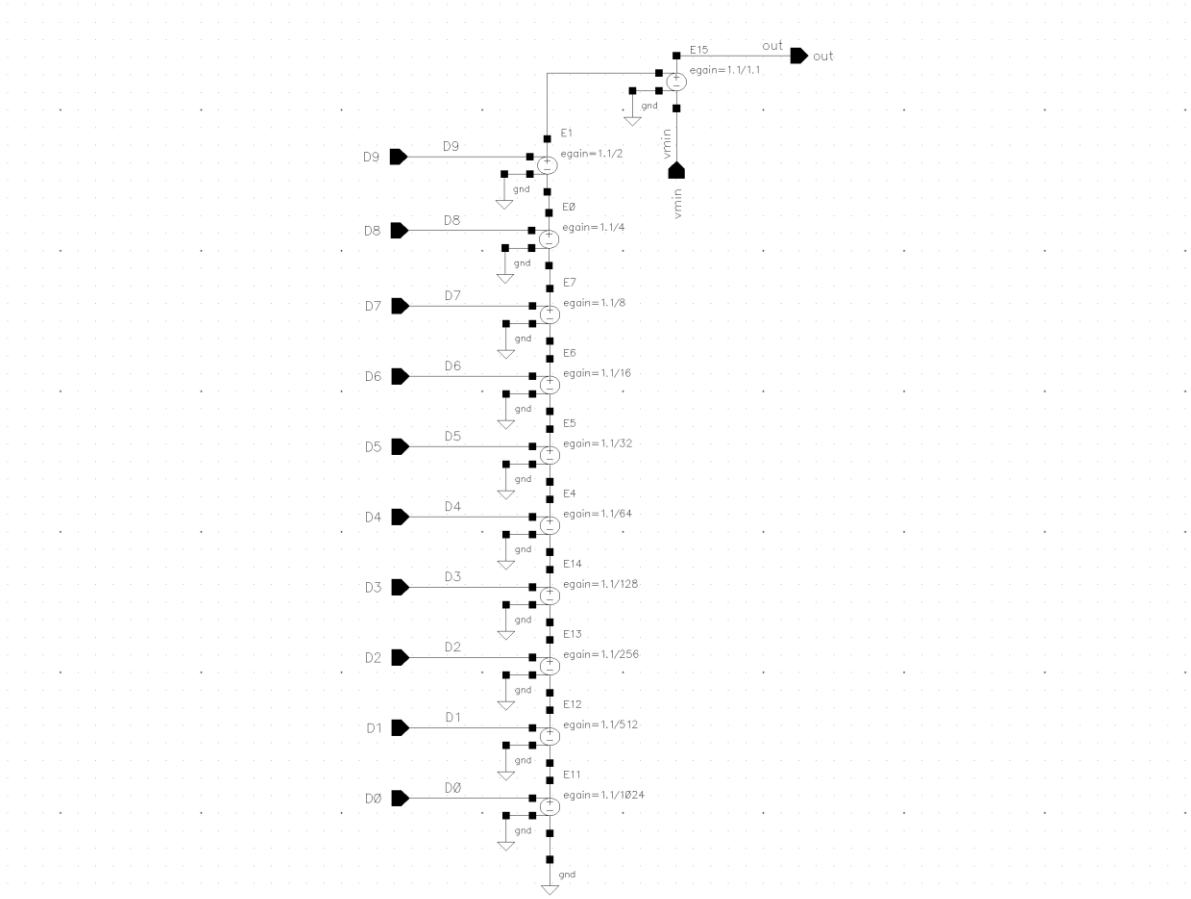


Figure 110: 10-bit Ideal output DAC

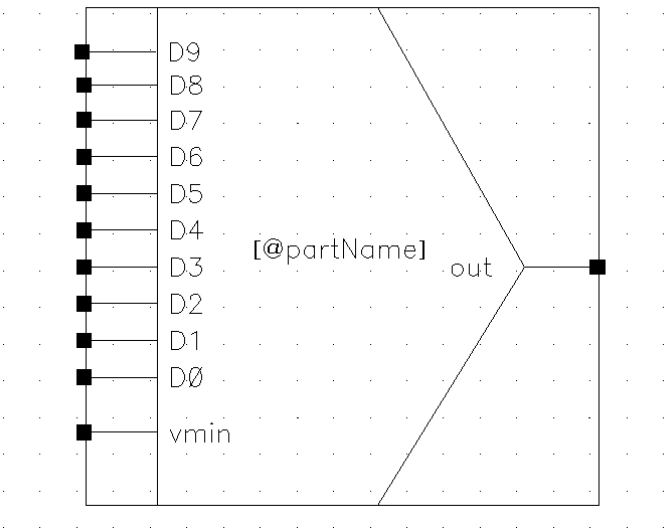
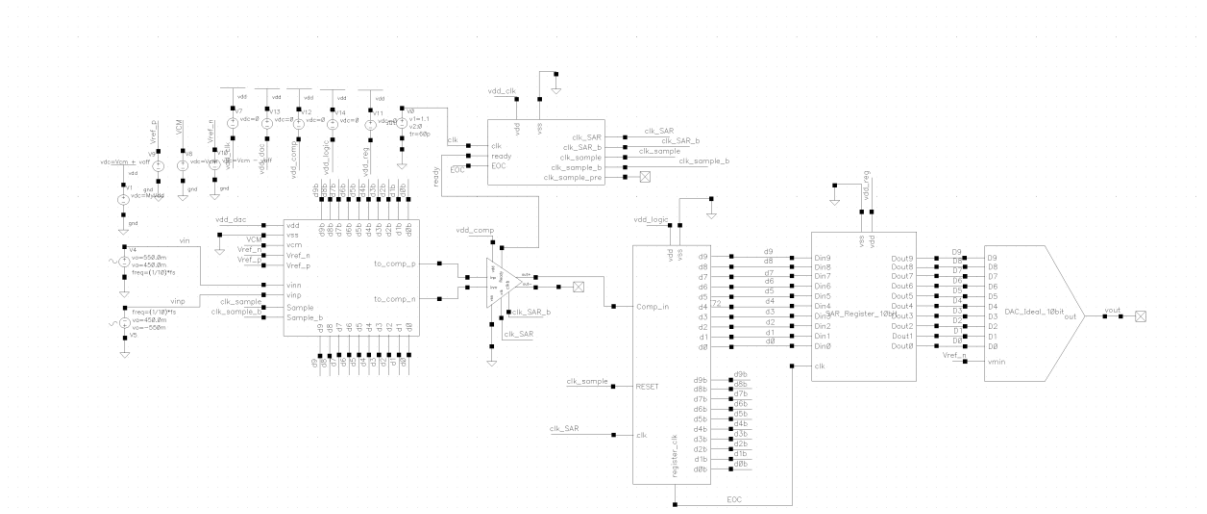


Figure 111: Ideal DAC Symbol

4.4.7 Complete Asynchronous 10-bit SAR ADC Testbench



112(a)

Design Variables

	Name	Value
1	xlc	6
2	x	11
3	Ca	32/31
4	Cd	71.2
5	Boot_m	30
6	tg_dac_pW	875n
7	tg_dac_pm	25
8	tg_dac_nW	500n
9	tg_dac_nm	20
10	SR_nmos	15
11	SR_outp_inv	50
12	SR_outn_inv	15
13	Vcm	550m
14	voff	450m
15	m_nand3	1
16	m_nand2	1
17	MyVdd	1.1
18	P_inv	6
19	N_inv	6
20	fs	20M

112(b)

Figure 112 (a): Testbench of the whole asynchronous SAR ADC, (b): Design Variables

4.4.8 Output of the 10 bit SAR

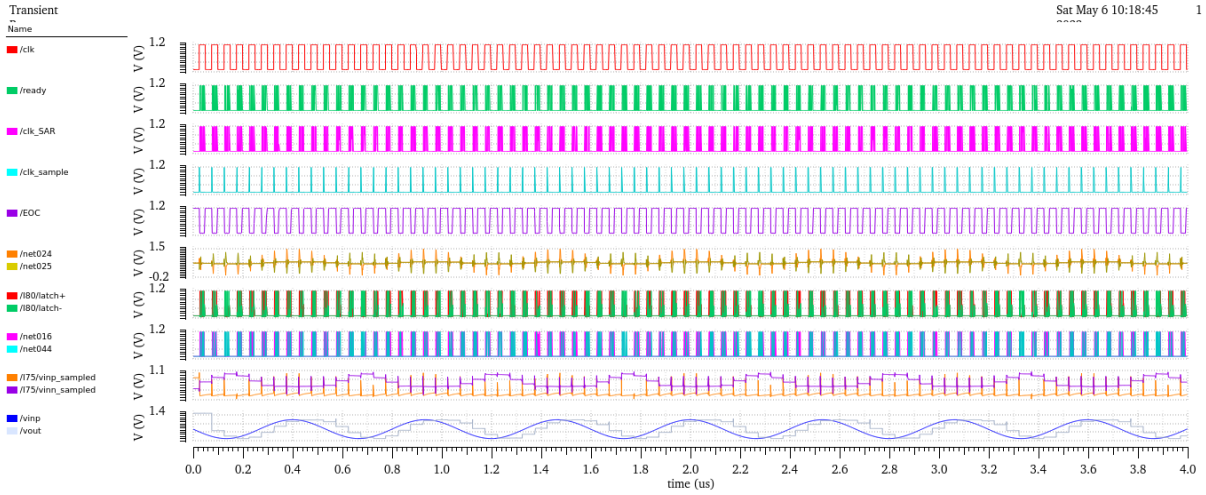


Figure 113: Transient waveforms of the asynchronous SAR ADC testbench

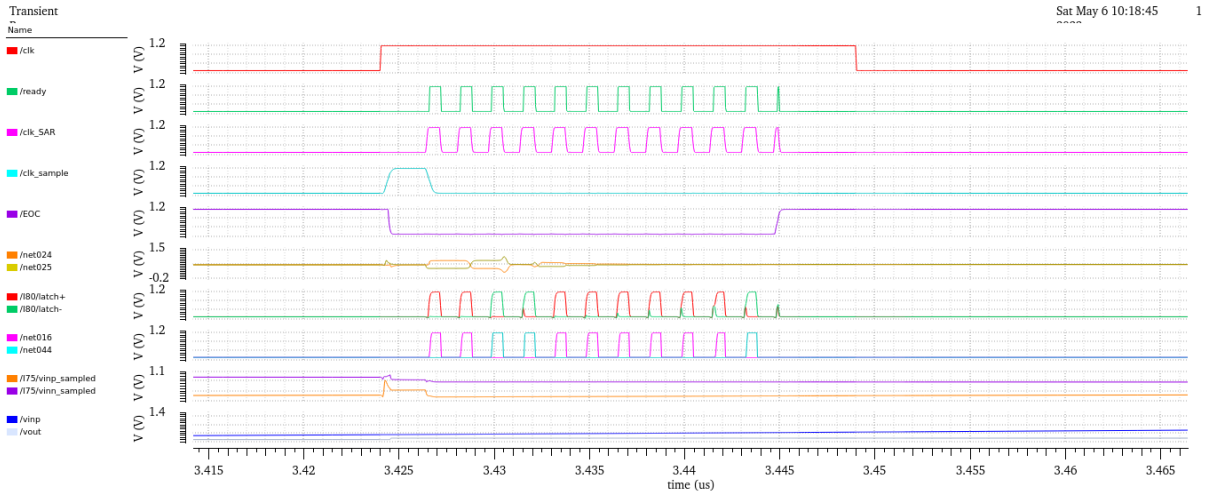


Figure 114: Waveforms of the asynchronous SAR ADC testbench during 1 conversion cycle

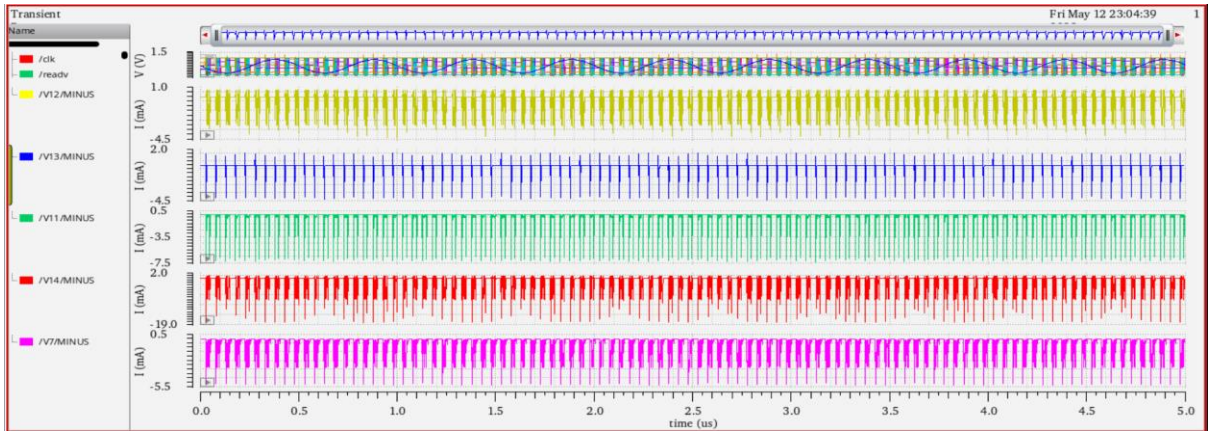


Figure 115: Current consumption for each block

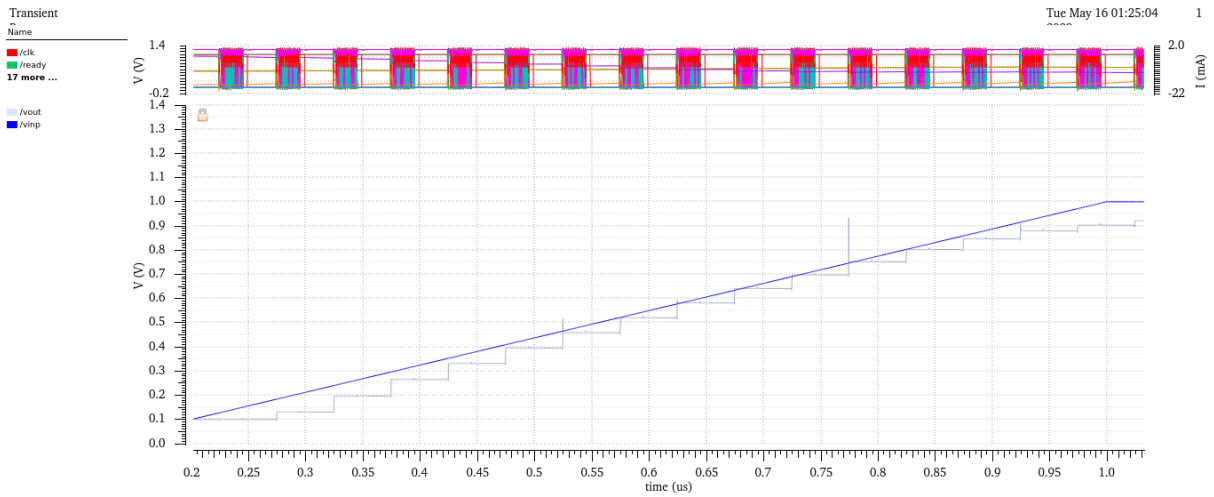


Figure 116: Transient response of the ADC for a Ramp Signal

These key metrics and parameters of the system are displayed in Table 14. The figure-of-merit (FOM) of the system is defined by equation (41). The aim of the design is to decrease the FOM, which mainly involves decreasing the total power consumption and improving the ENOB. The power is improved by using circuits that consume no static power like the two stage dynamic comparator, while theENOB is improved by using techniques like bootstrapped switching and highly sensitive strongarm latch design. The achieved FOM from the proposed SAR ADC is 2.277 fJ/conversion-step which is comparable to earlier asynchronous SAR ADC designs.

Calculating SINAD:

SINAD = 6.02 * ENOB + 1.76 dB

= 6.02 * 9.38 + 1.76 dB

= 56.5296 dB

Calculating SFDR:

SFDR = ENOB * 6.02 dB + 1.76 dB

= 9.38 * 6.02 + 1.76 dB

= 58.0388 dB

Calculating FOM: FOM = Total Power / (Sampling Rate * SINAD)

= 0.676 mW / (20 MS/s * 10^(SINAD/10))

= 0.676 mW / (20 MS/s * 10^(56.5296/10))

Note: In the calculation of FOM, the SINAD value should be converted from dB to linear scale (10^(SINAD/10)).

Evaluating the FOM numerically:

FOM ≈ 0.676 mW / (20 MS/s * 271.9927)

≈ 1.239e-5 mW / (MHz * 271.9927)

≈ 4.554e-11 mW / (MHz)

≈ 45.54 pW / (MHz)

Therefore, based on the given parameters, the calculated values are:

SINAD ≈ 56.53 dB SFDR

≈ 58.04 dB FOM

≈ 45.54 pW/MHz

Converting FOM from pW/MHz to fW/conversion:

FOM_fW = FOM_pW * 1e-3

= 45.54 pW / (MHz) * 1e-3

= 45.54 fW / (MHz)

Now, let's calculate the FOM in fJ/conversion:

FOM_fJ = FOM_fW * (1e-3 / frequency)

= 45.54 fW / (MHz) * (1e-3 / 20 MS/s)

= 45.54 fW / (MHz) * 5e-14 s = 2.277 fJ / (MHz)

Table 14: Performance Summary

Parameter	Value
Technology	UMC 65 nm CMOS
Power Supply	1.1 V
Resolution	10 bits
Sampling Rate	20 MS/s
Common-Mode Voltage	0.55 V
Differential Input Range	1.1 V
Sampling Unit Cap	71.2 fF
Bridge Capacitor	32/31
SINAD	56.53 dB
SFDR	58.04 dB
ENOB	9.38 bits
Total Power	0.676mW

Table 15shows how the total power is divided among the different blocks. Most of the power consumption come from the digital blocks, with the delay cells being the biggest contributor to

the high power. The power of the digital circuits usually scales down well with supply, since the dynamic power is directly proportional to VDD 2 as shown in equation (42). This allows the proposed asynchronous SAR ADC to have the potential to offer more power reduction in future design work.

Table 15: Power Consumption Per Block

Block	Power
Internal Clock Generator (including delay cells)	199.15 uW
SAR Logic	389.2 uW
Comparator	62.30 uW
DAC + Switches	26.15 uW
Total Power	676 uW

Conclusion and Future Work

A low-power 10-bit asynchronous SAR ADC with a 20 MHz clock input, designed in CMOS 65 nm technology and a voltage of 1.1 V is presented. This design uses an internal clock generator to control the conversion process by generating a clock signal for the rest of the circuit. A bootstrap switch is used to sample the differential input signal from the input signal and provide a high ENOB. Binary weighted charge redistribution capacitive DACs provide input levels for comparator comparison without consuming static power. The comparison is performed by a low power two stage comparator. The 's SAR logic block that generates digital code uses CMOS flip-flops to further reduce the power consumption, TSPC or TG D-Flipflops can be used. The measured ENOB system was 9.38bits, while consuming 676 uW of total power, the gave a FOM of 2.277 fJ/conversion step. Improvements can be applied to the design for better FOM. As shown in the results section, most of the 's power consumption comes from the digital blocks, so the power consumption can be reduced by lowering the supply voltage for these blocks or using other logic topologies such as dynamic CMOS logic. The other capacitive DAC topologies also offer lower switching energy due to the split capacitor arrangement and the monotonic switching method as described in reference [107]. Changing the switching scheme from the DAC would also require a redesign of the SAR logic block. Other internal clock generator topologies can also help the save power, as described in reference [106]. The proposed design shows that the asynchronous SAR ADC architecture can provide energy efficient ADC and FOM without using an oversampling clock.

Future Works

Here are the key learnings derived from the research and implementation:

- Asynchronous systems are advantageous in cases where supporting an oversampled clock is complex or not feasible. Asynchronous ADCs have simpler IO interfaces compared to synchronous data converters.
- The functioning of asynchronous SAR (Successive Approximation Register) logic relies on a comparator's decision to proceed with subsequent operations. This means that if one comparator "hangs," it can lead to a failure for the entire conversion. In contrast, in a synchronous system, a comparator failure affects only a single bit in the conversion.
- Asynchronous SAR logic does not guarantee automatic and proper DAC (Digital-to-Analog Converter) settling. The appropriate delays in the CLKC clock generator must be determined through precise transistor-level simulations.

- In an asynchronous SAR design, the comparator reset phase and DAC settling occur almost simultaneously. If the DAC settling time dominates, it may be possible to relax the comparator's performance requirements to save power.
- It is crucial to analyse the critical path through the digital logic and optimize the logic accordingly. Non-critical gates can be loosened to conserve power.
- When a comparator is combined with a transistor-based DAC, the transistors in the comparator need to be tuned. Their behaviour differs when driven by an ideal components DAC.
- Bootstrap circuits are necessary for front-end switches to enhance DAC performance.
- A binary-weighted capacitive DAC may not be the most suitable choice for an asynchronous SAR system with a resolution of 10 bits or higher. The advantages of speed and energy efficiency in the asynchronous system diminish due to DAC settling. Another approach, the split-array DAC, is therefore considered.

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[1] N. T. Tasneem and I. Mahbub, "A 2.53 NEF 8-bit 10 kS/s 0.5 μm CMOS neural recording read-out circuit with high linearity for neuromodulation implants," *Electronics*, vol. 10, no. 5, pp. 1–15, 2021.
   a. View at: Google Scholar

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