# REALISATION OF RECIEVER(RX) EQUALIZATION TECHNIQUES TO ENHANCE THE EYE-DIAGRAM FOR USB 3.2 AT 10 Gb/s SPEED

**THESIS SUBMITTED IN PARTIAL FULFILLMENT**

**OF THE REQUIREMENT FOR THE DEGREE OF**

**MASTER OF TECHNOLOGY**

**IN**

**VLSI DESIGN & MICROELECTRONICS TECHNOLOGY**


THESIS SUBMITTED BY

**DEBADITTYA DAS**

**University Registration No.: 154104 of 2020-2021**

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UNDER THE SUPERVISION OF

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**JUNE 2023**

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Thesis Title

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# ABSTRACT

In recent years, technology scaling and the demand for higher data rates have driven innovation at high-speed interfaces. To meet the requirements of ultra-low power and high-speed data rate signaling, integrated systems-on-chip have become essential components in modern computing systems. While traditional parallel links have been used for a long time, controlling the skew between clocks and data lanes in the link becomes increasingly challenging with faster data rates. To address this issue, faster serial links with reduced pin count and area have emerged as an alternative. High-speed serial IO standards like PCI-e, SATA, USB, TBT, DP, HDMI, and M-PHY have replaced traditional parallel links like PCI, serving multiple applications such as processor-to-processor or processor-to-peripheral communication.

A typical highspeed serial communication consists of two blocks namely the transmitter (TX) block and the receiver (RX) block and a medium through which the communication happens known as channel. However, as the data rates increase, these channels behave as lossy transmission lines due to different factors like skin effect, crosstalk, internal resistance of the transmission line, Inter-Symbol Interference and dielectric absorption of signals which severely degrades the transmitted data symbols.

To mitigate these losses, various techniques can be employed, such as using low-loss dielectric materials, optimizing the conductor size and spacing, employing shielding to reduce interference and crosstalk, and using equalization. Out of these, equalization being the most widely used technique in the industry postproduction. Equalization techniques are used at both the transmitter (TX) and the receiver (RX) end of the communication to compensate for signal distortion due to losses in the channel.

This thesis concentrates mainly on the realization and comparison of various techniques of equalization applied at the receiver (RX) end of communication for widely used serial highspeed communication protocol named USB (specifically USB 3.2). Presently, various industry standard equalization techniques and even the combination of two or more equalization techniques at the receiver (RX) end is studied, discussed, and performed in a lab environment to conclude as of which of these equalization techniques produces the best eye-diagram by compensating for the losses that occur in the channel at the industry level. All these studies are performed at a data rate of 10 Gb/s.

# ABBREVIATIONS

| | |
|---|---|
| **PCI-e** | Peripheral Component Interconnect express |
| **SATA** | Serial Advanced Technology Attachment |
| **USB** | Universal Serial Bus |
| **TBT** | Thunderbolt |
| **DP** | Decentralized Periphery |
| **HDMI** | High-Definition Multimedia Interface |
| **M-PHY** | MIPI Physical layer |
| **PCI** | Peripheral Component Interconnect |
| **IO** | Input/Output |
| **SerDes** | Serializer/Deserialize |
| **OEM** | Original Equipment Manufacturer |
| **SSP** | Super Speed Plus |
| **PAM** | Pulse Amplitude Modulation |
| **NRZ** | Non-Return-to-Zero |
| **CTLE** | Continuous Time Equalization |
| **DFE** | Decision Feedback Equalization |
| **FFE** | Feed Forward Equalization |
| **IC** | Integrated Circuits |
| **PCB** | Printed Circuit Boards |
| **SCSI** | Small Computer Systems Interface |
| **ISA** | Industry-Standard Architecture |
| **PCMCIA** | Personal Computer Memory Card Industry Association |
| **HSTL** | High-Speed Transistor Logic |
| **SSO** | Simultaneous Switching Outputs |
| **DMT** | Discrete Multitone Transmission |
| **DAC** | Digital to Analog Converter |
| **ADC** | Analog-to-Digital Converter |
| **FEC** | Forward Error Correction |
| **BER** | Bit Error Rate |
| **CP PLL** | Charged Pump Phase Locked Loop |
| **LC-VCO** | Inductance Capacitance Voltage Controlled Oscillator |
| **ISI** | Inter Symbol Interference |
| **HPC** | High-Performance Computing |
| **AI** | Artificial Intelligence |
| **TSMC** | Taiwan Semiconductor Manufacturing Company Ltd. |
| **AVIPSA** | Automated Validation of Internet Security Protocol and Applications |
| **HDL** | Hardware Description Language |
| **RFI** | Radio Frequency Interference |
| **CMOS** | Complementary Metal-Oxide Semiconductor |

| | |
|---|---|
| **ESD** | Electrostatic Discharge |
| **DDR** | Double Data Rate |
| **ADS** | Advance Design Systems |
| **LE** | Linear Equalizer |
| **CDR** | Clock Data Recovery |
| **PFD** | Phase-Frequency Detector |
| **LF** | Loop Filter |
| **PWM** | Pulse-Width Modulation |
| **VNA** | Vector-Network-Analyzer |
| **HFSS** | High-Frequency Structure Simulator |
| **PLL** | Phase- Locked Loop |
| **USB-IF** | Universal Serial Bus Implementers Forum |
| **USB-PD** | USB Power Delivery |
| **PHY** | Physical Layer |
| **LFPS** | Low-Frequency Periodic Signaling |
| **SSC** | Spread Spectrum Clocking |
| **EMI** | Electromagnetic Interference |
| **SNR** | Signal-to-Noise Ratio |
| **VNA** | Vector Network Analyzer |
| **NEXT** | Near End Cross Talk |
| **FEXT** | Far End Cross Talk |
| **DJ** | Deterministic Jitter |
| **DCD** | Duty Cycle Distortion |
| **HPJ** | High Probability Jitter |
| **RJ** | Random Jitter |
| **DDJ** | -Data Dependent Jitter |
| **SJ** | Sinusoidal Jitter |
| **PJ** | Periodic Jitter |
| **UUGJ** | Uncorrelated Unbounded Gaussian Jitter |
| **CBGJ** | Correlated Bounded Gaussian Jitter |
| **UI** | Unit Interval |
| **FB** | Feedback Filter |
| **PFAG** | Pulse Function Arbitrary Generator |
| **DUT** | Device Under Test |
| **CLB** | Compliance Load Board |
| **SMA** | Subminiature Version A |
| **CP** | Compliance Patterns |
| **PRBS** | Pseudo Random Binary Sequence |
| **EW** | Eye Width |
| **EH** | Eye Height |

# CONTENTS

# Chapter 1
# Introduction

## 1.1 Chapter Overview

The transmitter (TX) and receiver (RX) circuits in high-speed serial links use physical medium for communication between the device I/O interface and the host I/O interface and vice-versa. These channels are specifically designed for high-speed operation and are utilized to send and receive data. The channel through which the data is transmitted is referred to as the medium, and in an optimal scenario, it would be represented by a wire behaving as a short circuit. However, as data rates escalate, the wires begin to operate as lossy transmission lines, which can lead to severe degradation of the transmitted data symbols. To counteract these non-idealities caused by the channel, equalization is a widely used technique. [1]

This chapter focuses on the motivation behind the use of different equalization techniques used in USB based serial communication to compensate for the losses to the data signal during transmission. Also, the objectives of using these equalization techniques during validation process of USB based products post-production to ensure the proper transfer of data between the device and host is discussed briefly. Lastly, the structure of the thesis work that is carried out is discussed to give reader an idea of the flow of this thesis paper.

## 1.2 Motivation

The progress in semiconductor processing technology has enabled processors to handle vast amounts of data. To take full advantage of this development, I/O links must also increase their bandwidth while minimizing the impact on pin count, area, and power consumption. Traditional parallel links have been in use in circuits for a long time, but with faster data rates, controlling the skew between clocks and data lanes in the link becomes difficult. A viable alternative is to use faster serial links, which require fewer pins and less area [2]. High-speed serial I/O standards such as PCI-e [3], HDMI [4], and USB [5], have replaced traditional parallel links and are utilized in multiple applications, such as processor-to-processor or processor-to-peripheral communication. Serial I/O communication poses some challenges, including channel loss, Inter-Symbol Interference (ISI), crosstalk, and increased complexity in the receiver (RX) to facilitate clock recovery from the data stream [2].

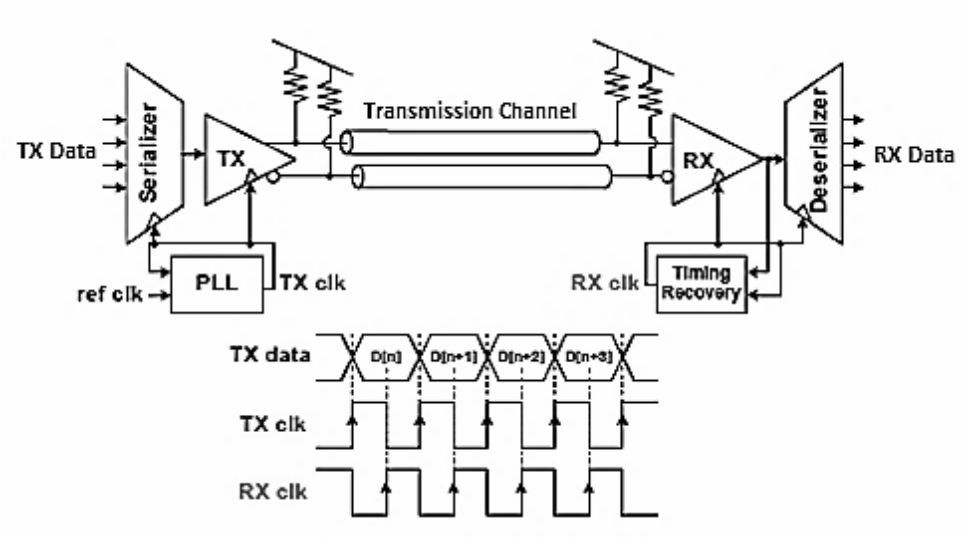


Fig.1.1: High speed serial IO link [2].

The diagram in Figure 1.1 displays the primary constituents of a standard high-speed serial link (SerDes). As there is a constraint on the number of I/O pins in chip packages and printed circuit boards, a transmitter (TX) converts incoming parallel data into a serial format, while a receiver (RX) converts high-speed serial data into parallel data [2]. The data signals that are transmitted via these channels are affected by the channel loss, ISI, cross-talks etc. that causes the signals to lose the amplitude. This is the reason behind the application of equalization in both transmitter (TX) and receiver (RX) end. Equalization boosts the amplitude of the high frequency component of the signal to compensate for the loss during transmission.

## 1.3 Objectives

There are different industry accepted equalization techniques which are used to validate the high-speed serial link communication between the host and device and vice versa.

- This thesis concentrates on comparison of different receiver (RX) equalization techniques and different combinations of those techniques. The comparison is based on eye-diagrams and signal amplitude obtained from the data signals passing through the channel.
- The objective of this thesis is to have a better understanding of equalization and more specifically receiver (RX) equalization for USB standard-based product validation at a high speed of 10 Gb/s and conclude finally as to which equalization technique works the best to mitigate the channel losses and helps to study the communication link in a better way.
- The objective of this thesis is also to give the reader an overall perspective of the factors taken into consideration while validating an USB standard-based product in any industry which deals with high-speed serial link communication.

## 1.4 Structure of Work

In this section, the outline of the thesis work is mapped with brief introduction about each of them.

- **Chapter 2. Literature Review:**

  This chapter contains brief reviews of various thesis papers, journals, book chapters, books and publications related to High-speed serial links, Equalization techniques and USB. These papers have inspired and supported the thoughts required to complete this thesis paper.

- **Chapter 3: Architecture of High Speed SerDes:**

  This chapter describes the fundamental concept and architecture of High- speed SerDes. Different blocks and their constituents and their operations are covered in detail.

- **Chapter 4: USB-3.2:**

  This chapter concentrates mainly on the USB-3.2 and everything about its architecture and other necessary topics that will help the reader to understand the focus of this work. This chapter also compares the USB 3.2 with its predecessors.

- **Chapter 5: Equalization Techniques:**

  This chapter discusses different equalization techniques on both the transmitter (TX) and the receiver (RX) end. But the focus will be on the equalization techniques on the receiver (RX) end.

- **Chapter 6: Measurement and Results**

  This chapter contains information about the measurement set-up and the different eye-diagrams obtained when various equalization techniques are implemented, and data signals are sent via channel.

- **Chapter 7: Conclusion and Future Works**

  This chapter concludes all the findings of the work carried out and the future works that can possibly be accepted and applied by the industry.

# Chapter 2

# Literature Review

## 2.1 Chapter Overview

This chapter contains detailed review of different book chapters, papers, journals related to topics like data transmission, high speed serial link, SerDes architecture, different versions of USB and equalization. These documents fueled the knowledge required to complete this thesis. Section 2.2 presents a brief history of high-speed serial links, its comparison with its parallel counterpart, challenges related to channel losses in high-speed communication, differential signaling and SerDes Architectures and Applications. Section 2.3 contains review of different papers related to analysis of USB 3.2 architecture, analysis of predecessor versions and their physical layers and architectures. Section 2.4 finally, contains brief review of different research works having information about different equalization techniques, their significance, why and where they are used in both transmitter (TX) and receiver (RX) block and proposed ideas to increase the equalizer's efficiency by putting additional circuitry or by enhancing the existing circuit.

## 2.2 High Speed Serial Link

### 2.2.1 Brief History of High-Speed Serial Links

In paper [6] it is mentioned that in the past, circuit design primarily relied on Transistor-Transistor Logic (TTL). More complex integrated circuits (ICs), such as multi-bit registers and counters, were created by discrete gate ICs communicating with each other using parallel communication on printed circuit board (PCB) assemblies. However, the alignment of these circuits for external communication was challenging. As a result, serial ports became the standard for communication between boxes in early computers. Over time, alignment issues were resolved, and high-speed parallel printer ports became more common. Parallel technologies, such as Industry-Standard Architecture (ISA) [7], Small Computer Systems Interface (SCSI) [8], Peripheral Component Interconnect (PCI) [9], and Personal Computer Memory Card Industry Association (PCMCIA) [10], evolved. Despite these advancements, serial technology remained prevalent. Ethernet and Token Ring became popular in many applications, with the latter adapted to work on category 5 (Cat 5) wire. Parallel technologies faced challenges in accommodating new interface demands, and standards like PCI 33 evolved into PCI 66 to support more exotic signaling. However, attempts to support parallel technology, such as using low-swing standards like High-Speed Transistor

Logic (HSTL), were not very successful. Meanwhile, Ethernet speeds increased from 10 Mb to 100 Mb to 1000 Mb/s, making it highly desirable for desktop use.

[6] also mentioned that around the same time, the fractional phase detector was introduced, which boosted serial interface speeds to the multi-gigabit range. This made serial technology a strong contender, especially as a backplane technology. As serial pin count and simultaneous switching outputs (SSO) improved, multi-gigabit serial became the preferred option on PCB assemblies, ultimately replacing parallel technology.

### 2.2.2 Serial Vs parallel Communication

In [11], the author discussed an elaborated comparison between serial and parallel communication based on few parameters as follows:

| **Parameters** | **Serial Communication** | **Parallel Communication** |
|---|---|---|
| Bit transmission | Serial transmission involves the transfer of a single bit of data per clock pulse. | Parallel transmission involves the transfer of 8 bits of data per clock pulse. |
| Performance | Due to the transfer of only one bit per clock pulse in serial transmission, its performance is typically slower than that of parallel transmission, which can transfer 8 bits per clock pulse. | Parallel transmission is generally considered to be more efficient in performance than serial transmission because it can transfer 8 bits per clock pulse. |
| Complexity | Serial transmission is typically less complex than parallel transmission. | Parallel transmission is generally considered to be more complex than serial transmission. |
| Wiring Complexity | Serial communication typically requires less channel and less wiring resulting in less wiring complexity. | Parallel communication has more wiring and channels and is more complex than serial communication. |

| | | |
|---|---|---|
| Signal Integrity | Serial communication is less susceptible to noise and signal degradation as compared to parallel communication since the data are transmitted via same channel | Parallel communication on the other hand is more susceptible to noise and signal degradation because each bit is transferred on separate wires which causes crosstalk between the data signals |
| Data Rates | Can achieve higher data rates compared to parallel communication, particularly over long distances because the signals are less degraded by noise. | Parallel communication links cannot achieve higher data rates for long distance communication because of lossy channels. |
| Preference | Serial Transmission is preferred for long distance transmission | Parallel Transmission is preferred only for short distance. |
| Cost Efficiency | Serial transmission requires only a single link, making it relatively easy to implement without incurring significant costs. As a result, it is often considered to be a cost-efficient option | Parallel transmission typically requires multiple links, resulting in higher implementation costs and making it less cost-efficient than serial transmission. |

### 2.2.3 SerDes Architecture and Applications

According to [12], when evaluating SerDes devices, many system designers focus solely on speed and power consumption without considering the internal architecture of the SerDes and how it processes data. However, the internal architecture of the SerDes can greatly impact system parameters such as topology, protocol overhead, data formatting and flow, latency, clocking and timing requirements, and the need for additional buffering and logic, which can ultimately affect system cost, performance, and efficiency.

Also [12] , said that there are four distinct SerDes architectures that have evolved over the years to address specific system design issues: parallel clock SerDes, 8b/10b SerDes, embedded clock

bits (also known as start-stop bit) SerDes, and bit interleaving SerDes. The inner workings of these architectures, their differences were explored and demonstrated how each is suited to specific applications in today's industry.

In paper [13] it is presented a high-speed wireline communication system implementation utilizing Discrete Multitone (DMT) transmission. The study included a theoretical analysis of channels typically employed for SERDES chip-to-chip communication, highlighting the benefits of DMT technology, such as improved spectral efficiency and simplified transceiver design due to DMT's pseudo-narrowband characteristics. Simulation results demonstrated that DMT can achieve higher data rates than traditionally used non-return-to-zero (NRZ) and pulse-amplitude modulation (PAM) techniques, even with typical channel correction circuitry such as continuous-time linear equalizers (fs) and decision-feedback equalizers (DFEs). Additionally, a combined bit-loading/power allocation and transmit side equalization algorithm is presented to improve the system's data rate and reduce its bit error rate. The measurement results in [13] included a demonstration of a digital-to-analog converter (DAC) and analog-to-digital converter (ADC) test bed operating under realistic conditions for chip-to-chip communication with a data rate exceeding 250 GB/s, including sufficient overhead for forward-error-correction (FEC) coding needed to reduce the bit-error rate (BER).

As IoT and Cloud Computing continue to evolve, the data center is experiencing an increase in bandwidth demands, resulting in the development of new 112 Gb/s electrical interface standards for wireline communication. To maintain compatibility with existing 56 Gb/s standards, PAM4 is the chosen signaling method. Paper [14] presented the design and implementation of a 112 Gb/s PAM4 wireline receiver (RX) test-chip, which was implemented in FinFET technology. The receiver (RX) 's architecture included a four-stage continuous-time linear equalizer (CTLE), a peaking capacitance buffer, a 56 GSa/s time-interleaved 7-bit SAR ADC, DSP, and adaptation loops.

The study in [15] , reported the design of a high-performance 3 GHz charge pump phase-locked loop (CP PLL) in TSMC 28nm CMOS technology, featuring a low phase noise LC voltage-controlled oscillator (LC-VCO) and high accuracy charge pump (CP). The paper [15] also addressed nonideal effects and provides corresponding solutions for CP and LC-VCO. Post-layout simulation results indicated that the PLL can achieve 0.86 ps rms jitter and a power consumption of 13 mW at 3 GHz.

### 2.2.4 Channel Noises

Paper [16] mentioned that the communication industry is continually evolving towards higher speeds, lower power consumption, and bigger data rates. While Ethernet has reached its peak, optical interconnects have been integrated into electronic devices and chips to support multi-gigabit rates, and wireless telecommunications are transitioning towards the 5G era. However, these advancements have resulted in new challenges such as crosstalk, refraction, and Inter-Symbol Interference (ISI) that can affect Signal Integrity. Maintaining Signal Integrity is crucial for researchers involved in designing high-speed and big data systems. [16] also mentioned that ISI is an unavoidable problem in both wireless and wired systems, where reflections of signals and multipath propagation cause ISI. One of the most effective ways to combat ISI is equalization. As a signal travels from the transmitter (TX) to the receiver (RX), it is distorted by the channel and other noises. The equalizer's job on the receiver (RX) end is to use filters to recover the original signal from the distorted signal. Equalization is widely used to mitigate ISI distortion in optical, PCB backplanes, and cable channels, among other applications. Fig.2.1 gives an oversight of ISI effect

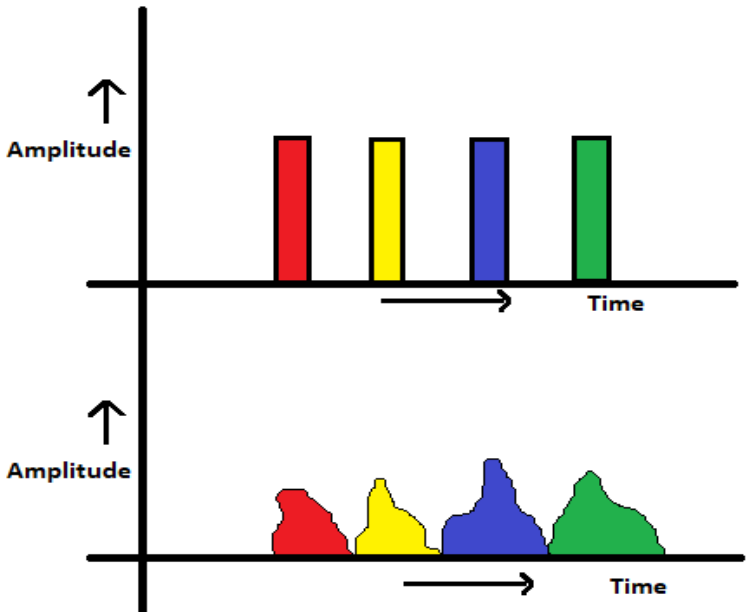


Fig. 2.1: Effect of Inter symbol Interference on data bits [16].

### 2.2.5 Latency

Paper [17] considered throughput and latency to be two critical factors in context of High-Performance Computing (HPC), Artificial Intelligence (AI), and high-frequency trading applications, particularly for larger capacitive loads. The latency part, which must be low for such applications to perform effectively was under the limelight. To reduce overall latency without

affecting the Serializer/Deserializer (SerDes) throughput, the function of each transceiver component and implemented circuits that address latency was examined. Some conventional transceiver blocks had been replaced with a proposed architecture that significantly reduced associated latency. Paper [17] also offered a detailed account of the implementation, including circuit simulation up to the extracted netlist level. A 20Gb/s transceiver using Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) 28nm HPC+ technology was developed, focusing solely on the transmitter (TX) portion and as a result, Significant latency reduction was observed as compared to another conventional transmitter (TX)s.

### 2.2.6 Differential Signaling

In paper [18] it is mentioned that a technique called single-ended signaling is utilized where a dedicated transmission line is used for each bit on the bus. Signal integrity maintenance, however, becomes challenging due to the noise generated by digital systems, crosstalk, and nonideal current return paths with higher data rates. In single-ended signaling, the bus clock receives each data bit transmitted on a single transmission line. The received waveform is compared to a reference voltage $V_{ref}$, and a logic 1 is latched in if the voltage is greater than $V_{ref}$, otherwise, it is latched in as a logic 0. If the magnitude of the noise coupled onto the driver, receiver (RX), transmission lines, reference planes, or clock circuits is significant, the relationship between the transmitted waveform and $V_{ref}$ can be distorted, resulting in bit errors. How noise can cause uncertainty in determining a logic 0 or 1 is depicted in Figure 2.1.

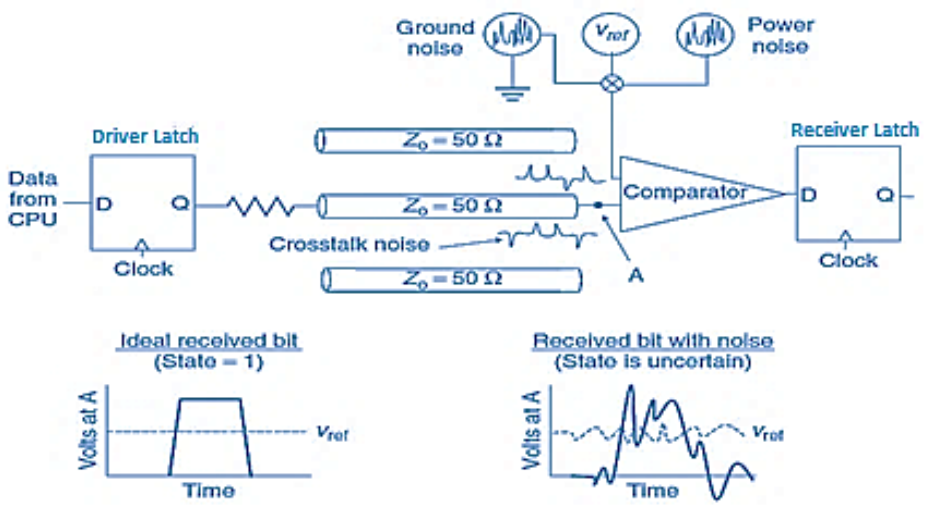


Fig. 2.2: How system noise can severely degrade signal integrity on single-ended buses. The ideal versus noisy receiver (RX) voltages compared to the reference voltage [18].

Also [18] mentioned a method that significantly mitigates the impact of system noise is to use a pair of transmission lines for each bit on the bus. The two transmission lines are driven in opposite directions (180 degrees out of phase) in the odd mode, and the voltage difference between them is utilized to restore the signal at the receiver (RX) with the aid of a differential amplifier. This method is commonly known as differential signaling and is shown in Figure 2.2.

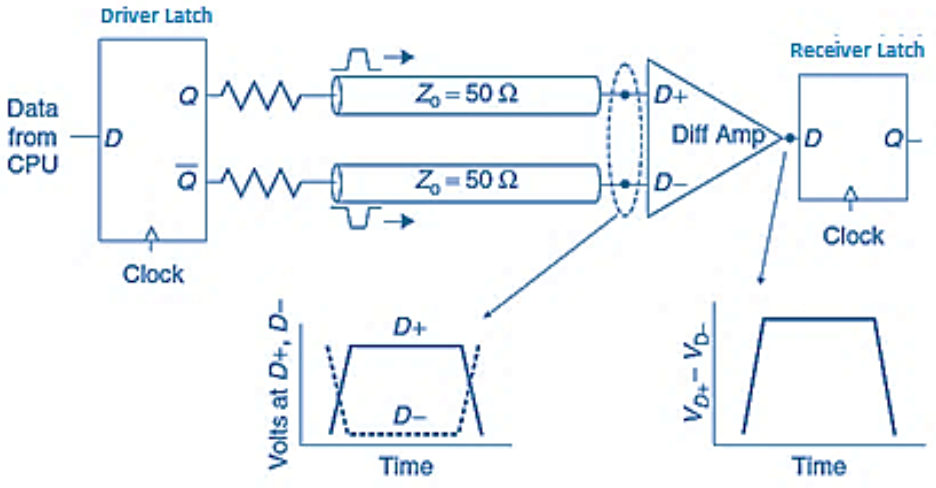


Fig. 2.3: Differential signaling where each bit is transmitted from the driver to a receiver (RX) using a pair of transmission lines driven in the odd mode. The signal is recovered at the receiver (RX) with a differential amplifier [18].

## 2.3 Universal Serial Bus (USB)

In paper [19] it is mentioned that the use of USB 2.0 device controllers in electronic devices such as mobile devices, external hard drives and gaming controllers has become very common, which calls for the need to develop an efficient USB 2.0 device controller architecture to address the battery life concerns in current devices. Explanation on the functionality of a USB 2.0 device controller and the main reason behind its power inefficiency was given. Thereafter, an architecture that employed clock gating techniques and a fine-grained power gating approach based on data traffic to enhance power efficiency was presented. The design was based on the open-source USB 2.0 device controller soft-core from the Open Cores Organization.

In paper [20], an analysis of why USB 3.0 is a perfect upgrade from its predecessor was made. The USB 3.0 technology offers faster transmission speeds of up to 5 Gb/s, which is ten times faster than USB 2.0 (480 Mb/s). This increased speed translates to reduced transmission times for data. Other features of USB 3.0 include reduced power consumption and backward compatibility with USB 2.0. In November 2008, the USB 3.0 Promoter Group completed the specification of version 3.0 and transitioned it to the USB Implementers Forum (USBIF), which is the managing body of

USB specifications. This move made the specification available to hardware developers for implementation in future products. One of the new features of USB 3.0 is the "SuperSpeed" bus that provided a fourth transfer mode at 5.0 Gb/s. Although the raw throughput is 4 Gb/s, the specification deemed it reasonable to achieve 3.2 Gb/s (0.4 Gb/s or 400 Mb/s).

Paper [21] mentioned USB as a widely used interface for connecting external computer peripherals. For high-speed data transfer, dedicated hardware implements all the functions of the USB interface. It is a standard for wired connection between two electronic devices, with a maximum speed of 5Gb/s. The cable has a connector at either end, with one end being the same across all USB cables, while the other end is specific to the mobile device. The USB standard has evolved over time, with different versions including USB 1.0, 1.1, USB 2.0, and USB 3.0. The USB Host Controller manages the transmission, reception, and flow control of packets on the bus. Investigation on the architecture of USB 3.0, including its different layers and power management is finally done.

In [22], a secure USB mechanism that prevented leakages of authentication data and eliminated the need to compare authentication data for smart human care services, which has been a significant issue with existing flash drives was proposed. The proposed mechanism ensured confidentiality, integrity, authentication, and access control and protects data from impersonation, man-in-the-middle, replay, and eavesdropping attacks by malicious attackers. Formal verification using the AVISPA tool confirmed the security of the proposed mechanism. Therefore, it was expected that a safer and more secure USB flash drive can be produced using the mechanism proposed.

Paper [5] focused on the design of the physical layer of USB3.0 with Super Speed capability, which included the PCI express and PIPE interface. The design in this paper [5], enabled data to be transferred serially from transmitter (TX) to receiver (RX) at 2.5 Gb/s and generated a clock that ran at a frequency of 125MHz to transfer data in parallel interfaces. The authors also proposed an architecture for the USB3.0 physical layer, which was implemented using Verilog HDL in Xilinx Vivado 2017.4.

In [23], the radio frequency interference (RFI) caused by the universal serial bus 3.0 connector to a nearby antenna was investigated. A model of the connector radiation as an equivalent stripline-fed slot antenna, which is based on analyzing the common mode current path on the connector structure was also proposed. This model allowed replacing the original connector radiation source with an equivalent magnetic dipole source that is directly correlated with the physical quantity on

the connector. Reciprocity theorem to use the equivalent dipole source for predicting the coupled noise power to the antenna was applied in [23]. The proposed model and mechanism are validated using full-wave simulation and measurement. Application of the magnetic dipole source for estimating RFI in a real laptop system was demonstrated.

In paper [24], the impact of mechanical tolerances on skew in USB 2.0 cables was examined in. A full-wave simulation of the cable cross section was used to determine the contribution of tolerances to skew. Using a fractional factorial experimental design, the contributing factors and interaction terms were identified, and Monte Carlo simulations were conducted to investigate each factor's sensitivity to skew. By employing the design of experiments approach, the relationship between mechanical tolerances and skew was recognized. Furthermore, a systematic approach was used to determine the relationship between skew and emission. The results indicated that a net skew of approximately 20-30 ps resulted in a 4-5 dB increase in emission above 350 MHz.

According to [25], The USB 3.2 specification defined the latest iteration of the USB industry standard. It outlined the protocol definition, bus management, and programming interface required to develop systems and peripherals that adhere to this standard. USB 3.2 was designed to improve the performance of USB 3.1 by adding dual-lane support to the USB Type-C cable and connector, thereby providing more bandwidth for devices like Solid State Drives and High-Definition displays. The specification referred to Enhanced SuperSpeed as a set of features or requirements that apply to USB 3.x bus operation. Differences from USB 3.0's SuperSpeed features or requirements were identified as Superspeed Plus (or SSP) features or requirements. The primary goal of USB 3.2 was to enable devices from different vendors to interoperate in an open architecture while leveraging the existing USB infrastructure, such as device drivers and software interfaces. The specification was meant to enhance the PC architecture, from portable and business desktop environments to simple device-to-device communications. It was intended to give OEMs and peripheral developers enough flexibility for product versatility and market differentiation without losing compatibility or carrying obsolete interfaces.

## 2.4 Equalization Techniques

The study in [26], focused on the operation of a 4Gb/s serial channel over copper wires. To cancel out the frequency-dependent attenuation caused by skin-effect resistance in copper wires, a 4GHz FIR equalizing filter was incorporated into a differential transmitter (TX). The equalizer achieved a flat frequency response to within 5% over the 200MHz to 2GHz bandwidth, even over wires with high-frequency attenuation of 6dB. Most of the transmitter (TX) operates at 400MHz, except

for the final stage. The transmitter (TX) output stage uses a stable 10-phase 400MHz clock to sequence an array of drivers that implement the FIR filter. The concept of digital-signal equalization was presented in [26] ,the system design and circuit design of the equalizing transmitter (TX) was described too, and finally, simulation results from a 0.5mm CMOS transmitter (TX) operating at 4Gb/s were presented.

To address limitations in data transmission caused by modal dispersion in fiber-optic links, [27] proposed two different equalizer implementation approaches to improve transmission capacities. The equalizer's building blocks, including a multiplier cell, a delay line, and an output buffer stage, are fully integrated on a 0.18-µm CMOS process. In [27] comparison between performance of a passive LC delay line and an active inductance peaking delay line for continuous-time tap-delay implementation against process variation and power consumption were made. Additionally, a delay-locked loop was proposed to counter delay variations caused by changes in the process corner. After transmission through a 500-m multimode-fiber channel, a 10-Gb/s nonreturn-to-zero signal is received, and signal impairment due to differential modal delay was successfully compensated using both feed-forward equalizers.

A 7-tap 40 Gb/s feed forward equalizer (FFE) is presented in the [28], which has been fabricated using a 65 nm standard CMOS process. Broad banding and calibration techniques were implemented to ensure high-speed operation while keeping power consumption low. The chip consumed 80 mW from a 1 V supply, and featured ESD protection for 40 Gb/s I/Os, as well as an inexpensive plastic package to bring it closer to commercial viability. The tap delay frequency response variation was measured to be less than 1 dB up to 20 GHz, and the tap-to-tap delay variation was less than 0.3 ps. The chip exhibited more than 50% vertical and 70% horizontal eye opening from a closed input eye. The use of a CMOS process allowed for further integration of this core into a decision feedback equalizer or a clock and data recovery/demux based receiver (RX).

In [1], equalization techniques for mitigating Inter-Symbol Interference (ISI) in high-speed communication links were discussed. The paper covered both transmit and receive equalizers and included the presentation of high-speed circuits for implementing them. Also, in [1], it was demonstrated that a digital transmit equalizer was the easiest to design, while a continuous-time receiver (RX) equalizer usually delivered better performance. Decision feedback equalizer (DFE) was described, and the loop latency issue was addressed. Additionally, techniques for adaptively setting the equalizer parameters were also presented.

In [29], considerations and decisions involved in designing equalization circuits for USB 3.0 SuperSpeed transceivers were outlined. Different interconnect channels and their electrical characteristics, the USB 3.0 specification requirements that impacted equalizer optimization, the parameters that defined equalizer behaviour and their recommended operating ranges, and the challenges and solutions for equalizer training implementation were also covered. While the USB 3.0 specification provides guidelines for SuperSpeed transceiver design, [29] offered additional insights and recommendations for transceiver designers dealing with equalization.

In paper [30], the author said that the difference in speed between on-chip and off-chip communication has widened as the IC process technology has shrunk to improve chip performance. On-chip circuit speed has surpassed off-chip communication speed, limiting the performance threshold of systems with multiple ICs. To address this gap, I/O interfaces like PCI-Express, USB 3.0, and DDR3 use high-speed transceiver systems that operate in the Giga-Hertz range. However, the copper interconnect on a motherboard backplane cannot support data rates, leading to signal integrity issues with nonideal effects introduced by the channel. To compensate for high-frequency losses introduced by the channel, a Continuous-Time Linear Equalizer (CTLE) was used at the receiver (RX) front-end. The implementation of CTLE was typically limited to first-order, but second-order CTLE offered incremental peaking gain when dealing with channels of high losses. Paper [30], therefore presented the characteristics and theoretical circuit analysis of first-order and second-order CTLEs, both designed to address a 5Gb/s data rate transmission. An arbitrary 20-inch channel was used as a test bench to compare the performance of the two equalizers. Simulation results demonstrated an improvement in receive eye voltage opening and insertion loss for second-order CTLE but with degradation in terms of receive eye time opening, jitter, and amplitude noise.

In paper [31], a USB 3.0 compatible transmitter (TX) and a corresponding receiver (RX) linear equalizer are presented, with an exploration of the architecture and circuit design techniques utilized to satisfy strict overall link design requirements. The output voltage amplitude and de-emphasis levels of the transmitter (TX) are programmable, and the output impedance is calibrated to 50 Ω. A programmable receiver (RX) equalizer was also presented, designed to compensate for channel losses, and employed alongside a DC offset compensation scheme. The equalizer operated at 6.25 GHz and provides 10 dB overall gain equalization, with 5.5 dB peaking at the maximum gain setting. The layout area of the transmitter (TX) core was 400 μm x 210 μm, and the equalizer core was 140 μm x 70 μm, designed using a well-established 65 nm complementary metal oxide semiconductor process. At a data rate of 5 Gb/s, the power consumption of the transmitter (TX)

and the equalizer were 55 mW and 4 mW, respectively, from a 1.2 V supply. The target application for these high-speed blocks was the implementation of the critical part of the physical layer, which defined the signaling technology of SuperSpeed USB3 PHY.

In Paper [32], the author focused on optimizing equalization architecture for high-speed serial communication, specifically for 25Gb/s or above backplane communication. The Advance Design Systems (ADS) Channel Simulator was used to analyze the high-speed backplane channel by examining its frequency and impulse responses. Various equalization architectures, including the high frequency boost values of linear equalizer (LE) and tap coefficients of decision feedback equalizer (DFE), were analyzed in detail. The results demonstrated that using a combined LE/DFE yields much better performance compared to using LE or DFE separately, with only a slightly increased complexity cost.

In paper [33] it is mentioned that low-power equalization was still in high demand for wireline receiver (RX) s that operate at high speeds on copper media. Also, in [33] , a design was presented that included a continuous-time linear equalizer and a two-tap half-rate/quarter-rate decision-feedback equalizer that utilized charge steering techniques to reduce power consumption. The prototype was implemented in 45 nm technology and consumed only 5.8 mW from a 1 V supply, while compensating for a 24 dB loss with BER < $10^{-12}$.

Equalization is used to combat Inter-Symbol Interference (ISI) caused by multipath in time-dispersive channels. ISI occurs when the modulation bandwidth is greater than the coherence bandwidth of the radio channel and modulation pulses are spread in time. A receiver (RX) with an equalizer can combat an average range of delay and channel amplitude that is expected. Equalizers must be adaptive because the channel is generally time-varying. Various adaptive equalizers can be used in radio channels to cancel interference while providing diversity. They track the time-varying characteristics of the mobile channel because the mobile fading channel is time-varying, and the equalizer must be adaptive in nature to combat this. In [34], different equalization techniques in digital communication were analyzed and a conclusion as to how much each of them is effective was derived.

With the communication industry rapidly moving towards a multi-gigabit era, inter symbol Interference (ISI) has become a significant issue that needs serious attention. As the world moves towards 5G and beyond, and with the introduction of electronic devices designed for multi-Gigabit data transfer, there is a greater need for exploration of Equalization Techniques compared to the past with low data rates. The main purpose of Equalization techniques is to ensure that the receiver

(RX) detects the same pattern as the transmitter (TX) and correct any errors caused by the transmission path. Paper [16], presented a comparative analysis of different equalization techniques using MATLAB simulation. Furthermore, Advance Design System (ADS) and Optic Wave simulations were conducted for high-speed serial link design and Optical link, and the receiver (RX) output was compared using Q-factor and Eye pattern, both with and without the implementation of Equalization.

In [35], a neural equalizer as a potential solution for better performance compared to traditional conversational equalizers was proposed. The neural equalizer was designed to minimize mean square error and distortion due to ISI. The results of the analysis indicated that the operational behaviour of the neural equalizer was superior to that of all existing conversational system of equalizers. The proposed equalizer was tested for every channel with its own bit-error rate and noisy data, and simulation results showed that the properly designed equalizer had a lower bit error rate (BER) and better overall performance.

In the field of wireline communication, a recent study [36], showcased a PAM4 receiver (RX) design. This design incorporated continuous time linear equalizers (CTLEs) and a 2-tap direct decision feedback equalizer (DFE). The receiver employed a CMOS track-and-regenerate slicer and was fabricated using 28-nm CMOS technology. Remarkably, the design achieved impressive performance results, with a bit-error-rate (BER) surpassing 10-12 and an energy efficiency of 1.1 pJ/b at a data rate of 60 Gb/s. These measurements were taken over a channel with an 8.2-dB loss at the Nyquist rate.

# Chapter 3

# Architecture of High Speed SerDes

## 3.1 Data Transmission

Data transmission refers to the transfer of digital data from one device to another through point-to-point data streams or channels. These channels can be wired or wireless. The transmission can occur over a wired or wireless network, using various communication technologies and protocols. Data transmission can include both analog and digital data.

Figure 3.1 gives an insight of the most common methods of data transmission include serial transmission and parallel transmission. In serial transmission, data is sent one bit at a time over a single communication channel. This method is slower than parallel transmission, which sends multiple bits simultaneously over multiple channels.

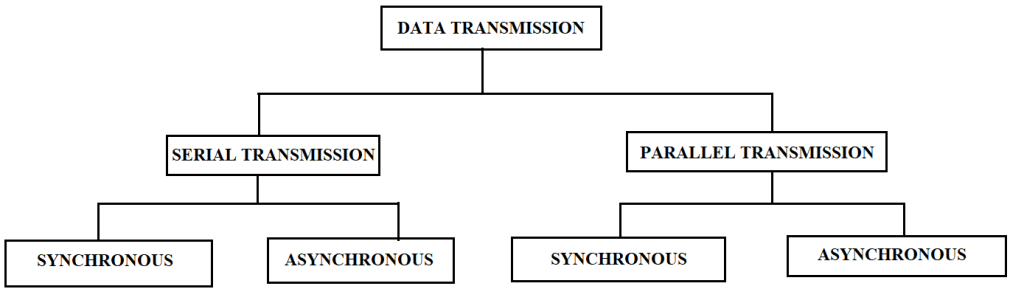


Fig. 3.1 Types of data transmission

Data transmission is an essential aspect of modern communication and plays a crucial role in enabling communication between different devices. It is used in various applications, including voice and video communication, internet browsing, and file sharing. However, it is important to ensure that the data transmitted is secure and free from unauthorized access.

The effectiveness of data transmission is heavily dependent on the amplitude and transmission speed of the carrier channel. The data transfer rate, which refers to the amount of data transferred within a given time period, determines whether a network can support data-intensive tasks. Network congestion, latency, server health, and insufficient infrastructure can cause data transmission rates to decline, which can negatively impact business performance. High-speed data transfer rates are essential for processing complex tasks like online streaming and large file transfers.

In conclusion, data transmission is the backbone of modern communication and enables the transfer of digital data between devices. To ensure efficient data transmission, it's important to have a reliable communication network and infrastructure. This will help guarantee high-speed data transfer rates, which are necessary for handling data-intensive applications.

## 3.2 Types of Data Transmission

### 3.2.1 Parallel Transmission

Parallel transmission is a data transmission method in which multiple bits of data are transmitted simultaneously over multiple data lines. In parallel transmission, each bit is transmitted through a separate data line, which allows for faster data transfer compared to serial transmission.

Parallel communication comprises multiple data lines that can carry multiple data bits simultaneously. The data from the transmitting port will be sent to the corresponding receiving port. Therefore, for n-bit parallel communication, 2n ports and n wires are needed as shown in Fig.3.2

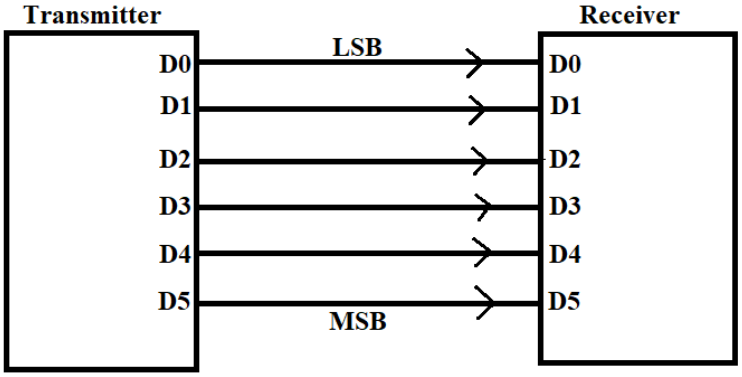


Fig. 3.2 Parallel transmission interface

Parallel transmission is commonly used in computer systems for data transfer between components such as memory, processors, and input/output devices. This is because computer systems require high-speed data transfer for quick processing and response times.

One of the advantages of parallel transmission is its ability to transmit multiple bits of data simultaneously, which results in faster data transfer rates. Parallel transmission is also less susceptible to errors than serial transmission, as errors can be easily detected and corrected.

However, one of the main limitations of parallel transmission is the requirement for multiple data lines, which can be expensive, takes more area and is complex to implement in some applications.

Additionally, parallel transmission is susceptible to skew, which occurs when the signals on different data lines arrive at different times, causing errors in data transmission.

There are two main types of parallel transmission: synchronous and asynchronous.

Synchronous parallel transmission involves sending data in parallel at fixed intervals, with a clock signal used to synchronize the transmission. This type of transmission is commonly used in computer memory systems and other high-speed applications, where the timing of data transfer is critical. Figure 3.3 gives an insight of the data flow in a synchronous transmission.

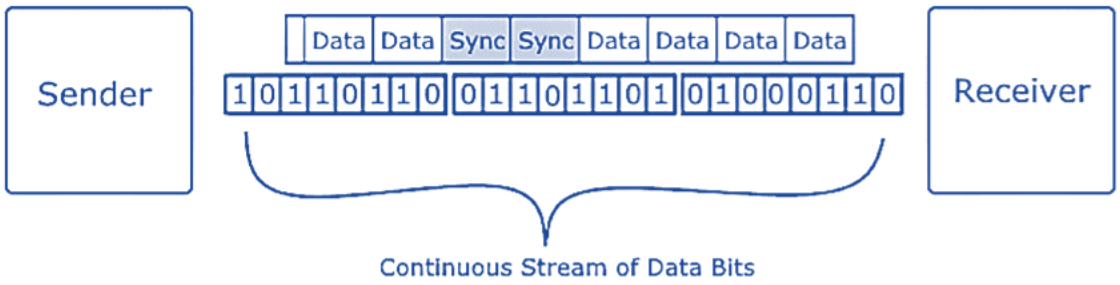


Fig. 3.3. Alignment of data bits in a synchronous data transmission [37].

Asynchronous parallel transmission, on the other hand, involves sending data in parallel without a fixed clock signal. Instead, each data bit is accompanied by a start and stop bit to indicate the beginning and end of the data transmission. This type of transmission is commonly used in low-speed applications, such as keyboard input, where timing is less critical. Figure 3.4 gives an insight of the data flow in an asynchronous transmission.

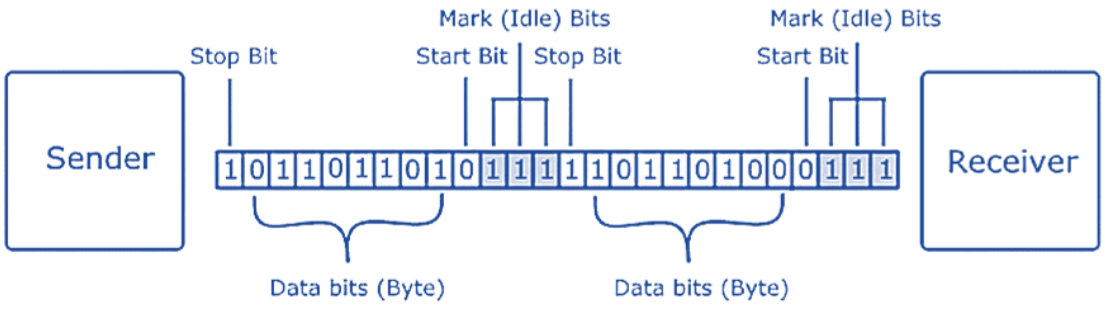


Fig. 3.4. Alignment of data bits in an asynchronous data transmission [37].

In conclusion, parallel transmission is a data transmission method that offers faster data transfer rates compared to serial transmission. It is commonly used in computer systems for high-speed

data transfer, but it can be limited by its requirement for multiple data lines and susceptibility to skew. Despite these limitations, parallel transmission remains an essential component of modern computing.

### 3.2.2 Serial Transmission

Serial transmission is a method of transmitting data where the bits of data are transmitted sequentially, one after the other, over a single communication line as shown in Fig.3.3. In serial transmission, each bit is transmitted separately, resulting in slower data transfer rates than parallel transmission. Serial communication most commonly use in chip-to-chip data transfer because it requires only one communication line and is less susceptible to noise interference.

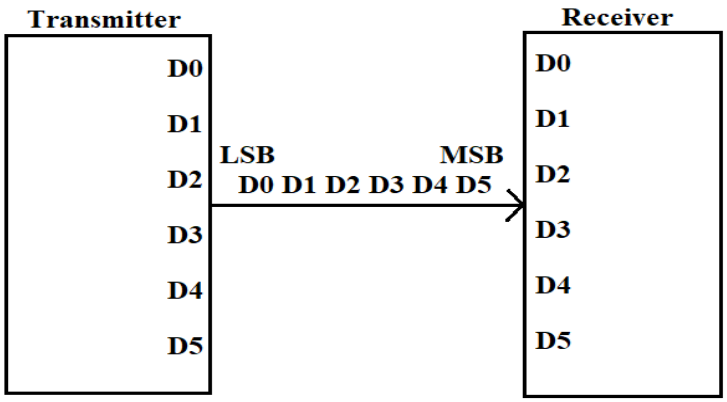


Fig. 3.3 Serial transmission interface

In serial transmission, data is sent in a specific format that includes start and stop bits to indicate the beginning and end of each data packet. This format allows for error detection and correction, making serial transmission a reliable method of data transfer.

Two main types of serial transmission exist, namely synchronous and asynchronous transmission.

Synchronous serial transmission employs a clock signal to synchronize the transmitter (TX) and receiver (RX), with data sent at fixed intervals. The transmitter (TX) generates the clock signal, which is transmitted alongside the data. Synchronous transmission is commonly used in applications where high data transfer rates are essential, such as in computer networking and telecommunications. Figure 3.3 shows how the data bits are aligned in a synchronous data transmission.

Asynchronous serial transmission, on the other hand, doesn't require a clock signal. Instead, each data byte is sent with start and stop bits that indicate the beginning and end of the transmission.

Asynchronous transmission is commonly used in low-speed applications such as keyboard input and serial printer communication. Figure 3.4 shows how the data bits are aligned in an asynchronous data transmission.

One of the main advantages of serial transmission is its simplicity and cost-effectiveness compared to parallel transmission. It is also ideal for long-distance communication because the data can be transmitted over long distances without significant signal degradation.

However, one of the limitations of serial transmission is its slower data transfer rates, which may not be suitable for applications that require high-speed data transfer, such as large file transfers or video streaming. However, with the advancements in data transfer protocols, improved circuitry and fast I/Os, serial communication has been upgraded in terms of speed and it is a preferred mode of data transmission in high-speed data transmission.

In conclusion, serial transmission is a reliable and cost-effective method of data transfer that is commonly used in communication systems. It is suitable for long-distance communication and offers error detection and correction. However, its slower data transfer rates may limit its use in applications that require high-speed data transfer.

## 3.3 Modes of Transmission

Data transmission is a crucial process involved in transmitting digital or analog data from one device to another. In general, two modes of data transmission are simplex and duplex.

Simplex transmission is a unidirectional mode of data transmission, where data only flows in one direction - from the sender to the receiver (RX). It is commonly used in scenarios where data is transmitted in one direction only, for instance, in broadcast systems or fire alarms. Figure 3.5 shows, the communication between sender and receiver (RX) in simplex transmission.

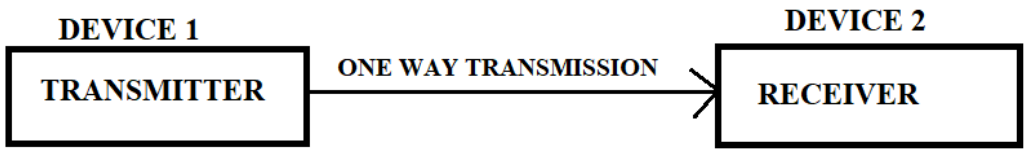


Fig 3.5. Simplex Transmission.

Duplex transmission, on the other hand, is a bidirectional mode of data transmission, where data flows in both directions simultaneously. It is commonly used in situations that require

simultaneous data transmission and reception, for example, in telephony, video conferencing, and computer networking.

Duplex transmission can further be categorized into two types:

Half-duplex transmission- It allows for the transmission and reception of data, but not simultaneously, Figure 3.6, shows the communication between sender and receiver (RX) in half-duplex transmission. The devices take turns to transmit and receive data, and this mode is commonly used in Ethernet networks and two-way radio communication.

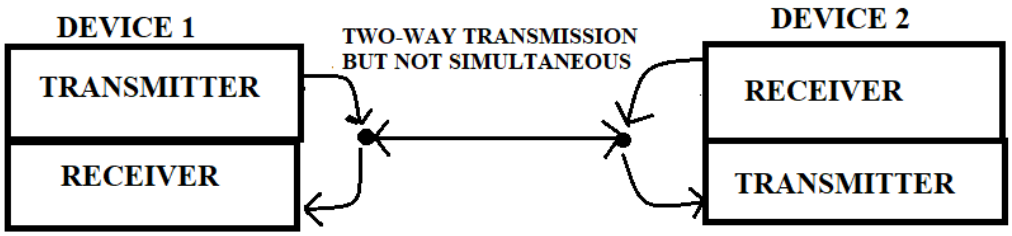


Fig. 3.6. Half-duplex transmission.

Full-duplex transmission- It enables simultaneous transmission and reception of data, which is required in scenarios that involve real-time, high-speed data transfer such as fiber optic communication, satellite communication, and internet data transfer. Figure 3.7 shows the communication between sender and receiver (RX) in full- duplex transmission

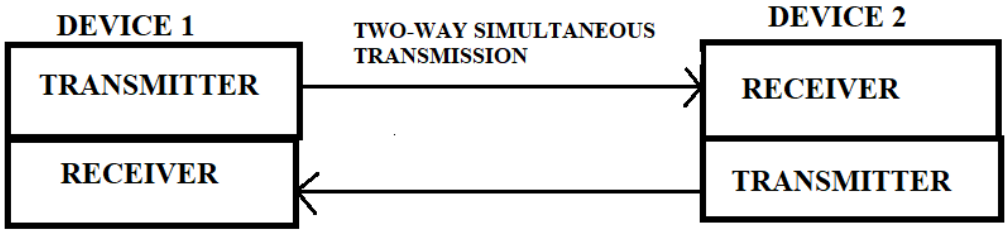


Fig. 3.7. Full-duplex transmission.

In conclusion, simplex and duplex are the two primary modes of data transmission, and duplex transmission can be divided into half-duplex and full-duplex. The choice of mode depends on the specific application requirements such as the rate of data transfer, direction of data flow, and the need for simultaneous data transmission and reception.

## 3.4 Significance of Serial Data Transmission

Serial data transmission is often considered a better option compared to parallel data transmission, due to several reasons:

Firstly, serial transmission requires fewer wires or channels than parallel transmission, thus making it more cost-effective and easier to implement.

Secondly, the single-stream nature of serial transmission makes it less vulnerable to signal interference and noise, as compared to parallel transmission. As a result, it is easier to detect and correct errors in data transmission. Moreover, a high-speed serial link will usually exhibit less radiated emissions a parallel transmission. This is because functioning gigabit links require excellent signal integrity.

Thirdly, serial transmission has the ability to cover longer distances between the transmitter (TX) and receiver (RX) as the signal can be amplified or regenerated at different points along the transmission path. In contrast, parallel transmission may suffer from signal degradation over longer distances, as each data line can be affected by interference and noise.

Fourthly, modern serial transmission technologies such as USB, Ethernet, and Thunderbolt, can achieve high data transfer rates that match those of parallel transmission, thus making it suitable for a wide range of applications.

Overall, while parallel transmission may have certain advantages in certain applications, serial transmission has become the preferred method for many data communication systems due to its simplicity, reliability, and flexibility.

## 3.5 Introduction to High-Speed SerDes

I/O design has incorporated serial-to-parallel and parallel-to-serial conversions as well as clock synchronization with incoming data since the early days. However, with the advancement of integrated circuit (IC) technology and the increase in maximum toggle rate (Fmax), the demand for I/O bandwidth has significantly grown. In fact, some advancements have enabled I/O frequency beyond Fmax, which has made SERDES an increasingly important technology.

The Serializer/Deserializer (SerDes) device is critical for high-speed applications because it can transfer data serially and convert parallel data to serial and vice versa. Figure 3.8 [38], shows a simplified model of the SerDes device [38].

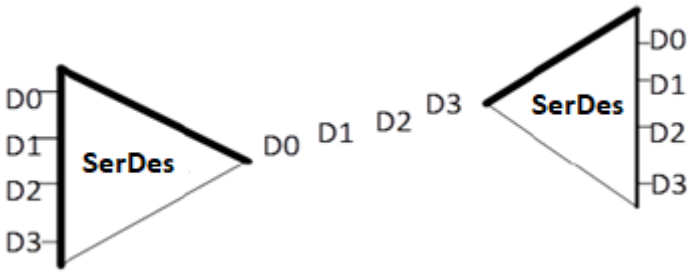


Fig. 3.8. Simplified model of SerDes link [38].

Figure 3.9, illustrates, a basic block diagram of a high-speed SerDes device. The process starts with n-bit parallel data, which is converted to serial data using a Serializer. An equalizer is utilized to ensure good signal integrity of the serialized data, which is then transmitted through a differential channel. On the receiver (RX) side, the serial data is received by a receiver (RX), and then fed into a Clock Data Recovery (CDR) circuit, which generates the clock. After passing through the equalization and recovery circuitries, the data is finally processed by a Deserializer, which converts the serial data back to parallel data.

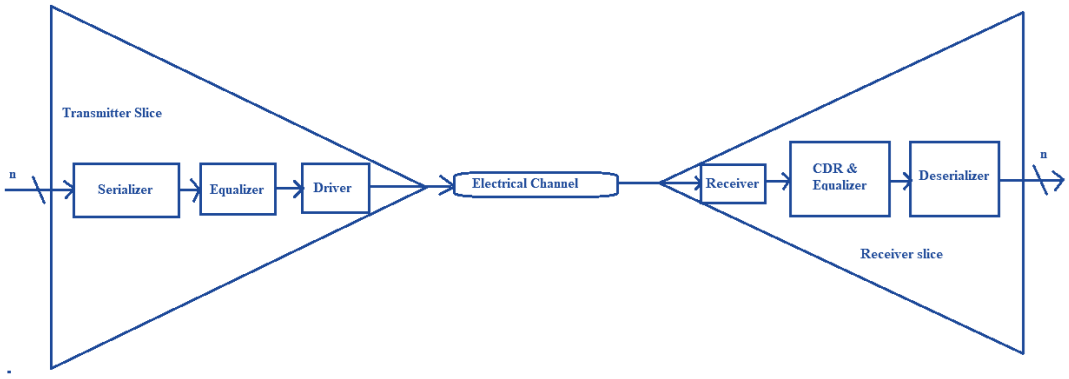


Fig. 3.9. Basic block diagram of a high-speed SerDes link

The generalized model of a High-Speed SerDes, depicted in Figure 3.9, is composed of a serializer and transmitter (TX) driven by a Phase-Locked Loop (PLL) clock synthesizer, a channel, a receiver (RX), and a Deserializer driven by a Clock-Data Recovery (CDR) unit. The serializer accepts the incoming parallel data-stream and converts it into a serial data-stream, which is then transmitted to the TX. The TX generates a pulse train depending on the data symbols to be transmitted across the channel and the pulse-width, which is determined by the transmit clock timing at the beginning, end, and edges. The receiver (RX) consists of a sampler and a decision circuit, which are responsible for sampling the received data-bit stream from the channel and recovering both the transmitted data and the clock. Once the receiver (RX) recovers the transmitted serial bit-stream,

it is sent to the Deserializer block, which converts the received serial data back to its original parallel form for future interfaces [39].

## 3.6 Transmitter (TX)

The primary function of the transmitter (TX) is to transmit a high-speed data stream to a receiver (RX) by providing a high-speed voltage swing at the transmitter (TX)'s pins. Figure 3.10 depicts a typical block diagram of the transmitter (TX), which encompasses four key operations: parallel to serial conversion, clock generation, feedforward equalization, and line driving. The transmitter (TX) receives an n-bit parallel data stream as input, which is then converted into a high-speed serial data stream by the serializer block. The PLL generates a multi-phase clock based on an external reference clock. The transmitter (TX) utilizes FeedForward Equalization (FFE) to mitigate the impact of Inter-Symbol Interference (ISI). Lastly, the driver is employed to match the output impedance of the transmitter (TX) with the impedance of the channel (transmission line) [38].

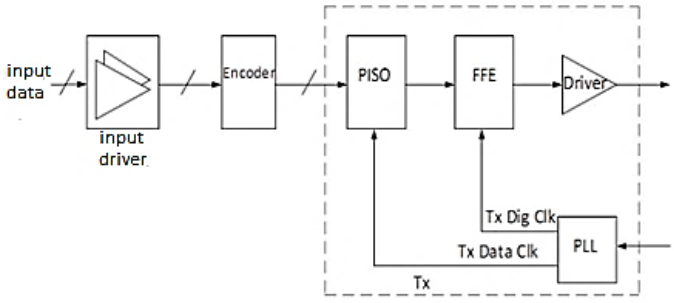


Fig. 3.10. Block Diagram of transmitter (TX) [38].

### 3.6.1 Phase-Locked Loop (PLL) Clock Generator

A Phase-Locked Loop (PLL) is a negative feedback system designed to generate an on-chip local clock at a desired frequency ($f_{OUT}$) by utilizing a reference input clock ($f_{REF}$). The PLL ensures that the output clock is phase-aligned with the input clock, and the output frequency ($f_{OUT}$) is a multiple (represented by $\alpha$) of the reference frequency ($f_{REF}$). PLLs are widely used in modern high-speed systems, both wired and wireless, as it is currently impractical to directly generate high-quality clock signals at microwave frequencies or high data rates. Piezo-electric crystals are commonly used as reference clocks in on-chip interface systems due to their high spectral purity, providing periodic and jitter-free clock signals up to around 200MHz. While crystals offer excellent spectral purity, their usage alone is insufficient to meet the demands of robust and high-speed signaling. Therefore, a PLL becomes essential. The primary goal of a PLL is to generate clock signals with

minimal timing noise, particularly low jitter (in the time domain) and phase noise (in the frequency domain). At a block level, a typical PLL clock generator circuit, as illustrated in Figure 3.11, consists of several components: a Phase-Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage-Controlled Oscillator (VCO), and Clock Divider (DIV) [39].

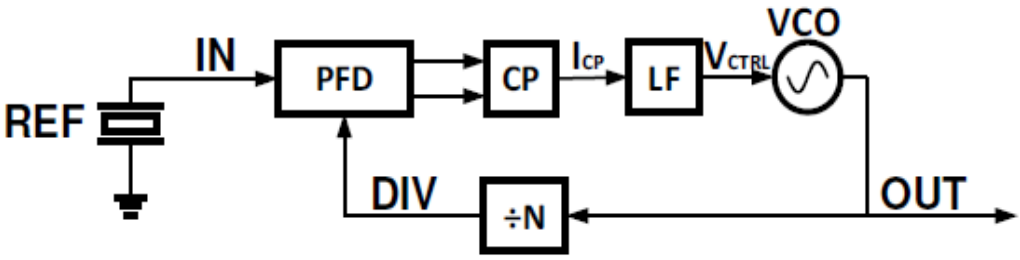


Fig. 3.11. Typical PLL Based Clock-Generator Block Diagram [39].

The PFD tracks the phase and frequency difference between the reference signal and the divider output signal. It produces pulse-width modulated (PWM) digital signals that are converted into an analog current signal by the CP. The LF then filters out high-frequency noise from the CP output current signal through low-pass filtering, generating a control voltage that drives the VCO. The VCO is a critical component in the PLL, responsible for generating the final output clock that drives the digital circuits of the system. Thus, achieving low phase noise in the VCO is of utmost importance since it dominates the noise within the PLL. Finally, the divider is employed in the feedback loop, returning the VCO output to the PFD. This ensures that the VCO output frequency matches the reference clock frequency, allowing the loop to dynamically drive any static phase errors between the reference clock and the divider clock to zero. Consequently, the loop is "locked," enabling a stable output clock at the desired operating frequency ($f_{OUT} = \alpha f_{REF}$), where $\alpha$ represents the multiplying factor [39].

### 3.6.2 Serializer

The Serializer converts parallel data into a serial bit-stream, as shown in Figure 3.12. A simplified circuit diagram of a 2:1 Serializer is presented here as an example [38].

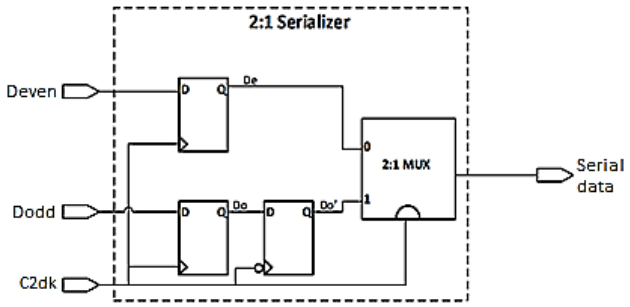


Fig. 3.12. 2 to 1 Serializer Block Diagram [38].

Assuming the parallel data bits $D_{even}$ and $D_{odd}$ are aligned in time within the serializer and synchronized with the half-rate $C_2$ clock signal, the first two D-latches capture the parallel $D_{even}$ and $D_{odd}$ signals. On the rising edge of the $C_2$ clock signal, the $D_e$ and $D_o$ outputs are generated. The $D_o$' signal is created by resampling the $D_o$ signal on the falling edge of the $C_2$ clock signal. The select input of the 2:1 MUX is controlled by the $C_2$ clock signal, resulting in the selection of the $D_e$ input signal when the clock is low and the selection of $D_o$' when the clock is high [38].

### 3.6.3 Transmitter (TX) Equalization

Transmitter (TX) equalization is a fundamental technique employed in high-speed communication systems to mitigate the adverse effects of channel impairments. When a signal traverses a transmission medium, such as a wired or wireless channel, it encounters various forms of distortions, including Inter-Symbol Interference (ISI) and attenuation. These distortions can degrade the quality and reliability of the received signal. Transmitter (TX) equalization aims to compensate for these impairments by applying specific pre-processing techniques to the transmitted signal. The goal is to enhance the signal quality at the receiver (RX) 's end, enabling more accurate and reliable data recovery [40].

One commonly used method in transmitter (TX) equalization is Feed-Forward Equalization (FFE). FFE involves incorporating a pre-emphasis filter at the transmitter (TX) side to boost the high-frequency components of the signal. This pre-emphasis filter selectively boosts certain frequency components, counteracting the effects of attenuation and ISI caused by the channel. The boosted high-frequency components help in reshaping the transmitted waveform, compensating for the distortions introduced by the channel.

Decision feedback equalization (DFE) is another technique employed in transmitter (TX) equalization. DFE utilizes feedback from the receiver (RX) to estimate and cancel the interference

caused by previously transmitted symbols. By continuously adapting to the received signal, DFE can dynamically adjust the transmitted signal to mitigate the impact of ISI. This adaptive nature allows DFE to effectively counteract the channel impairments and improve the overall signal quality.

Transmitter (TX) equalization plays a critical role in achieving reliable and high-speed communication. By compensating for the channel impairments, it enables the transmission of data at higher bit rates while maintaining signal integrity. Through techniques like FFE and DFE, transmitter (TX) equalization optimizes the performance of communication systems and enhances the overall quality of data transmission [40].

### 3.6.4 Driver

The transmitter (TX) is responsible for generating an accurate voltage swing on the channel in accordance with protocol specifications. To achieve this, either a current mode or voltage mode driver is utilized [38], as depicted in Figure 3.13. The selection of the driver depends on the desired voltage swing and impedance matching requirements.

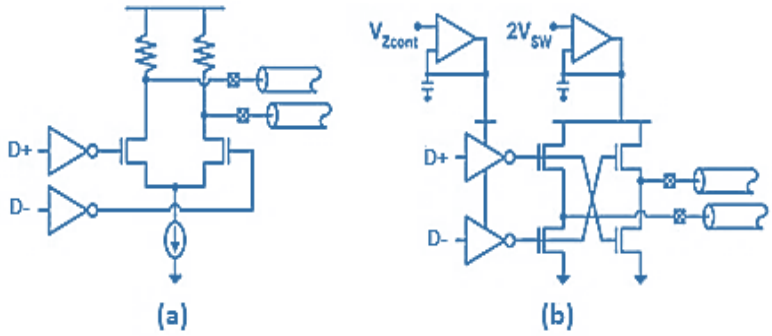


Fig. 3.13, (a) Current Mode Driver (b) Voltage Mode Driver [38].

In current mode drivers [38], currents are steered to generate a voltage swing of approximately 500 mV. Typically, a current close to 20mA is used for this purpose. To match the driver output impedance, a resistor is placed in parallel with the high-speed current switch. Current mode drivers are commonly employed when high voltage swing is required. They utilize Norton equivalent parallel termination, which facilitates easy control of the output impedance.

On the other hand, voltage mode drivers utilize Thevenin-equivalent series termination. With voltage mode drivers, the current required to generate the same voltage swing is lower compared to current mode drivers, resulting in lower power consumption. However, achieving impedance matching with voltage mode drivers can be more challenging.

The choice between current mode and voltage mode drivers depends on the specific requirements of the application, considering factors such as voltage swing, power consumption, and impedance matching. Each driver type has its advantages and trade-offs, and the selection should be based on the specific design considerations and performance goals.

## 3.7 The Channel

The channel serves as the electrical pathway connecting the TX and RX blocks in inter-IC communication systems. It typically consists of printed circuit-board (PCB) traces, vias, connectors, and other I/O interface components. In high-speed I/O interfaces, the channel often functions as a "backplane" that connects two PCBs together, resembling the interface depicted in Figure 3.10. As a link designer, the channel is considered a "known unknown" since its characteristics such as the channel impulse-response, can be determined through measurements using tools like a Vector-Network-Analyzer (VNA) or computational electromagnetic modeling software like Ansys HFSS (High-Frequency Structure Simulator). However, the exact way the channel degrades the transmitted signal stream remains unknown, posing a challenge for the designer. The challenge lies in devising a mechanism that counteracts this degradation, aiming to create a high-speed communication system with high signal fidelity, resilience to channel losses, low power consumption, and minimal footprint. Meeting these requirements becomes challenging due to the various types of microwave losses experienced by the channel at high speeds, such as impedance discontinuities between connectors, substrate loss, cross-talk effects, reflections, and ringing. Predicting and modeling these effects is inherently complex [39].

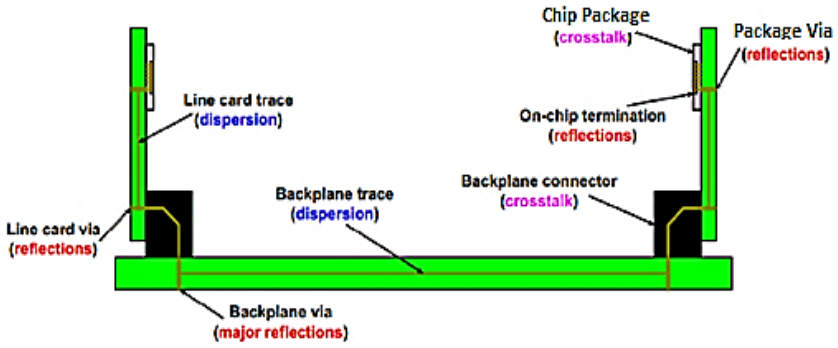


Fig. 3.10. Typical Backplane Channel Interface [39].

The I/O link interface for a 10Gb/s serial link across a backplane channel is illustrated in Figure 3.11. It is observed that transmitting a clean signal across a backplane channel at a speed of 10Gb/s results in significant signal loss. Consequently, the signal received at the receiver (RX) becomes

almost indistinguishable from noise, rendering it practically useless. To mitigate the deterioration of signal quality during transmission and reception, mixed-signal designers strive to develop high-frequency clocks with minimal timing skew at the transmitting end and ensure minimal sampling errors at the receiving end.

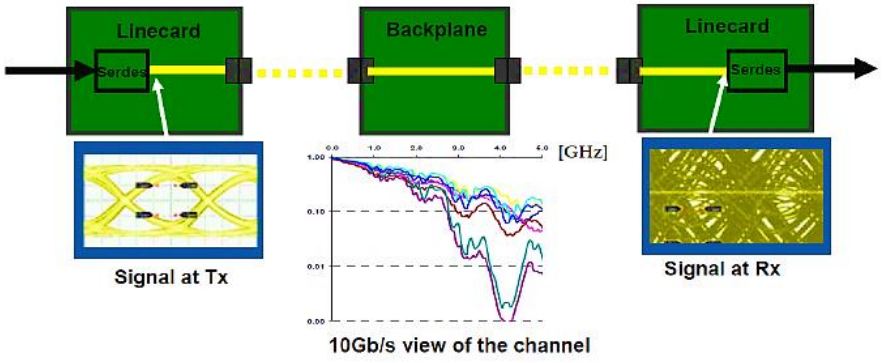


Fig. 3.11. 10Gb/s Backplane Serial Link Interface [41].

## 3.8 Receiver (RX)

The primary role of the receiver (RX) is to conduct equalization and successfully retrieve both data and clock signals. Figure 3.14 depicts a typical receiver (RX) block which comprises several key components, including a deserializer circuit, equalization block and a clock and data recovery (CDR) circuit [42].

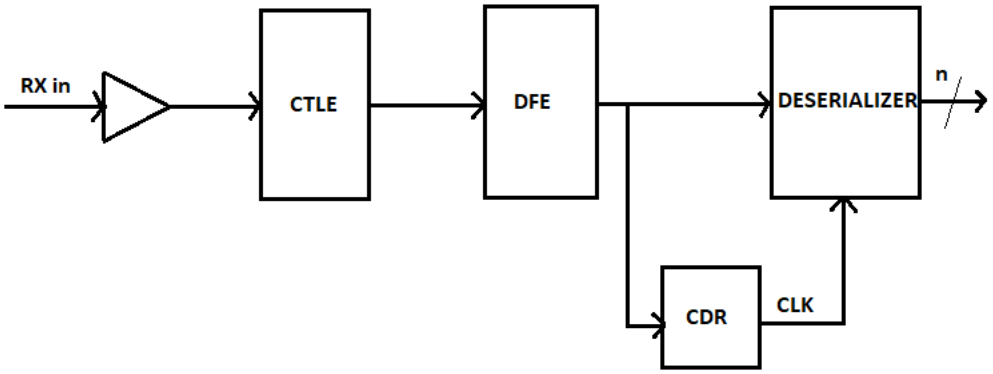


Fig. 3.14. Receiver (RX) Block Diagram [38].

### 3.8.1 Receiver (RX) Equalization

According to [43], receiver (RX) equalization is a crucial technique employed in high-speed communication systems to compensate for the distortions and impairments introduced by the channel. As a signal propagates through the transmission medium, it experiences various forms of

degradation, including Inter-Symbol Interference (ISI) and noise. These effects can significantly impact the accuracy and reliability of data reception. The primary goal of receiver (RX) equalization is to restore the original signal quality by employing specific signal processing techniques. By intelligently processing the received signal, equalization techniques aim to mitigate the impact of channel-induced distortions and enhance the overall performance of the communication system.

One widely used method in receiver (RX) equalization is linear equalization. Linear equalizers apply a digital filter to the received signal to compensate for the channel-induced distortions. The filter coefficients are typically adaptively adjusted based on the characteristics of the received signal and the channel. The objective is to reduce ISI and improve the overall signal quality, allowing for more accurate detection of the transmitted data. Another popular approach in receiver (RX) equalization is decision feedback equalization (DFE). DFE combines forward equalization with feedback equalization. It uses feedback from the detected symbols to estimate and cancel the interference caused by previously transmitted symbols. This iterative process helps to mitigate ISI and improve the overall performance of the receiver (RX).

Receiver (RX) equalization techniques play a critical role in achieving reliable and high-speed communication. By compensating for the channel impairments, equalization enhances the robustness and accuracy of data reception. It allows for the successful recovery of transmitted information, even in the presence of challenging channel conditions.

### 3.8.2 Clock and Data Recovery (CDR)

A Clock and Data Recovery (CDR) circuit performs the crucial task of extracting the clock information from the received signal in a communication system. In modern High-Speed Serial Links (HSSLs), it is necessary to have a clock recovery mechanism at the receiver (RX) because the transmitter (TX)'s clock information is typically embedded within the incoming data stream.

The CDR is essentially a modified Phase-Locked Loop (PLL) circuit where the phase detector samples the incoming data stream to extract both data and phase information from it. By detecting transitions in the received data stream, the phase detector drives a Voltage-Controlled Oscillator (VCO) to generate a periodic clock. This clock is then used to re-time the distorted received data through a decision circuit within the phase detector. The regenerated system clock has lower skew and jitter.

Designing a CDR is more intricate compared to a PLL because the CDR's loop bandwidth is often very small and determined by the system's jitter tolerance specifications. This leaves limited room for reducing VCO phase noise. A common implementation of a CDR (as shown in Figure 3.15) includes a regular PLL loop to track the exact frequency of the transmitter (TX)'s clock, a phase-tracking loop with a specialized phase detector to produce the retimed data, and a shared VCO that outputs a low-jitter, phase-noise replica of the transmitter (TX)'s clock [39].

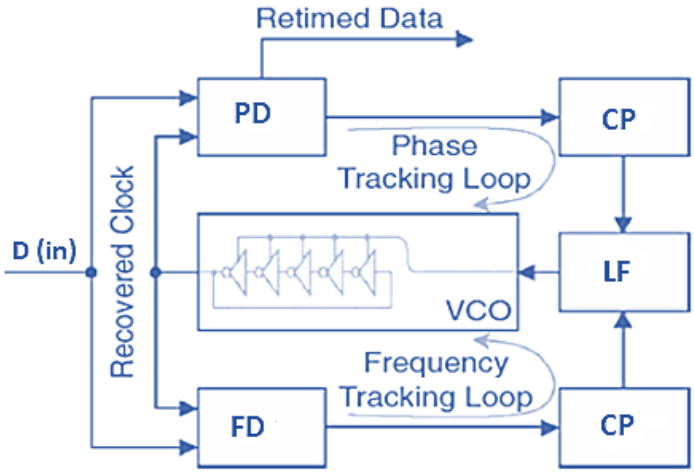


Fig. 3.15. A Typical CDR Unit Implementation [39].

### 3.8.3 Deserializer

The purpose of a deserializer circuit is to convert the incoming serial bit-stream data back into its original parallel bus form. As the name implies, the deserializer is a fully digital block located after the RX driver circuit. In essence, it functions as a demultiplexer circuit, driven by the clock that is recovered by the Clock and Data Recovery (CDR) circuit [39]. An illustrative representation of a 1:2 demultiplexer is provided below as an example, as depicted in Figure 3.16.

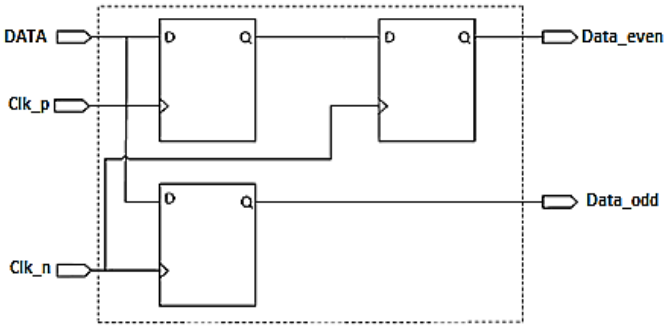


Fig. 3.16. 1 to 2 Deserializer Block Diagram [38].

The incoming serial data is directed to two D flip-flops, capturing the data at both the rising and falling edges of the clock. This process results in two separate data streams: even data and odd data. However, the even data arrives earlier than the odd data. To align the timing of the even data with the odd data, the even data stream is further delayed by the falling edge of the clock. As a result, two parallel data streams are obtained [38].

## 3.9 Summary

This section touched upon a detailed description of fundamental concepts and architecture of SerDes. The block diagram and the components of the block diagram are discussed to have an overall idea of High-Speed Serial Links. The further chapters cover topics like USB, which works on the principle of SerDes architecture. Rather, one can say that USB is a communication protocol based on SerDes architecture.

# Chapter 4

# Universal Serial Bus 3.2 (USB 3.2)

## 4.1 Introduction

The acronym USB stands for Universal Serial Bus, where "bus" refers to a circuit connection utilized for data and power transfer between components within an electronic system. In the context of USB, the term "serial" signifies the transmission of data one bit at a time over a single wire. USB serves as an engineering standard that defines the specifications for connectors and cables, enabling the interconnection of diverse devices in an electronic system [44].

Universal Serial Bus (USB) has emerged as the dominant interface for computer peripherals, providing a standardized means of communication between devices and personal computers. The development of USB begins in 1994 and was a collaborative effort involving seven prominent companies, including Compaq, DEC, IBM, Intel, Microsoft, Nortel, and NEC. These companies recognized the need to replace existing parallel ports and external power chargers with a universal and simplified communication standard that could facilitate efficient data exchange and serve as a power supply. In the present day, USB has become the universal and essential interface found on most motherboards, single board computers, and embedded microcontroller boards. It has also become a standard feature on a wide range of digital peripherals, spanning from traditional computer accessories such as keyboards, mice, and joysticks, to advanced smart devices including cameras, flash drives, smartphones, and tablets. The ubiquitous presence of USB ports highlights its widespread adoption and versatility in the digital landscape [45].

## 4.2 Data Transfer in USB

When a peripheral device is connected through a USB interface, the host computer employs an automatic detection mechanism to identify the type of device and load the necessary driver for its operation. The data exchange between the host computer and the device occurs in the form of small packets. Each packet consists of a specific number of bytes, which is a unit of digital information. Alongside the data, additional information is transmitted within each packet, including the data's source, destination, length, and any detected errors.

Four types of data transfer are commonly used in USB [46]:

1. **Interrupt Transfer:** This type of transfer is employed by devices like keyboards and mice to transmit smaller amounts of data. It is typically used for infrequent but important requests. The

peripheral devices generate the requests, but they must wait for the host to inquire about the specific data needed. If the initial transfer fails, these requests are guaranteed to be retried. Interrupt transfers also provide updates on the device's status.

2. **Bulk Transfer:** Printers and digital scanners utilize bulk transfer for transferring large amounts of data. This type of transfer has low priority and is not time-critical. If the host computer has multiple USB devices connected, the transfer speed may be affected.
3. **Isochronous Transfer**: Real-time data such as audio and video employ isochronous transfer. While errors can occur during the transfer, the packets are not resent, and the transfer continues uninterrupted. Isochronous transfers are typically used in situations where data accuracy is not critical, such as audio where missing elements are preferred over glitching audio.
4. **Control Transfer:** Control transfer is used to configure and control USB devices. The host initiates a request to the device, followed by the data transfer. Control transfers are also used to check the status of a device. Only one control request is processed at a time.

## 4.3 Advantages of USB

USB has emerged as the preferred interface for a wide range of digital equipment, including embedded microcontroller boards, motherboards, and various digital peripherals such as keyboards, mice, joysticks, as well as smart devices like mobile phones, tablets, cameras, and flash drives. This preference can be attributed to the numerous advantages that USB offers over alternative interfaces [45]:

1. **Versatility:** USB provides a versatile solution by offering a single interface that can support multiple devices. This eliminates the need for different connector types and hardware requirements for each peripheral, simplifying the overall system design.
2. **Plug-and-Play:** USB incorporates an auto-configuration feature, making it effortless to connect devices. Once a USB peripheral is plugged into a host device, the necessary device driver is automatically installed, enabling seamless and immediate device recognition.
3. **Expandability:** USB offers easy expandability. In situations where the built-in USB ports on a device are insufficient, USB hubs can be utilized to add additional ports, allowing for the connection of more peripherals.
4. **Compact Size:** USB connectors are compact in size compared to older interfaces like RS232 [47], or parallel ports. This compactness enhances portability and facilitates the integration of USB into smaller devices with limited space.

5. **Power Delivery:** USB provides power supply capabilities, allowing devices to be powered directly through the USB interface. Host devices can deliver a specified amount of direct current (DC) power to the connected peripherals, eliminating the need for separate external power sources.

Overall, the advantages of USB make it a highly desirable interface for a wide range of digital devices, enabling seamless connectivity, ease of use, and efficient power management.

## 4.4 USB Standards

Prior to USB, data transfer in computers involved the use of serial and parallel ports, along with proprietary plugs, connectors, and cables. This fragmented approach resulted in slow data transfer rates, ranging from 100 kB/s for parallel ports to 450 kB/s for serial ports. Connecting devices often required the host computer to be disconnected or restarted, and dedicated drivers and cards were often necessary. The USB standard was initially developed by the USB Implementers Forum (USB-IF) in 1994. Although several pre-release versions of the standard, such as USB 0.8, USB 0.9, and USB 0.99, were announced during that year, they were not commercially available at the time. After that, several USB standards and their updated versions were introduced with successive ones being better than its predecessor. The journey of USB standards mentioned in [44] as follows:

1. **USB 1.0**- In 1996, USB 1.0 was introduced as the initial significant release in the USB series. This version featured data transfer rates of 1.5 megabits per second (Mb/s) for low-speed devices and 12 Mb/s for full-speed devices. One of its notable advantages was its self-configuring capability, which eliminated the need for users to manually adjust device settings to accommodate peripherals. Additionally, USB 1.0 supported hot-swapping, allowing devices to be connected or disconnected without requiring the host computer to be rebooted. Despite being the first commercially available USB version, it initially faced limited market acceptance, and only a few devices were accessible to consumers.
2. **USB 1.1-** In 1998, a revised version of the initial USB standard was released, known as USB 1.1. This updated version maintained the same data transfer rates as USB 1.0 but introduced the capability to operate at slower speeds for devices with lower bandwidth requirements. It was marketed as "Full Speed." Apple's iMac G3 was one of the early adopters of the USB 1.1 standard, discontinuing the use of serial and parallel ports in favor of USB connections. This significant move by Apple played a crucial role in promoting the wider adoption of USB in the industry and driving consumer acceptance of USB products. USB 1.0 and 1.1 utilized standard

Type A (rectangular) or Type B (square with beveled top corners) connectors. Type A and Type B connectors are shown in figure 4.1.

3. **USB 2.0-** With the growing popularity of personal computers (PCs) and their accompanying peripherals, the demand for faster data transfer speeds became evident. To address this need, USB 2.0 was introduced in April 2000, boasting a data transfer rate of 480 Mb/s. However, due to bus limitations, the effective speed was reduced to 280 Mb/s. It was marketed as "High Speed" and supported data transfer rates of 12 and 1.5 Mb/s for devices with lower bandwidth requirements. USB 2.0 also brought plug-and-play functionality for multimedia and storage devices, along with support for power sources up to 5 V and 500 mA using USB connectors.

One significant feature introduced with USB 2.0 was USB On-the-Go, allowing two devices to communicate without the need for a separate USB host. USB 2.0 maintained compatibility with USB Type A, B, and C connectors, as well as USB Mini and Micro A & B connectors. However, the release of Micro A & B connectors didn't occur until 2007. Figure 4.1 shows USB Type A, B, C, Mini and Micro A & B connectors. In the year 2000, the first commercially available USB flash drives hit the market, offering storage capacities of up to 8 megabytes. This further contributed to the widespread adoption of the USB standard. Today, USB flash drives are available with storage capacities reaching the terabyte range.

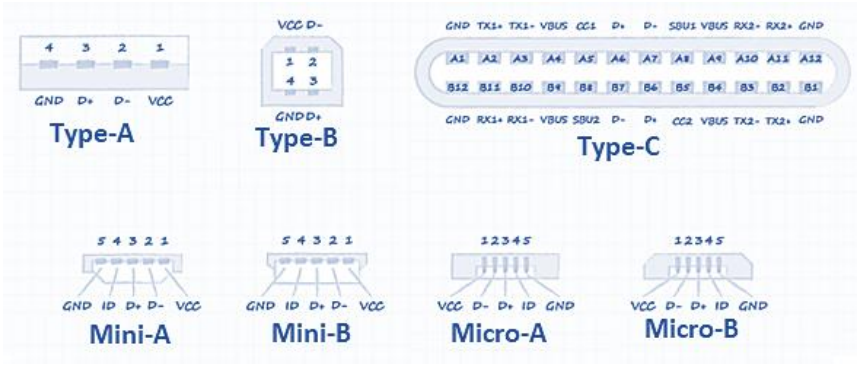


Fig. 4.1. USB Type A, B, C, Mini and Micro A & B connectors [44].

4. **USB 3.0 (now USB 3.2 Gen 1)-** The USB 3.0 standard was introduced in November 2008 to address the growing need for higher storage capacity and faster data transfer rates. With a maximum data transfer rate of 5 gigabits per second (Gb/s), although typically operating at around 3 Gb/s, USB 3.0 was branded as SuperSpeed USB. It featured eight connection lines, doubling the four lines of USB 2.0, enabling bi-directional data transfer. USB 3.0 maintained backward compatibility with USB 2.0 devices. In later updates, USB 3.0 was renamed using the USB 3.2 naming conventions and is now referred to as USB 3.2 Gen 1.

Moreover, the USB 3.0 standard increased the power transfer capability to 5 volts and 900 milliamperes (mA). It supported physical connectors such as USB 3.0 Type A and Type B, as well as the USB Type-C connector. To visually distinguish USB 3.0 connectors, they were typically colored blue.

5. **USB 3.1 (or USB 3.2 Gen 2*1)-** The USB 3.1 standard, released in July 2013, served as an interim update to USB 3.0, primarily focusing on increased data transfer speeds. The USB 3.1 version, also known as USB 3.1 Gen 2, offered data transfer rates of up to 10 gigabits per second (Gb/s). Like USB 3.0, USB 3.1 underwent a name update and is now referred to as USB 3.2 Gen 2, earning the designation of SuperSpeed+. In addition to the improved transfer speeds, USB 3.1 maintained compatibility with the existing USB 3.0 connectors, including USB Type A, Type B, Mini, and Micro connectors.

   Another significant development in USB technology occurred in 2014 with the introduction of USB Type-C connectors. Initially proposed in 2012, the USB Type-C connector revolutionized connectivity by offering a single, small, reversible connector capable of transmitting data, display, and power signals. With an oval-shaped design, the USB Type-C connector is approximately one-third the size of the original USB Type A connector and slightly thicker than the USB Mini and Micro versions. It incorporated additional wires and pins to enhance its data transfer capabilities.

6. **USB 3.2-** USB 3.2, introduced in September 2017, brought significant advancements and replaced the previous USB 3.0 and USB 3.1 standards. Designed to address the growing demand for faster data transfer speeds, USB 3.2 represented an interim step in USB technology evolution. One of the key enhancements of USB 3.2 was the doubling of data transfer speeds to 20 gigabits per second (Gb/s) with the USB 3.2 Gen 2x2 specification. This speed boost was achieved by expanding the data transfer channels from a single lane to two, effectively doubling the throughput. The introduction of USB Type-C connectors played a crucial role in enabling this improvement.

Table 4.1. USB 3.2 naming conventions.

| Name | Maximum Speed | Alternate Name | Previous name |
|---|---|---|---|
| USB 3.2 Gen 2x2 | 20Gb/s | SuperSpeed USB 20Gb/s | USB 3.2 |
| USB 3.2 Gen 2 | 10Gb/s | SuperSpeed USB 10 Gb/s | USB 3.1 Gen 2 |
| USB 3.1 Gen 1 | 5Gb/s | SuperSpeed USB 5Gb/s | USB 3.1 Gen 1 or USB 3.0 |

To fully leverage the 20 Gb/s data transfer speeds, USB Type-C cables are required. These cables can transmit 10 Gb/s in each direction over two wire pairs, maximizing the available bandwidth. USB 3.2 also maintained backward compatibility with previous USB generations and supported a variety of connectors, including USB Type A, Type B, Mini, Micro, and the versatile USB Type-C.

7. **USB 4.0-** USB 4.0, launched in August 2019, incorporates the Thunderbolt 3 protocol [48], enabling high-speed data transfer rates of up to 40 Gb/s. It also integrates the Power Delivery 3.1 standard, allowing for power transfer of up to 240 Watts. Thunderbolt 3, initially developed by Intel in 2015, was designed to facilitate fast data and video transmission.

   One notable advantage of USB 4.0 is its compatibility with existing USB Type-C connectors, eliminating the need for new connector designs. By efficiently sharing lanes, data and video signals can fully utilize the device's maximum bandwidth, resulting in optimized data transfer speeds. USB 4.0 remains backward compatible with USB 2.0 and 3.2 versions using adapters, although transfer speeds may be impacted.

   Intelligent Power Delivery is another key feature of USB 4.0, enabling a USB 4.0 cable to supply power according to the specific requirements of the connected device, supporting up to 240 Watts and 5 Amps. Moreover, power delivery is bi-directional, allowing power to flow to or from the connected device as needed. USB 4.0 offers significant advancements in terms of data transfer speed, power delivery, and versatility while maintaining compatibility with existing USB technologies.

## 4.5 Architectural Overview of USB 3.2

This section provides an overview of the architecture and fundamental principles of Universal Serial Bus 3.2. It follows the same fundamental concept as previous versions, serving as a cable bus that facilitates data transfer between a host computer and multiple peripherals that can be accessed simultaneously. Bandwidth allocation among connected peripherals is managed by the host through a scheduled protocol. USB 3.2 allows peripherals to be attached, configured, used, and detached while the host and other peripherals remain operational. It also employs a dual-bus architecture that ensures backward compatibility with USB 2.0. One of the buses adheres to the USB 2.0 standard, while the other is an Enhanced SuperSpeed bus as shown in Figure 4.3. Notably, USB 3.2 introduces dual-lane support as an additional feature. It is important to note that USB 3.2 maintains compatibility with previous USB versions while incorporating dual-lane support to enhance its capabilities [25].

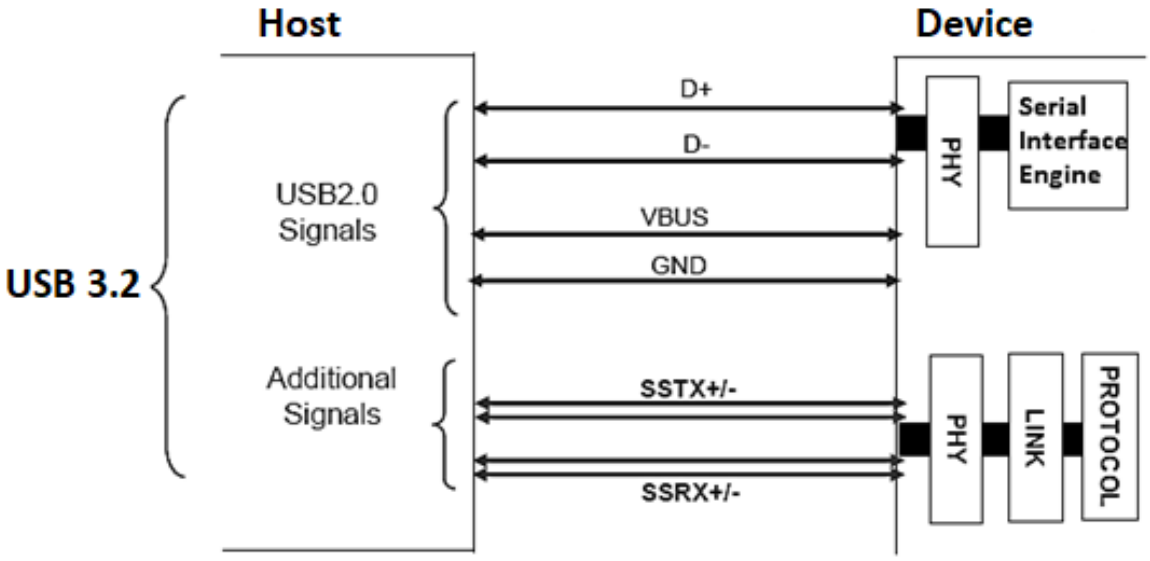


Fig. 4.3. USB3.2 Bus Communication Architecture [21].

## 4.6 Architectural Differences between USB 3.2 and USB 2.0

The author in [25] maps the key architectural differences between Enhanced Superspeed Bus and USB 2.0 as follows:

| **Characteristics** | **Enhanced SuperSpeed USB** | **USB 2.0** |
|---|---|---|
| Data Rate | Gen 1 has a speed of 5.0 Gb/s and Gen 2 has a speed of 10 Gb/s. | low-speed has a speed of 1.5 Mb/s, full-speed has a speed of 12 Mb/s, and high-speed operates at 480 Mb/s. |
| Data Interface | Dual-simplex, four-wire differential signaling for each lane (separate from USB 2.0 signaling, a total of eight wires for a two-lane configuration). Simultaneous bi-directional data flows | Half-duplex two-wire differential signaling. Unidirectional data flow with negotiated directional bus transitions |
| Cable signal count | Legacy cables supporting one lane with four for Enhanced SuperSpeed data path, two for USB 2.0 data path<br>USB Type-C cables supporting two lanes with eight for Enhanced SuperSpeed data path, two for USB 2.0 data path | Two: Two for low-speed/full-speed/high-speed (USB 2.0) data path |
| Bus transaction protocol | Host directed; asynchronous traffic flow Packet traffic is explicitly routed | Host directed; polled traffic flow Packet traffic is broadcast to all devices. |

| | | |
|---|---|---|
| Bus power | For one lane operation: Support for low (150 mA)/high (900 mA) bus-powered devices with lower power limits for un-configured and suspended devices. For two lane operation: Support for low (250 mA)/high (1,500 mA) bus-powered devices with lower power limits for un-configured and suspended devices. | Support for low (100 mA)/high (500 mA) bus-powered devices with lower power limits for un-configured and suspended devices. |
| Power management | Multi-level link power management supporting idle, sleep, and suspend states. Link-, Device-, and Function-level power management. | Port-level suspend with two levels of entry/exit latency Device-level power management. |
| Port State | Port hardware detects connect events and brings the port into operational state ready for Enhanced SuperSpeed data communication. | Port hardware detects connect events. System software uses port commands to transition the port into an enabled state (i.e., can do USB data communication flows). |
| Data transfer types | USB 2.0 types with Enhanced SuperSpeed constraints. Bulk has streams capability | Four data transfer types: control, bulk, Interrupt, and Isochronous |

## 4.7 USB 3.2 System Description

### 4.7.1 Introduction

According to [25], USB 3.2 incorporates both a physical SuperSpeed bus and a physical USB 2.0 bus, operating in parallel (Figure 4.4). The architectural components of USB 3.2 closely resemble those of USB 2.0, including:

- USB 3.2 interconnect
- USB 3.2 devices
- USB 3.2 host

The USB 3.2 interconnect is the method through which USB 3.2 and USB 2.0 devices establish connections and communicate with the USB 3.2 host. While inheriting fundamental architectural elements from USB 2.0, the USB 3.2 interconnect incorporates several enhancements to support its dual bus architecture. The underlying structural topology remains consistent with USB 2.0, featuring a hierarchical star configuration where a single host resides at tier 1, and hubs at lower tiers enable device connectivity across the bus.

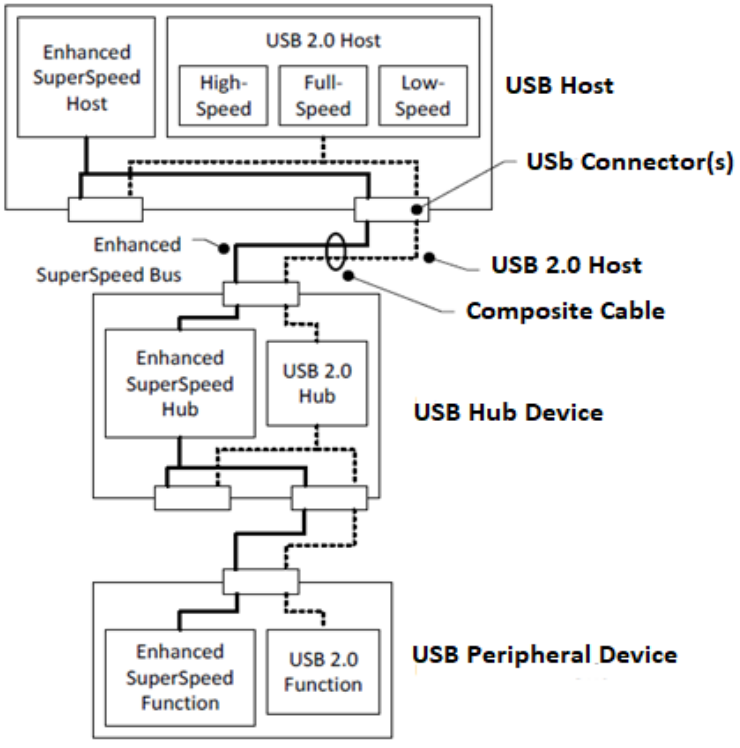


Fig. 4.4. USB 3.2 Dual Bus System Architecture [25].

The USB 3.2 connection model enables compatibility with both USB 3.2 and USB 2.0 devices, allowing them to be connected to either a USB Type-C connector or a USB 3.1 legacy connector. Similarly, USB 3.2 devices can be connected to a USB 2.0 legacy connector. This backward and forward compatibility is achieved through a composite cable and connector assemblies that serve as the mechanical infrastructure for the dual-bus architecture. To maintain backward compatibility, USB 3.2 peripheral devices include both Enhanced SuperSpeed and USB 2.0 interfaces. USB 3.2 hosts also have both Enhanced SuperSpeed and USB 2.0 interfaces, which function as parallel buses that can be active simultaneously. The USB 3.2 connection model facilitates the identification and configuration of USB devices at the highest signaling speed supported by the peripheral device, the maximum signaling rate supported by the hubs between the host and the peripheral device, as well as the current capability and configuration of the host. USB 3.2 hubs, specifically designed for this purpose, provide additional connection points to the bus beyond those offered by the host.

### 4.7.2 Mechanical

This section provides an overview of the USB connectors and cables designed to support various levels of USB 3.2 functionality. Every USB device requires an upstream connection, while hosts and hubs have one or more downstream connections. In the case of USB legacy connectors, the upstream and downstream connectors are not mechanically interchangeable, preventing unauthorized loopback connections at hubs. With USB Type-C connectors, the upstream and downstream behaviours are determined using the configuration features of the USB Type-C functional architecture. USB 3.1 receptacles for legacy connectors (both upstream and downstream) are backward compatible with USB 2.0 connector plugs. However, USB 3.1 cables and plugs are not intended to be compatible with USB 2.0 upstream receptacles. To ensure backward compatibility with USB Type-C, specific cables and adapter assemblies are defined for legacy adaptation [25]. Table 4.2 provides information on the standard USB cables and adapter assemblies that are applicable to USB 3.2. Among these, the USB 3.1 Type-C to USB 3.1 Type-C cable assembly is the only one capable of offering dual-lane support.

Table 4.2. Information on the Standard USB Cables and Adapter Assemblies that are Applicable to USB 3.2 [25].

| **Standard USB Cables Applicability to USB 3.2** | | |
|---|---|---|
| **Plug #1** | **Plug #2** | **Applicability** |
| USB 3.1 Standard-A | USB 3.1 Standard-B | Enhanced SuperSpeed Gen 1*1<br>Enhanced SuperSpeed Gen 2*1 |
| USB 3.1 Standard-A | USB 3.1 Micro-B | |
| USB 3.1 Standard-A | USB 3.1 Standard-A | |
| USB 3.1 Standard-A | USB 3.1 Type-C | |
| USB 3.1 Micro-A | USB 3.1 Standard-B | |
| USB 3.1 Micro-A | USB 3.1 Micro-B | |
| USB 3.1 Type-C | USB 3.1 Standard-B | |
| USB 3.1 Type-C | USB 3.1 Micro-B | |
| USB 3.2 Type-C | USB 3.2 Type-C | Enhanced SuperSpeed Gen 1*1<br>Enhanced SuperSpeed Gen 1*2<br>Enhanced SuperSpeed Gen 2*1<br>Enhanced SuperSpeed Gen 2*2 |
| | | |
| | | |
| | | |
| | | |
| **Standard USB Adapter Assemblies Applicability to USB 3.2** | | |
| **Plug** | **Receptacle** | **Applicability** |
| USB Type-C | USB 3.1 Standard-A | Enhanced SuperSpeed Gen 1*1<br>Enhanced SuperSpeed Gen 2*1 |

### 4.7.3 Power Standards and Management

USB has transformed from being a mere data interface to becoming a primary power source alongside data transmission. Nowadays, USB ports found in laptops, workstations, docking stations, displays, vehicles, airplanes, and even wall sockets are commonly used for charging and powering various devices. It has become a universal power socket for small gadgets like cell phones, tablets, portable speakers, and other handheld devices. Users rely on USB not just for data transfer but also for conveniently providing power to their devices, often without the need for driver installation, to perform traditional USB functions.

The USB Power Delivery (USB PD) Specification plays a crucial role in maximizing the capabilities of USB by allowing more flexible power delivery in conjunction with data transfer over a single cable. Its objective is to operate within the existing USB ecosystem and enhance it

further. In 2021, the USB PD Revision 3.1 specification was announced as a significant update to enable power delivery of up to 240W through fully featured USB Type-C cables and connectors. Before this update, USB PD was limited to 100W using a solution based on 20V and USB Type-C cables rated at 5A. The USB Type-C specification has also been revised to Release 2.1, which outlines the requirements for 240W cables. With these updated USB PD protocols and power supply definitions, USB power delivery can now be applied to a wide range of applications where 100W was previously insufficient [49]. Table 4.3 gives specifications of USB Power Standards [50].

Table 4.3. USB Power Standards [50].

| **Standard** | **Port Type** | **Max Watts** | **Max Amps** | **Volts** |
|---|---|---|---|---|
| USB 3.2/3.1/3.0 | USB-A, USB-B | 4.5W | 900mA | 5V |
| USB Power Delivery (PD) | USB-C only | 240W | 5A | 5V, 9V, 15V, 20V, 28V, 36V, 48V |
| USB Battery Charging (BC) | USB-A, USB- C | 7.5W | 1.5A | 5V |
| USB-C (non PD) | USB-C | 15W | 3A | 5V |
| USB 2.0 | USB-A, USB-B, micro USB | 2.5W | 500mA | 5V |

The SuperSpeed architecture of USB 3.2 has been designed with a focus on maximizing power efficiency. Several key enhancements have been implemented to achieve this objective, including [21]:

- **Elimination of continuous device polling:** This means that devices connected via USB no longer need to be constantly checked for activity, reducing unnecessary power consumption.
- **Elimination of broadcast packet transmission through hubs:** Broadcast packets, which were previously sent to all devices connected to a hub, are no longer required. This helps minimize power usage by reducing unnecessary data transmission.
- **Introduction of link power management states:** SuperSpeed USB incorporates power management states that enable devices to enter aggressive power-saving modes when idle. This helps conserve power when there is no active data transfer taking place.
- **Host and device-initiated transition to low power states:** Both the host (such as a computer) and USB devices can initiate the transition to low power states when appropriate. This allows for efficient power management based on the device's usage patterns.
- **Device and individual function level suspend capabilities:** USB devices now can suspend power to specific parts of their circuitry when not in use. This allows for selective power removal from portions that are not actively being utilized, further optimizing power efficiency.

These power efficiency enhancements in the SuperSpeed architecture contribute to reducing power consumption and promoting energy-efficient operation for USB devices.

### 4.7.4 Enhanced SuperSpeed Bus Architecture

The Enhanced SuperSpeed bus comprises various components that form a layered communications architecture. These elements include [25]:

- **Enhanced SuperSpeed Interconnect:** The Enhanced SuperSpeed interconnect is responsible for the connection and communication between devices and the host over the Enhanced SuperSpeed bus. It encompasses the topology of the connected devices, the communication layers, and the interactions between them. Its purpose is to facilitate the exchange of information between the host and devices. The reference diagram in Figure 4.7 provides an overview of the Enhanced SuperSpeed interconnect, showcasing the communication layers and the topology of the host, hubs, and devices. The diagram represents the Enhanced SuperSpeed interconnect as rows indicating the different layers: device or host, protocol, link, and physical. On the left-hand side of the diagram, the three columns depict the topological relationships between the devices connected to the Enhanced SuperSpeed bus. These columns represent the host, hub, and device connections within the topology. The right-most column in the diagram illustrates the impact of power management mechanisms on the communication

layers. It highlights how power management influences the functioning of the Enhanced SuperSpeed interconnect.

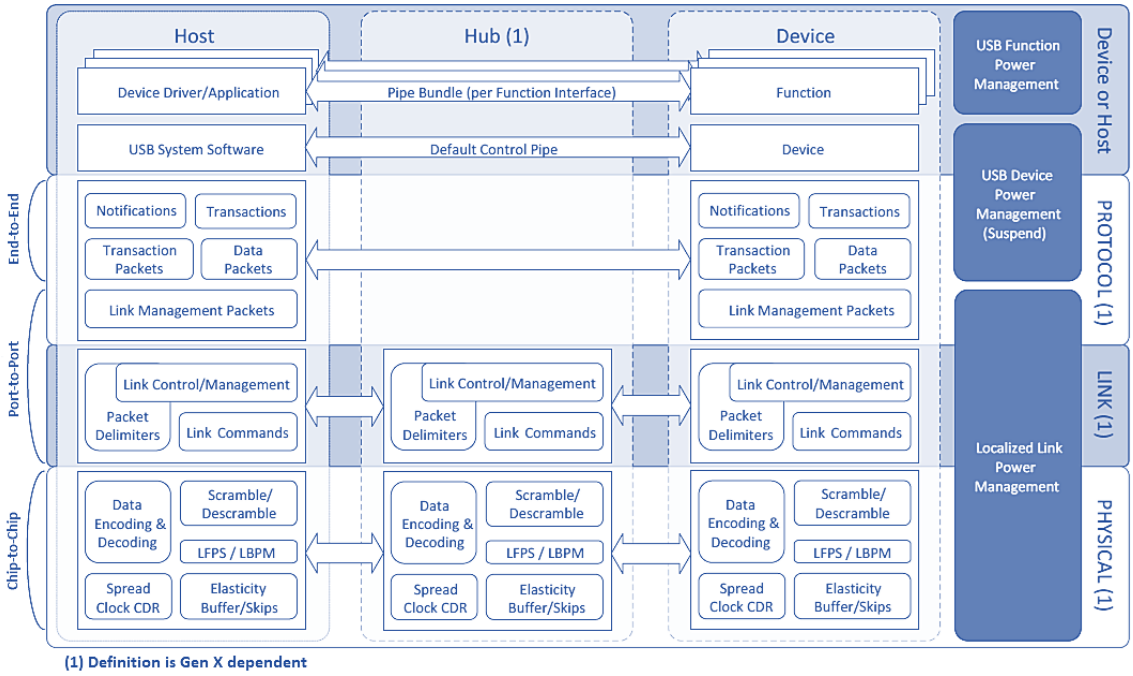


Fig. 4.7. Reference Diagram of the Enhanced SuperSpeed interconnect [25].

- **Devices:** Enhanced SuperSpeed devices function as sources or sinks of information exchanges. They implement the necessary communications layers specific to Enhanced SuperSpeed to enable information exchange between a driver on the host and one or more logical functions on the device.
- **Host:** An Enhanced SuperSpeed host serves as a source or sink of information. It implements the required communications layers specific to Enhanced SuperSpeed on the host side. The host manages the Enhanced SuperSpeed bus, including the data activity schedule and the devices connected to it.

The Enhanced SuperSpeed bus architecture ensures efficient and reliable communication between the host and devices by defining the interconnect, device, and host components, along with their respective roles and responsibilities. Figure 4.8 illustrates the reference model for the terminology in this specification.

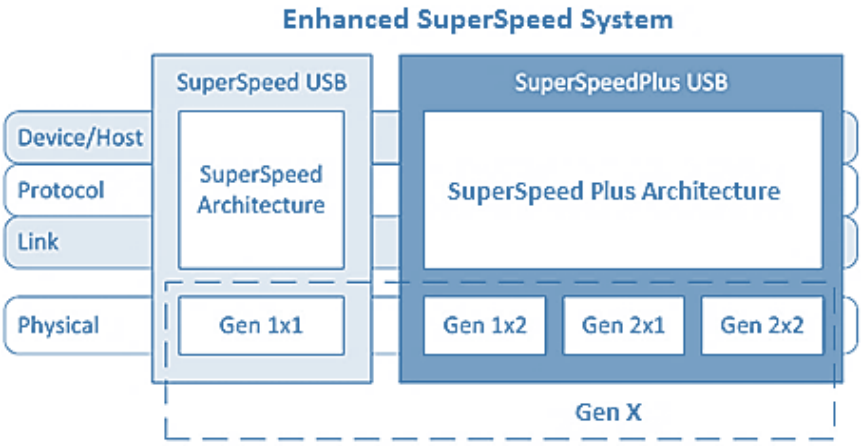


Fig. 4.8. USB 3.2 Terminology Reference Model [25].

### 4.7.5 Physical Layer

In [25], the physical layer of USB 3.2 includes the PHY (Physical Layer) component of a port and the physical connection between a downstream-facing port (on a host or hub) and the upstream-facing port on a device. In the Gen X physical connection, each lane consists of two differential data pairs, one for transmitting data and one for receiving data. Dual-lane support (Gen X*2) enables two-lane operation using the USB Type-C cable and connector.

The electrical aspects of each path within the physical layer are divided into a transmitter (TX), channel, and receiver (RX), forming a unidirectional differential sub-link. AC coupling is implemented with capacitors located on the transmitter (TX) side of the differential sub-link. The channel encompasses the electrical characteristics of the cables and connectors involved in the connection. At the electrical level, each differential sub-link is initialized by enabling its receiver (RX) termination. The transmitter (TX) detects the receiver (RX) termination at the far end, indicating a bus connection, and communicates this information to the link layer for proper management and operation. When receiver (RX) termination is present but no active signaling occurs on the differential sub-link, it enters the electrical idle state. In this state, low-frequency periodic signaling (LFPS) is utilized to signal initialization and power management information. LFPS is a simple and low-power method of signaling.

Each PHY has its own clock domain with Spread Spectrum Clocking (SSC) modulation. The USB 3.2 cable does not include a reference clock, so the clock domains on each end of the physical connection are not explicitly connected. Bit-level timing synchronization relies on the local

receiver (RX) aligning its bit recovery clock to the remote transmitter (TX)'s clock through phase-locking to the signal transitions in the received bit stream.

The receiver (RX) is responsible for reliably recovering clock and data from the bit stream. In Gen 1 operation, the transmitter (TX) encodes data and control characters into symbols. Control symbols are used for byte alignment, framing data, and managing the link. Special characteristics make control symbols distinguishable from data symbols. In Gen 2 operation, the transmitter (TX) block encodes the data and control bytes, and special control blocks are used for block alignment and link management in the receiver (RX).

Several techniques are employed to improve channel performance. For instance, transmitter (TX) de-emphasis may be applied to prevent overdriving and enhance eye margin at the receiver (RX) when multiple bits of the same polarity are transmitted. Equalization may also be utilized in the receiver (RX), with the equalization profile characteristics established adaptively during link training to optimize channel performance.

### 4.7.6 Gen 1 Physical Layer

The Gen 1 physical layer of USB 3.2 as described in [25], has a nominal signaling data rate is 5 Gb/s. To transmit data and control characters, a Gen 1 transmitter (TX) uses an 8b/10b encoding scheme. This means that 8-bit data from the link layer, along with control characters, are encoded into 10-bit symbols for transmission over the physical connection.

Before transmission, the physical layer scrambles the data to reduce electromagnetic interference (EMI) emissions. The scrambled 8-bit data is then encoded into 10-bit symbols, and spread spectrum is applied to further lower EMI emissions. The resulting bit stream, including the spread spectrum, is sent over the physical connection at the nominal signaling data rate of 5 Gb/s. At the receiver (RX) end, the bit stream is recovered from the differential sub-link. The receiver (RX) assembles the received bits into 10-bit symbols, and then decodes and descrambles them. This process produces the original 8-bit data, which is sent to the link layer for further processing. Figure 4.9 shows the Gen 1 transmitter (TX) and Receiver (RX) block diagram.

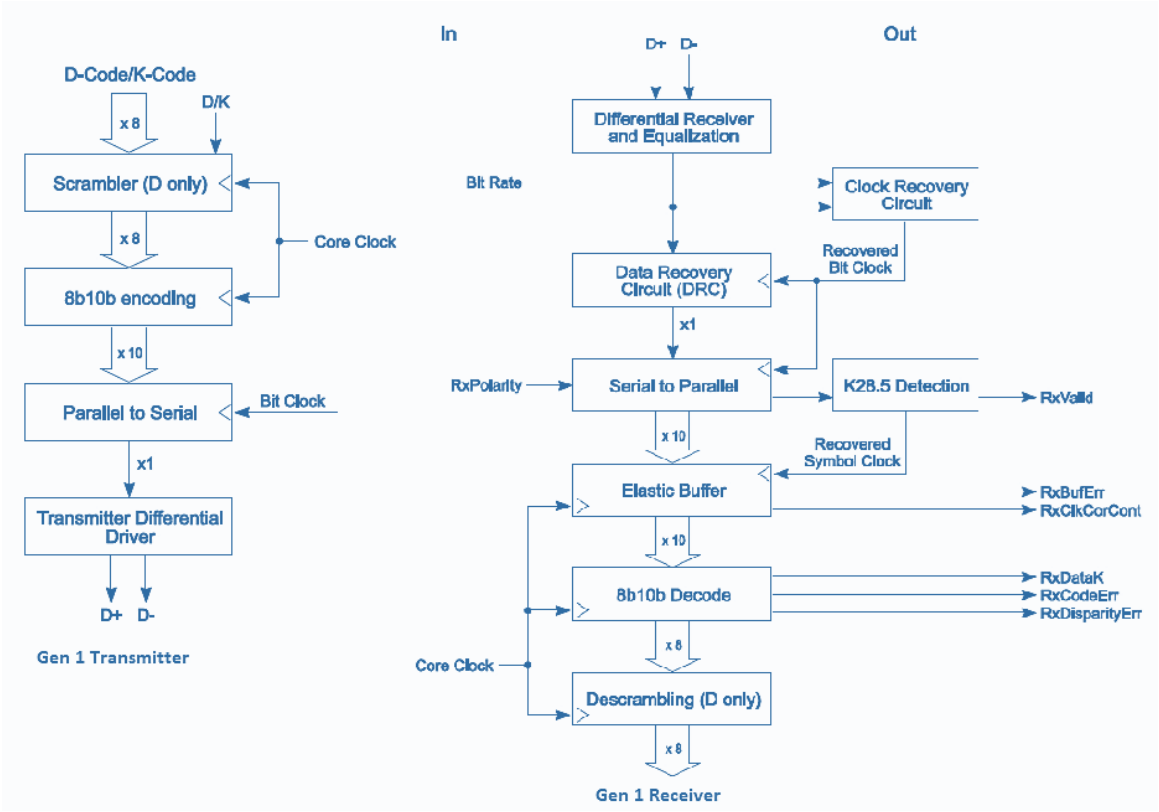


Fig. 4.9. Block Diagram for Gen 1 TX and RX [25].

In summary, the Gen 1 physical layer of USB 3.2 employs an 8b/10b encoding scheme to transmit data and control characters. Scrambling and spread spectrum techniques are applied to reduce EMI emissions. The receiver (RX) recovers the bit stream, decodes, and descrambles it to obtain the original data for further processing by the link layer.

### 4.7.7 Gen 2 Physical Layer

The Gen 2 physical layer of USB 3.2 as described in [25], operates at a nominal signaling data rate of 10 Gb/s. In the Gen 2 physical layer, a transmitter (TX) frames data and control bytes (referred to as symbols) by adding a 4-bit block identifier to 16 symbols, creating a 128b/132b block. The symbols within the block may undergo scrambling or remain unscrambled, depending on their type (data or control symbol). Like Gen 1, the resulting data is transmitted across the electrical interconnect using spread spectrum clocking to reduce electromagnetic interference (EMI) emissions.

At the receiver (RX) end, the bit stream is recovered from the electrical interconnect. The receiver (RX) assembles and aligns the received bits into 132-bit blocks. The data is then descrambled, and the identifier information and descrambled bits are passed on to the link layer for further

processing. Additionally, in Gen 2 operation, the PHY utilizes a protocol based on low-frequency periodic signaling (LFPS) to negotiate and determine the highest common data rate capability between two connected PHYs. This allows the PHYs to establish the most suitable data rate for communication. Figure 4.10 shows the Gen 2 transmitter (TX) and Receiver (RX) block diagram.

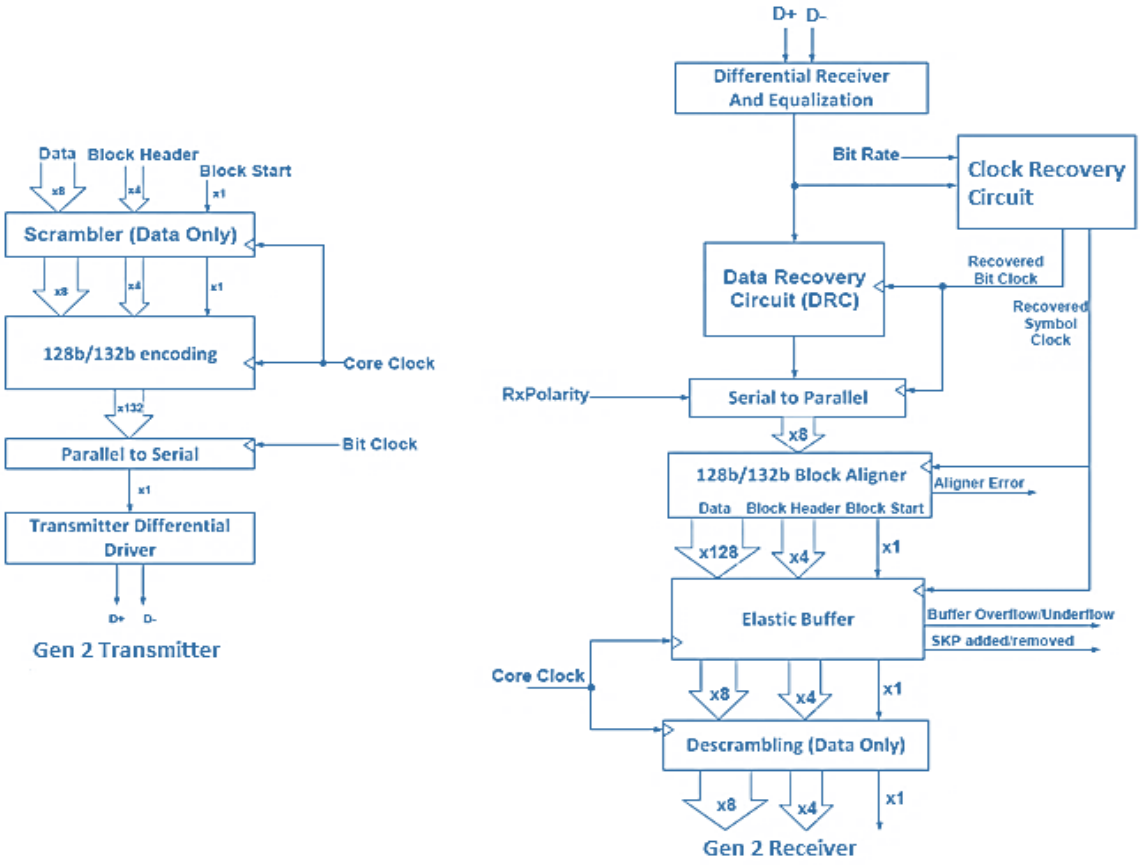


Fig. 4.10. Gen 2 transmitter (TX) and Receiver (RX) [25].

To summarize, the Gen 2 physical layer of USB 3.2 operates at a nominal signaling data rate of 10 Gb/s. Transmitter (TX)s frame data and control bytes into 128b/132b blocks, which are transmitted with spread spectrum clocking. Receiver (RX) s recover the bit stream, assemble and align the bits, descramble the data, and pass it to the link layer for further processing. Additionally, a negotiation protocol using LFPS signaling determines the highest common data rate between connected PHYs.

## 4.8 Summary

In conclusion, USB 3.2 has emerged as a significant advancement in the field of universal serial bus technology, providing enhanced data transfer speeds and improved performance over its predecessors. This architectural overview has shed light on the key features and specifications of USB 3.2, highlighting its potential to meet the increasing demands of modern data-intensive applications. USB 3.2 introduces the concept of multi-lane operation, allowing for the aggregation of multiple data lanes to achieve higher data transfer rates. With the SuperSpeed USB 10 Gbps and SuperSpeed USB 20 Gbps modes, USB 3.2 provides impressive throughput capabilities, enabling faster file transfers, improved multimedia streaming, and reduced latency.

Moreover, USB 3.2 maintains backward compatibility with previous USB generations, ensuring seamless connectivity and interoperability with existing USB devices. This backward compatibility, combined with the introduction of new connector types such as USB Type-C, makes USB 3.2 a versatile and future-proof solution for a wide range of devices, including laptops, desktops, smartphones, and other consumer electronics. The USB 3.2 architectural overview also touched upon the advancements in power delivery capabilities, offering increased power levels and more flexible power profiles to support the charging and powering of various devices. This enables the consolidation of power and data transmission through a single USB cable, simplifying connectivity and enhancing convenience.

# Chapter 5

# Equalization Techniques

## 5.1 Channel Impairments

Channel impairments which cause channel noise in high-speed USB3.2 systems have been prevalent reason for the signal to degrade while travelling from the transmitter (TX) side to the receiver (RX) side. These impairments arise from various sources and can degrade the signal quality, leading to bit errors and reduced data integrity at the receiver (RX) end of the system. Understanding and mitigating these channel noises are essential for designing robust and efficient USB 3.2 links. Some predominant channel impairments that cause signal losses in USB 3.2 system are as follows:

- **Resistive Loss:** Resistive losses in USB 3.2 systems occur due to the resistance encountered in the transmission path, resulting in power dissipation and signal degradation. These losses can have a significant impact on system performance and signal integrity. In USB 3.2 communication, resistive losses mainly arise in the conductors and transmission media used for signal transmission. The resistance of these components leads to power dissipation and signal attenuation. Key aspects of resistive losses in USB 3.2 systems include:

1. Power Dissipation: When electrical current flows through a conductor with resistance, it generates heat, causing power dissipation. This energy loss reduces the available power for signal transmission, increasing power consumption and heat generation.
2. Voltage Drops: Resistance in the transmission path causes voltage drops along the conductors. As the signal propagates, the voltage levels decrease due to this resistance. Voltage drops can cause signal distortion, reducing the voltage margins available for reliable signal detection at the receiver (RX). Excessive voltage drops may lead to signal errors.
3. Signal Attenuation: The resistance in the transmission path causes the signal strength to weaken as it travels. This attenuation results from power dissipation across the resistance. Weakened signals become more vulnerable to noise and interference, degrading the signal-to-noise ratio (SNR) and affecting the reach and reliability of the USB 3.2 link.
4. Impedance Mismatch: Resistive losses can also occur due to impedance mismatches in the transmission path. When the impedance of the transmitter (TX), transmission line, and receiver (RX) is not properly matched, a portion of the transmitted power reflects back, leading to

power losses and signal degradation. Techniques like controlled impedance routing and termination are used to minimize these losses.

- **Skin Effect:** The skin effect is a phenomenon observed in USB 3.2 transmission lines where high-frequency currents tend to concentrate near the surface of a conductor. As the signal frequency increases, the current prefers to flow through a thin layer close to the conductor's surface, reducing the available cross-sectional area for current transmission. At high frequencies, the skin effect causes the majority of the current to be confined to the thin surface layer of the conductor. This behaviour arises due to the electromagnetic fields generated by the changing current. The current's magnetic field induces a counteracting magnetic field within the conductor, pushing the current towards regions with weaker opposing fields, which happens to be the surface layer of the conductor.

The skin effect has notable implications in USB 3.2 transmission:

1. Increased Effective Resistance: The concentration of current near the surface layer reduces the effective cross-sectional area for current flow. This results in higher resistance, leading to increased power dissipation and resistive losses. These effects can impact signal quality and restrict the maximum achievable data rate. Skin effect is inversely proportional to skin depth and directly proportional to the frequency of the signal. Skin depth is the the distance from the outer surface to the strand of the conductor where the flow of current is maximum. This is indicated as ‘δ’ in figure 5.1.

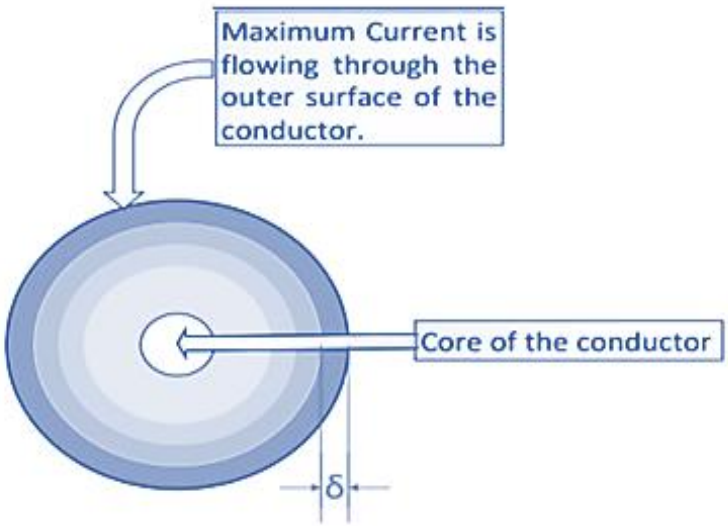


Fig. 5.1. Geometry of the Channel conductor where, δ is the skin depth [51].

The formula to calculate Skin depth is given as**:**

$$\boldsymbol{\delta = \frac{1}{\sqrt{\pi * f * \mu * \sigma}}} \qquad \text{Eqn. 1}$$

Where,

f- Frequency of the signal

μ- Relative permeability of conductor

σ- Conductivity of conductor

2. Attenuation of High-Frequency Components: The skin effect causes higher frequency components of the signal to experience greater attenuation compared to lower frequency components. As the signal propagates through the transmission line, the high-frequency content may suffer signal distortion and a decrease in amplitude. This limitation can restrict the bandwidth and introduce frequency-dependent losses.
3. Signal Delay and Phase Shift: Due to the current's preference for the surface layer, the effective current path is closer to the conductor's surface. This effectively increases the transmission line's effective length for high-frequency components, resulting in signal delay and phase shift relative to lower frequency components. Consequently, this can introduce signal distortion and affect the timing and synchronization of transmitted data.

- **Return Loss:** Return loss is another critical factor affecting the signal integrity and system performance in USB 3.2. It accounts for amount of power that is reflected back from the transmission line or the interface. Return loss occurs when there is an impedance mismatch between the source (transmitter (TX)) and the load (Receiver (RX)). Figure 5.2 shows a rough electrical representation of how a transmission line looks like in USB 3.2.

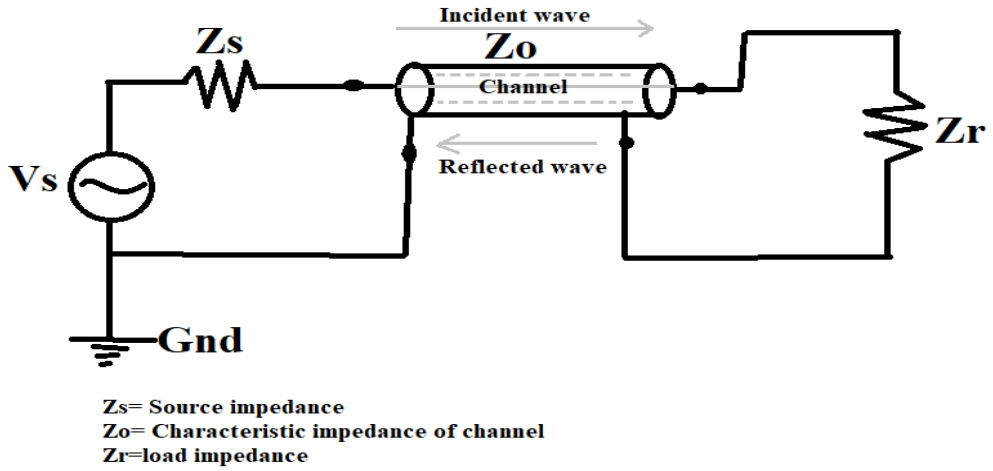


Fig.5.2. Transmission Line representation.

When a signal travels along a transmission line, it encounters a variation in load impedance ($Z_r$) compared to the line's characteristic impedance ($Z_0$). This variation represents a certain proportion or percentage of the signal that will reflect back to the transmitter (TX) and is given by the formula:

$$\Gamma = \frac{Z_r - Z_o}{Z_r + Z_o} \qquad \text{Eqn. 2}$$

Where, Γ is known as the transmission coefficient. In ideal condition, the characteristic impedance and the load impedance should be matched for maximum power transfer (measured in dB) of the signal at the receiver (RX) end. But, due to channel irregularities and parasitics, there is a mismatch between the impedances $Z_r$ and $Z_o$ which results in a part of the incident wave to reflect back towards the source (transmitter (TX)). The return loss is measured as the ratio of the reflected signal's power to the incident signal's power and is denoted in dB. High return loss indicates that a significant portion of the signal power is being reflected, which means less power is reaching the load. This can result in reduced signal amplitude, increased jitter, and degraded signal eye-diagram, leading to a decrease in the receiver (RX) 's ability to accurately detect and interpret the data. Return loss specifications cover a frequency range because impedance mismatches impact frequencies in distinct ways. With increasing frequency, the impact of impedance mismatches becomes more significant, underscoring the importance of evaluating return loss at the system's operating frequency.

The return loss is measured using specialized test equipment knows as the Vector Network Analyzer (VNA). A Vector Network Analyzer (VNA) is a useful tool for analyzing the behaviour of sine waves (signal waves) as they propagate through a transmission line. It

measures the ratio between the reflected and incident sine waves, known as the return loss or S11, as well as the ratio between the transmitted and incident sine waves, known as the insertion loss or S21as shown in Figure 5.3. These parameters, S11 and S21, or scattering parameters, provide a comprehensive description of how sine waves interact with the transmission line at each frequency.

Formula to calculate S-parameter is given as:

$$S(dB) = 20 * \log (mag(S)) \qquad \text{Eqn. 3}$$

Where:

$$mag(S) = \frac{\text{amplitude of Output sine wave}}{\text{amplitude of Input sine wave}}$$

To accurately measure these parameters, a 50-Ohm source and load are typically connected to the ends of the transmission line. If the characteristic impedance of the line differs from 50 Ohms, significant reflections can occur. Depending on the line's length and impedance discontinuities, periodic patterns may appear in the S parameters as the sine waves encounter resonances. [52].

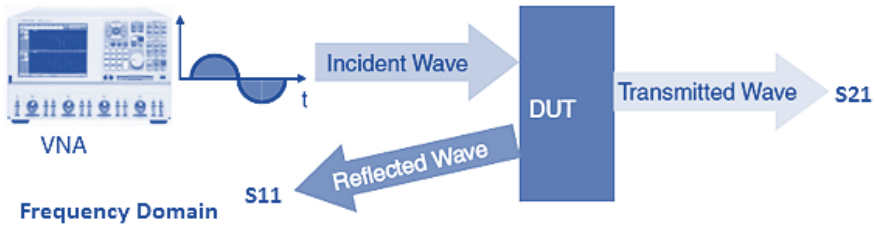


Fig.5.3. S-parameters are a formalism to describe how precision waveforms scatter from an interconnect or device under test (DUT) [52].

- **Crosstalk:** According to [53] ,crosstalk is a common phenomenon in USB 3.2 systems that can significantly impact signal integrity. It occurs when the signals from one channel interfere with and affect the signals on adjacent or nearby channels. This interference can lead to signal distortions, data errors, and reduced overall system performance. When a signal travels through an interconnect, it creates an electromagnetic wave that spans between multiple conductors. When these transmission structures are situated closely together, the electric and magnetic fields of the signal extend and interact with neighboring conductors. As a result, energy from the signal can couple or transfer to adjacent transmission structures when a stimulus is present.

This phenomenon is commonly referred to as crosstalk. Crosstalk, from a circuit perspective, arises due to the presence of mutual inductance and mutual capacitance between conductors. These two phenomena facilitate the transfer of energy between lines through the magnetic field (in the case of mutual inductance) and the electric field (in the case of mutual capacitance).

Mutual inductance, denoted as $L_M$, results in the transfer of current from a driven line to a nearby quiet line through the magnetic field, as depicted in Figure 5.4. In simple terms, if the victim trace is positioned close to the driven line such that their magnetic flux lines intersect, it will induce a current on the victim line. This mutual inductance generates voltage noise on the victim line, which is directly proportional to the rate of change of current on the driven line, as described by the specific equation:

$$\Delta V_L = L_M \frac{di}{dt} \qquad \text{Eqn 4}$$

Where, $\Delta V_L$, is the voltage coupled by the mutual inductance $L_M$, in response to the transient current i.

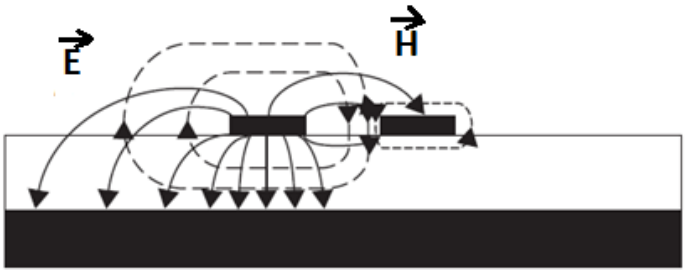


Fig.5.4. Coupled PCB transmission lines

Mutual capacitance represented as $C_M$, refers to the coupling of conductors through the electric field. When the victim trace is positioned close enough to a driven line as shown in Figure 5.4, such that its electric field lines intersect with the victim trace, a current is induced on the victim line. This induced current is directly proportional to the rate of change of voltage on the driven line and is represented by the formulae:

$$\Delta I_C = C_M \frac{dv}{dt} \qquad \text{Eqn 5}$$

Where, $\Delta I_C$, is the amount of current coupled through the mutual capacitance $C_M$, when driven by the voltage signal v.

There are two type of cross-talks that occur in a transmission line:

1. **Near End Crosstalk (NEXT):** NEXT is a type of crosstalk that occurs at the receiving end of a transmission line, or the driver side of the victim interconnect as shown in Figure 5.5. It happens when the transmitted aggressor signal interferes with and affects victim signals at its driver end, resulting in signal distortion and potential errors.
2. **Far End Crosstalk (FEXT):** FEXT is a type of crosstalk that occurs at the receiving end of the victim interconnect as shown in Figure 5.5. It happens when the transmitted aggressor signal induces interference on victim signals at the receiving end, leading to signal distortion and degradation.

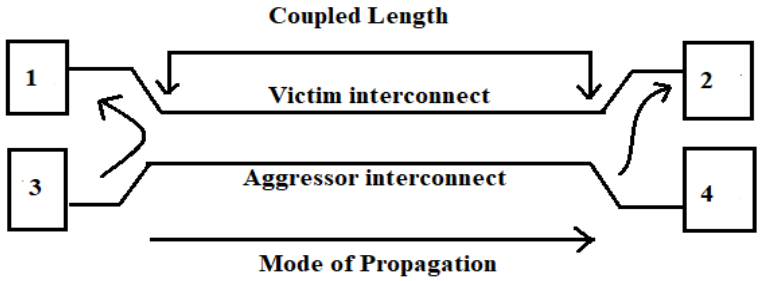


Fig. 5.5. Illustration of NEXT and FEXT. As the aggressor signal propagates from port 3 to port 4, Near-End XTalk appears on port 1 and Far-End XTalk appears on port 2 after one time delay (TD) of the interconnect.

- **ISI:** According to [54], in digital communication, symbols are used to represent information, and these symbols are typically transmitted over a channel. The channel introduces certain characteristics that can cause the symbols to overlap and interfere with each other as shown in Figure 5.6. This interference can result in errors in symbol detection and decoding at the receiver (RX), leading to a loss of data accuracy. Inter Symbol Interference (ISI) is a phenomenon that occurs in high-speed digital communication systems where the transmitted symbols interfere with each other, resulting in degradation of the received signal quality.

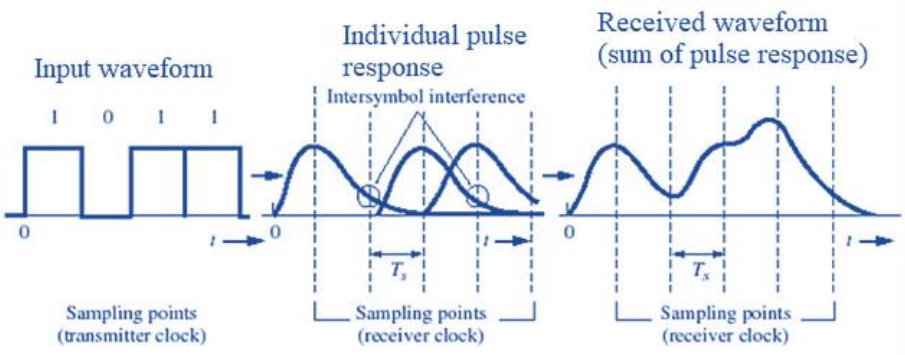


Fig. 5.6. Effect of ISI on the input waveform at the RX end [55].

Moreover, channel distortion, such as multipath propagation, can also contribute to ISI. In multipath environments, the transmitted signal reaches the receiver (RX) through multiple paths

due to reflections and scattering. Each path introduces a delayed and attenuated version of the signal, causing overlapping of symbols in the time domain and resulting in interference.

Inter Symbol Interference (ISI) is a significant challenge in high-speed digital communication systems. It occurs when transmitted symbols interfere with each other, leading to errors in symbol detection. Understanding the causes of ISI and implementing appropriate equalization techniques are crucial for mitigating its effects and ensuring reliable data transmission.

- **Jitter:** Jitter is the term used to describe the fluctuation or deviation from the desired timing of a signal's edges. It occurs because of various factors, such as noise, uncertainties in timing, challenges related to signal integrity, and imperfections in the transmitter (TX) and receiver (RX) components. According to [56], Every transmitter (TX) device exhibits a certain level of jitter in the transmitted data bits. Jitter generation refers to the measurement of timing variations within the transmitted data stream. In some cases, applications may impose specific limits on the maximum allowable jitter generation by a transmitter (TX) device, subject to predefined test conditions. These test conditions often involve the specification of test patterns and the connection of the transmitter (TX) device to a particular load. The jitter produced by the transmitter (TX) device undergoes amplification when it traverses through the channel. As the signal travels through the channel, it experiences distortion and frequency-dependent phase shifts. When the data pattern switches between 1s and 0s, the spectral characteristics of the data change accordingly. Consequently, the varying delay introduced by the channel adds to the overall jitter at the receiver (RX). Additionally, factors such as crosstalk, reflections caused by impedance inconsistencies, and return loss contribute to shifting the transition points of signal edges at the receiver (RX).

Also [56] mentions that in the field of data communication, jitter is commonly classified into two main components: deterministic jitter (DJ) and random jitter (RJ). These two categories accumulate differently within the link and give rise to distinct requirements for compliance and budgeting strategies.

1. **Deterministic Jitter:** Deterministic jitter (DJ) refers to the portion of total jitter that has a non-Gaussian distribution. DJ is characterized by a bounded amplitude and is caused by specific, identifiable factors. In the literature [1], DJ is also referred to as high probability jitter (HPJ). There are typically four types of jitters included within the DJ component:

- Duty cycle distortion (DCD): DCD occurs when there is a difference in width between logic "0" and logic "1" signals. This type of DJ arises from driver circuits with unequal rise and fall

times. Another cause of DCD is the presence of a DC voltage offset between the true and complementary legs of a differential signal. Additionally, DCD can be influenced by pulse width shrinkage due to passive or active components within the channel, and it is sometimes referred to as pulse width distortion.

- Data dependent jitter (DDJ): DDJ encompasses timing variations resulting from non-clock-like serial data waveforms as they propagate through a channel with limited bandwidth. By having knowledge of the preceding and subsequent bits in the transmission, DDJ can be predicted and mitigated through equalization techniques. DDJ is also known as pattern-dependent jitter or Intersymbol Interference (ISI).
- Periodic jitter (PJ): PJ is characterized by a single fundamental harmonic along with potential even and odd harmonics. Various electromagnetic noise sources in the system, such as power supply noise and crosstalk from periodic signals, contribute to PJ. Clock signals act as periodic signals that induce crosstalk leading to PJ in the affected signal.
- Sinusoidal jitter (SJ): SJ refers to jitter with a single fundamental harmonic and no additional harmonics. It is primarily defined within the context of applied SJ for receiver (RX) device jitter tolerance testing. Therefore, it is typically treated separately from periodic jitter originating from system sources.

2. **Random Jitter:** Random jitter (RJ) pertains to the portion of total jitter that adheres to a Gaussian distribution. RJ is also referred to as Gaussian jitter (GJ). RJ arises from semiconductor imperfections, quantum effects, and specific types of crosstalk. There are typically two types of jitters included within the RJ component:

- Uncorrelated unbounded Gaussian jitter (UUGJ): UUGJ represents the RJ component characterized by a true Gaussian distribution. It originates from imperfections in the semiconductor crystal lattice, thermal vibrations of conductor atoms, and various other small contributing factors. As the measurement time increases, the peak-to-peak value of UUGJ grows when observed over time.

3. **Correlated bounded Gaussian jitter (CBGJ):** CBGJ encompasses the RJ component with a Gaussian distribution, but with bounded amplitude and correlation to the transmitted signal amplitude. When crosstalk aggressor signals operate at a baud rate asynchronous to that of the victim, the resulting jitter on the victim can be approximated as a bounded Gaussian distribution. This type of jitter is included within the CBGJ component.

## 5.2 Eye-diagram

USB 3.2 communication plays a crucial role in modern high-speed data transmission systems, enabling efficient and reliable data transfer across various digital interfaces [57]. To assess the quality and integrity of the transmitted signals, engineers employ the eye-diagram [18]. The eye-diagram as shown in Figure 5.7, is a graphical representation of a digital signal's behaviour over time, displaying the superimposed waveforms of multiple data bits [18]. It derives its name from the resemblance of the graph to an open eye. By observing the eye-diagram, engineers can evaluate signal quality, detect impairments, and optimize the system's performance [57].

According to [18], an eye-diagram is generated by dividing the time-domain signal waveform into segments that encompass a small number of symbols and overlaying them. The time axis, represented horizontally, typically spans one or two symbols, while the vertical axis represents the signal's amplitude. The construction process of the eye-diagram, illustrated in Figure 5.8, demonstrates both an ideal "perfect" eye and one that exhibits distortion due to losses and/or reflections.

The visual depiction in Figure 5.8, reveals that signal distortion leads to the closure of the data eye. Ideally, we strive for an "open" eye, as a larger eye opening indicates a greater margin in voltage and timing requirements. Evaluating link performance quantitatively, the minimum height and width of the data at the receiver (RX) serve as crucial metrics. The eye's width should provide sufficient time to meet the receiver (RX) 's setup and hold requirements, while its height ensures that voltage levels comply with $v_{ih}$ (input high voltage) and $v_{il}$ (input low voltage) specifications in the presence of multiple sources of noise. This enables the successful resolution of input signals into digital values by the receiver (RX).

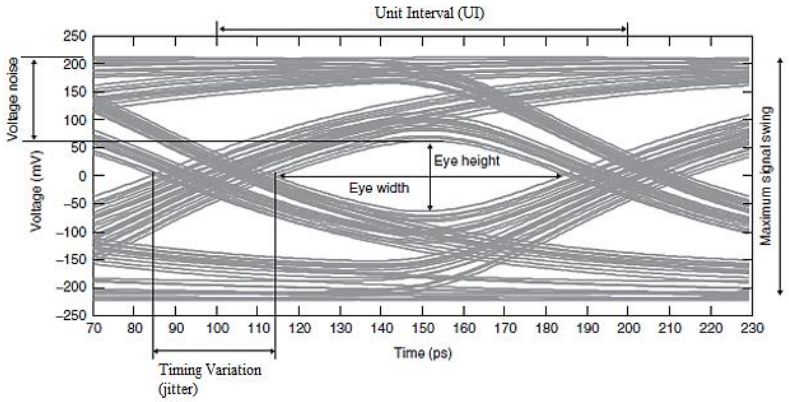


Fig. 5.7. Eye-diagram for a 10-Gb/s 100-bit Data Sequence [18].

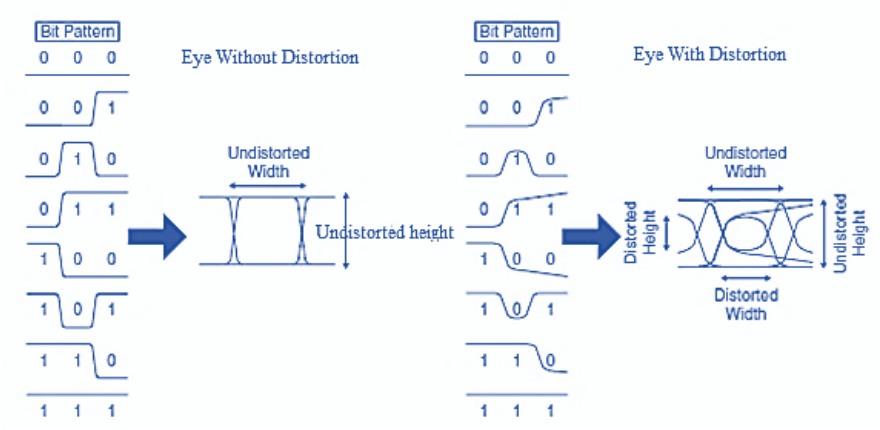


Fig. 5.8. Eye-diagram Construction Process and the Impact of Signal Distortion [18].

An eye-diagram typically consists of three main components: the vertical opening, horizontal width, and jitter [18].

**Vertical Opening:** The vertical opening represents the amplitude range of the signal. It is determined by the voltage levels of the high and low logic states. A smaller vertical opening indicates reduced noise margin and potential signal integrity issues [57].

**Horizontal Width:** The horizontal width represents the time interval of a single bit or unit interval (UI). It is usually measured from the 50% points of the rising and falling edges. An optimal eye-diagram exhibits a wide and symmetric eye opening, indicating a clear distinction between logic states [57].

Furthermore, the eye-diagram can be utilized to estimate the likelihood of receiving incorrect bits, commonly referred to as the bit error rate (BER) or bit error ratio. The BER is determined by calculating the ratio of erroneous received bits to the total number of transmitted bits over a significant duration:

$$BER\ (t_s, v_s) = \lim_{N \to \infty} \frac{N_{err}\ (t_s, v_s)}{N} \qquad \text{Eqn 6}$$

In the equation, $(t_s, v_s)$ denotes the relative voltages and times at which the signal is sampled, $N_{err}$ represents the count of erroneous bits received, and N signifies the total number of bits transmitted within the same time interval.

BER is very critical at system level for validation purposes. The estimated BER in industries is 1 error out of $10^{12}$ bits that are transferred.

## 5.3 Need for RX Equalization

Section 5.1 highlighted the main channel impairments occurring in high-speed serial link which adds noise to the signal and causes signal distortion. However, there are few techniques to avoid or lessen them such as transmitter (TX) pre-emphasis, proper interconnect width selection, using different filters at the transmitter (TX) end to curb the losses, insulating the interconnects and vias to avoid interference of signals and using EMC and EMI protection circuits, etc. But there are still few losses that cannot be controlled while the signal is on the move via the channel such as ISI, channel parasitics and Jitter. To compensate for these losses, a technique called equalization is implemented at the receiver (RX) end of the USB 3.2 architecture. The main objective of receiver (RX) equalization is to mitigate the distortions caused by the channel, allowing the receiver (RX) to interpret the signals and retrieve the original data from it without or with minimum errors. The need of receiver (RX) equalization is to eliminate the following impairments:

**Compensating for Attenuation:** Attenuation, a prevalent channel impairment, causes a reduction in signal amplitude as it propagates through the transmission medium. To mitigate this effect, receiver (RX) equalization techniques such as analog equalizers or digital filters are utilized. These techniques amplify the attenuated signals, restoring their original amplitudes and improving the overall signal-to-noise ratio.

**Mitigating Distortion:** Distortion can occur in the channel due to various factors such as signal reflections, frequency-dependent losses, and nonlinearities. Receiver (RX) equalization techniques, including adaptive equalizers or decision feedback equalizers, aim to counteract distortion by adjusting the received signal to match the original transmitted waveform. This adjustment minimizes errors caused by distortion and enhances the accuracy of signal detection.

**Addressing Inter-Symbol Interference (ISI):** Inter-Symbol Interference (ISI) arises when symbols from adjacent bits overlap, resulting in confusion and errors during signal detection. Receiver (RX) equalization techniques, such as linear equalizers or maximum likelihood sequence estimation (MLSE), are employed to mitigate ISI. These techniques utilize time-domain filtering or advanced algorithms that consider the statistical properties of the transmitted data, improving the receiver (RX) 's ability to accurately distinguish individual symbols.

## 5.4 Receiver (RX) Equalization Techniques for USB 3.2

With advancements in the operating speed of different USB versions, there have been significant changes in receiver (RX) equalization techniques as well. Some of the techniques are implemented

using software and others are implemented using hardware. For validation purpose in USB 3.2, there are prominently three receiver (RX) equalization techniques used to mitigate the channel losses namely: Continuous Time Linear Equalization (CTLE), Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE).

1. **Continuous Time Linear Equalization (CTLE):** According to [58], in a serial-data channel, the signal undergoes attenuation, with higher frequencies experiencing greater attenuation compared to lower frequencies. The purpose of Continuous-Time Linear Equalization (CTLE) is to enhance the higher frequencies at the receiver (RX), bringing all frequency components of the signal to a similar amplitude. This process improves the performance of jitter and eye-diagram. The objective is to equalize the combined characteristics of the transmitter (TX) and channel, eliminating Inter-Symbol Interference (ISI) at the sampling points of the received signal. When implementing CTLE, it operates on an analog input signal that has already been sampled by a sample-and-hold circuit. The term "linear" is used because it consists of no non-linear components. Typically, it is represented as a finite impulse response (FIR) filter with two poles (one zero). Figure 5.9 shows transfer function for different AC gain of Gen 2 Compliance receiver (RX) equalization.

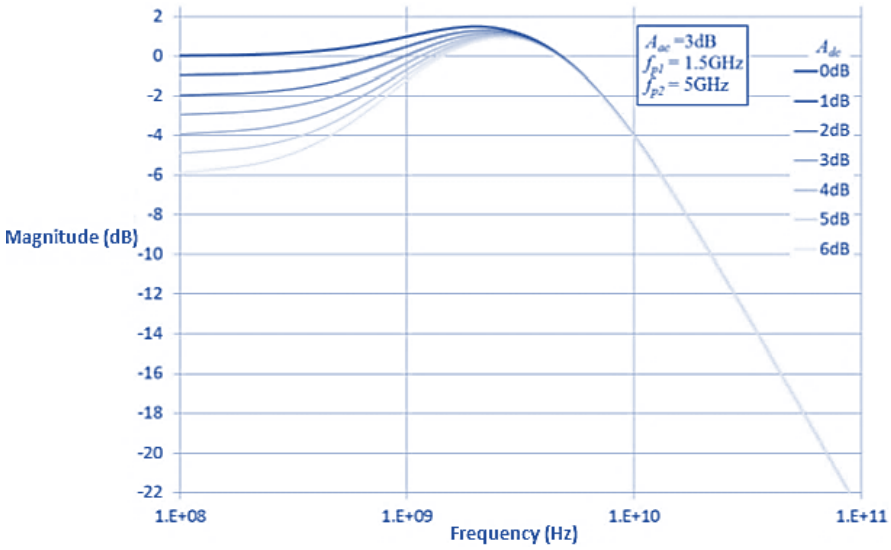


Fig. 5.9. Gen 2 Compliance Rx EQ Transfer Function [25].

The selection of DC gain values for the filter poles depends on the characteristics of the channel loss. In the case of a low-loss channel with a short physical length, the gain value approaches 0 dB, indicating minimal equalization. However, some level of CTLE is still necessary to create an inverse response to the channel. It is crucial not to excessively boost high frequencies beyond what is required, as this would negatively impact the noise performance. The frequency

response for the Gen 2 reference continuous time linear equalizer (CTLE) that is used for compliance testing is given as:

$$H(s) = A_{ac}\,\omega_{p2}\,\frac{S+\frac{A_{dc}}{A_{ac}}\omega_{p1}}{(s+\omega_{p1})(s+\omega_{p2})} \qquad \text{Eqn 7}$$

Where $A_{ac}$ is the high frequency peak gain

$A_{dc}$ is the DC gain

$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency

$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

For optimal CTLE performance, it is desirable to position the zero and first pole of the equalizer as closely together as feasible. The first zero contributes to boosting high frequencies, which in turn helps open the eye-diagram. By placing the first pole appropriately, the issue of peaking at the center of the eye can be avoided, while the second pole assists in limiting the bandwidth. It is important to refrain from equalizing the entire frequency band, especially including the noise frequencies. Excessive equalization runs the risk of generating a non-linear phase response. Moreover, with more boosting of higher frequencies, the noise frequencies are also boosted and hence noise performance degrades.

2. **Feed Forward Equalization (FFE):** According to [59], in addition to continuous time linear equalization (CTLE), another technique used to enhance signal quality in USB 3.2 systems is Feed-Forward Equalization (FFE). FFE, similar to pre-emphasis filtering on the transmitter (TX) side, involves implementing a digital finite impulse response (FIR) filter. FFE creates delayed versions of the input signal and combines them with appropriate weights. Typically, a delay of 1 unit interval (UI) is used. FFE implementations can utilize multiple-tap filters with various tap coefficients, including both pre-cursor and post-cursor taps. The weights assigned to these taps can be positive or negative, depending on their pre- or post-cursor positions. It is crucial to note that in a passive equalizer like FFE, the sum of all tap values must equal 1 in terms of net amplitude.

Figure 5.10 illustrates the block diagram of an M tap FFE, and its input/output relationship is described by [28]:

$$Y(nT) = \sum_{i=1}^{M} C_i \; . x((n+1-i)T) \qquad \text{Eqn. 8}$$

In the given context, the input and output signals are represented by x(n) and y(n) respectively. Ci represents the $i^{th}$ coefficient, while M denotes the number of taps. The input signal, x(n), travels through a delay line consisting of M delay elements of unit intervals. These delayed signals are then multiplied by adjustable coefficients and ultimately summed together. Among the taps within the delay line, the one near the center is commonly known as the main tap. The taps that come after and before the main tap are referred to as post-cursor and pre-cursor taps respectively.

To generate the output waveform, the individual stages of the Feed-Forward Equalization (FFE) process are combined by summing the weighted outputs of each delay block. This summation takes place at a summing node, and the resulting combined output is then fed to a bit slicer. This process mirrors the pre-emphasis performed at the transmitter (TX), but in this case, it compensates for pre- and post-cursor Inter-Symbol Interference (ISI) in the received signal [59].

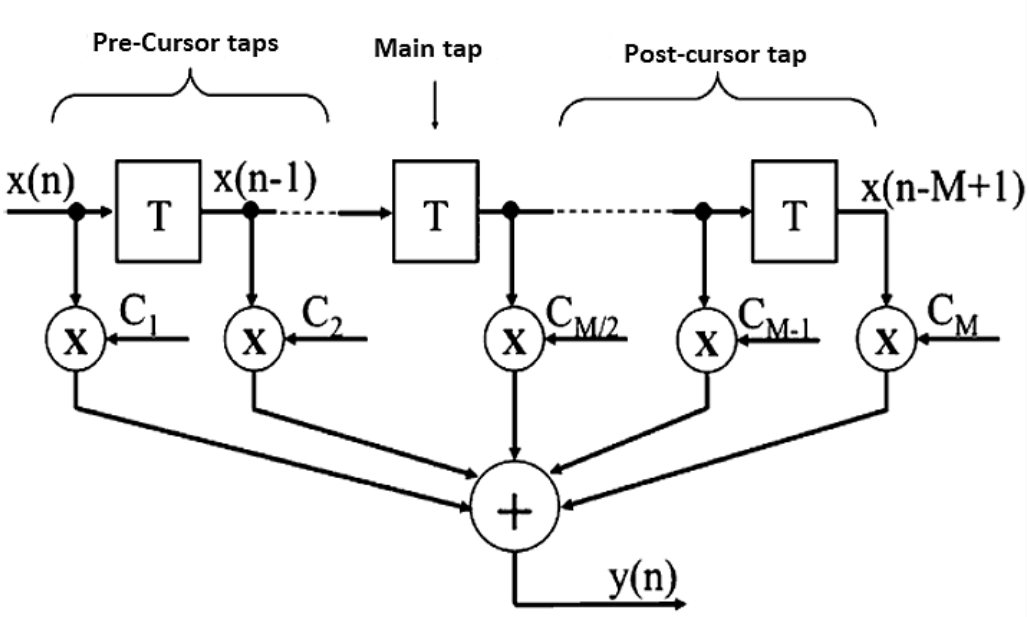


Fig. 5.9. Block diagram of a M tap FFE [28].

It is important to note that FFE implementations typically require significant power consumption and occupy a considerable amount of chip real estate due to the multiple delay elements and tap coefficients involved. As a result, FFE is commonly utilized in high-cost designs where equalization plays a crucial role. However, it is worth mentioning that since FFE compensates for the signal after it has traversed the channel, it tends to amplify high frequencies, thereby increasing noise levels [59].

3. **Decision Feedback Equalization (DFE):** DFE (Decision Feedback Equalization) is an essential equalization technique used in USB 3.2 systems to combat Intersymbol Interference (ISI) and improve the overall signal quality. DFE operates by making decisions based on previously received symbols and using them to cancel the interference caused by those symbols [60].

According to [25], the DFE (Decision Feedback Equalization) technique comprises two main components: a first order Continuous Time Linear Equalizer (CTLE) and a feedback filter (FB). The CTLE processes the incoming signal to estimate the transmitted symbol, while the FB filter nullifies the intersymbol interference (ISI) caused by previously transmitted symbols. The CTLE in DFE performs a linear filtering operation on the received signal using a weighted sum of past symbols. The tap weights are adjusted to minimize the difference between the estimated and actual received symbols. By effectively equalizing the received signal, the CTLE mitigates the impact of intersymbol interference and enhances the overall signal integrity. Figure 5.10 shows the block diagram of a DFE used in USB 3.2 receiver (RX) equalization.

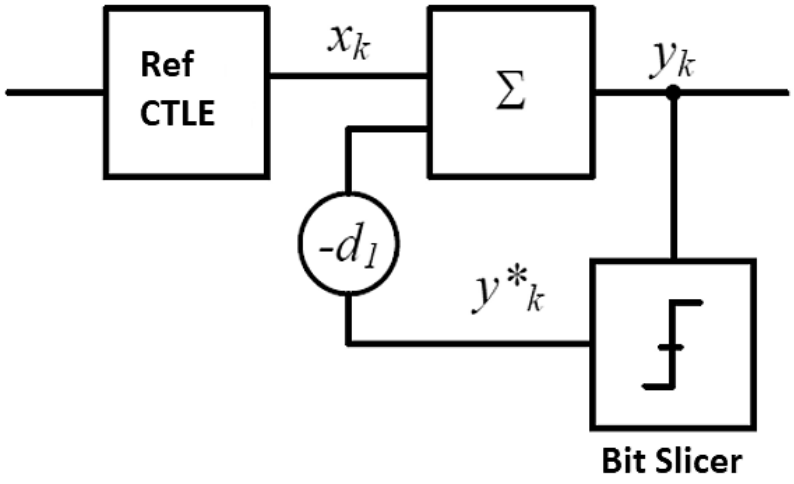


Fig. 5.10. Gen 2 reference DFE Function block diagram [25].

The feedback filter in DFE plays a critical role in canceling out the ISI introduced by the previously transmitted symbols. It utilizes the decisions made by the CTLE to estimate the ISI and subtract it from the received signal. This feedback mechanism enables interference cancellation, resulting in more accurate subsequent decisions. The DFE behaviour is described by equation:

$$y_k = x_k - d_1 \, \mathrm{sgn}(y_{k-1}) \qquad \text{Eqn. 9}$$

where, $y_k$ is the DFE differential output voltage

y*k is the decision function output voltage, |y*k| = 1

$x_k$ is the DFE differential input voltage

$d_1$ is the DFE feedback coefficient

k is the sample index in UI

One significant advantage of DFE is its adaptability. It continuously updates the tap weights of the CTLE, and FB filters based on the received symbols, allowing it to adapt to changing channel conditions and maintain optimal performance. This adaptability makes DFE well-suited for communication systems operating in dynamic environments where channel characteristics may vary over time.

## 5.5 Summary

Receiver (RX) equalization techniques play a crucial role in enhancing the performance and reliability of USB 3.2 interfaces. Throughout this discussion, we have explored various receiver (RX) equalization techniques employed in USB 3.2 to mitigate the effects of channel impairments and ensure robust signal integrity. Different types of channel impairments and their position of occurrence in the USB 3.2 communication channel were explained. It was established that these impairments cause the signal degradation at the receiver (RX) end. Also, importance of an eye-diagram was looked upon and found how eye-diagram helps to study the signal quality in USB 3.2. Finally, the need of equalization along with different receiver (RX) equalization techniques used for USB 3.2 validation were studied.

# Chapter 6

# Measurements and Results

## 6.1 Introduction

In this section the focus is on performing receiver (RX) equalization techniques on a USB 3.2 to analyze their effectiveness in combating signal impairments. The goal is to evaluate the performance of different equalization strategies and identify the most suitable approach from validation perspective. To accomplish this, a lab setup was prepared using the equipments used for validation purpose including the transmitter (TX), channel, and receiver (RX). Also, the channel impairments such as frequency-dependent loss, Inter-Symbol Interference (ISI), and crosstalk were replicated using noise board.

The lab setup allowed to assess the performance of various equalization techniques, such as Continuous Time Linear Equalization (CTLE), Decision Feedback Equalization (DFE), and Feed Forward Equalization (FFE). Throughout the experiment, influence of different channel impairments and noise sources on the system's performance were analyzed and effectiveness of each equalization technique in mitigating these impairments were also evaluated.

Furthermore, the efficiency of these equalization techniques based on their capability of opening the eye by mitigating the channel noises were investigated. The aim was to provide insights into the practical implementation of equalization techniques for USB 3.2 devices for post- Silicon validation purposes, considering real-world constraints and requirements. The results of this research will contribute to the understanding of equalization techniques for high-speed communication systems, particularly in the context of USB 3.2.

In the subsequent sections of this thesis, the measurement setup, the steps followed, and analyses of the results obtained through simulations are presented. Moreover, valuable insights on the application of the most efficient equalization technique that can be used for RX and TX behaviour analysis during product validation of USB 3.2 based devices were also provided.

## 6.2 Measurement Setup

Figure 6.1 shows the measurement setup and connections that were done in order to emulate the high-speed channel in a lab environment and to carry out the experiments that were required for this thesis.

The measurement setup consists of following components:

1. **A 120 MHz Pulse Function Arbitrary Generator (PFAG)-** A Pulse Function Arbitrary Noise Generator is a high-precision pulse generator enhanced with versatile signal generation, modulation, and distortion capabilities to stress the Device Under Test (DUT) to its limit. Some key features of the PFAG used are:
   - Signal type: pulse (frequency up to 120 Mhz), sine arbitrary (frequency up to 240 Mhz), ramp square, noise.
   - Number of outputs: 2 differential outputs.
   - Frequency range- 500 Mhz.
   - Amplitude- 50mV to 5V (peak-to-peak)
2. **A 33GHz Digital Signal Analyzer-** Some key features of the Digital Signal Analyzer used are:
   - 33 GHz of real-time bandwidth (upgradable to 63 GHz)
   - 80 GSa/s sample rate on 4 channels
   - Memory depth that captured milliseconds of data at 160 GSa/s
   - Clock recovery on NRZ data rates as fast as 120 Gb/s
3. **USB 3.1 Compliance Load Board (CLB) (5.6")-** The USB 3.1 Compliance Load Board emulated the host transmitter (TX) in this experiment. It connected the differential outputs of the PFAG to the input of the device receiver (RX) via an USB type-C cable as shown in Figure 6.1. The total trace length of the load board was 5.6 inches.
4. **Device 1C Fixture (Adapter):** The device 1C fixture acted as an interface between the Device Under Test (DUT) and the Oscilloscope which was emulating the receiver (RX) in this experiment. The fixture connected the Device's transmitter (TX) pins to the oscilloscope's receiver (RX) pins which enabled the oscilloscope to read the signals. It also Emulated a power delivery link partner for the DUT. Connection of Device fixture is shown in Figure 6.1.
5. **ISI Channel Board:** The ISI channel board used in this experiment emulates the channel noises ranging from minimum of -3.7 dB loss to a maximum of -14 dB loss. There are different

trace lengths which corresponds to different dB losses. For our experiment, we had considered trace number 23 for -10dB loss replication in the channel and trace number 35 for the maximum practical loss in USB 3.2 channel, which was-14dB and obtained the respective eye-diagrams.

6. **Device Under Test:** The device used for this experiment was a USB 3.2 removable storage device (1 Tera Byte) with dual lane which supports 10Gb/s transfer speed on both the lanes.
7. **SMA Cable:** The SMA (Subminiature version A) connectors used for this experiment are semi-precision coaxial RF connectors. They were designed to serve as a compact interface for coaxial cable, utilizing a screw-type coupling mechanism. These connectors maintain a consistent impedance of 50 Ω and have an outer diameter of 4.13mm.
8. **Power Supply:** The power supply used provided a constant DC voltage of 5 V.
9. **Type C Cable:** USB type- C cable was used to connect the USB compliance board to the device 1C fixture in order to transfer the pings from PFAG to the device.

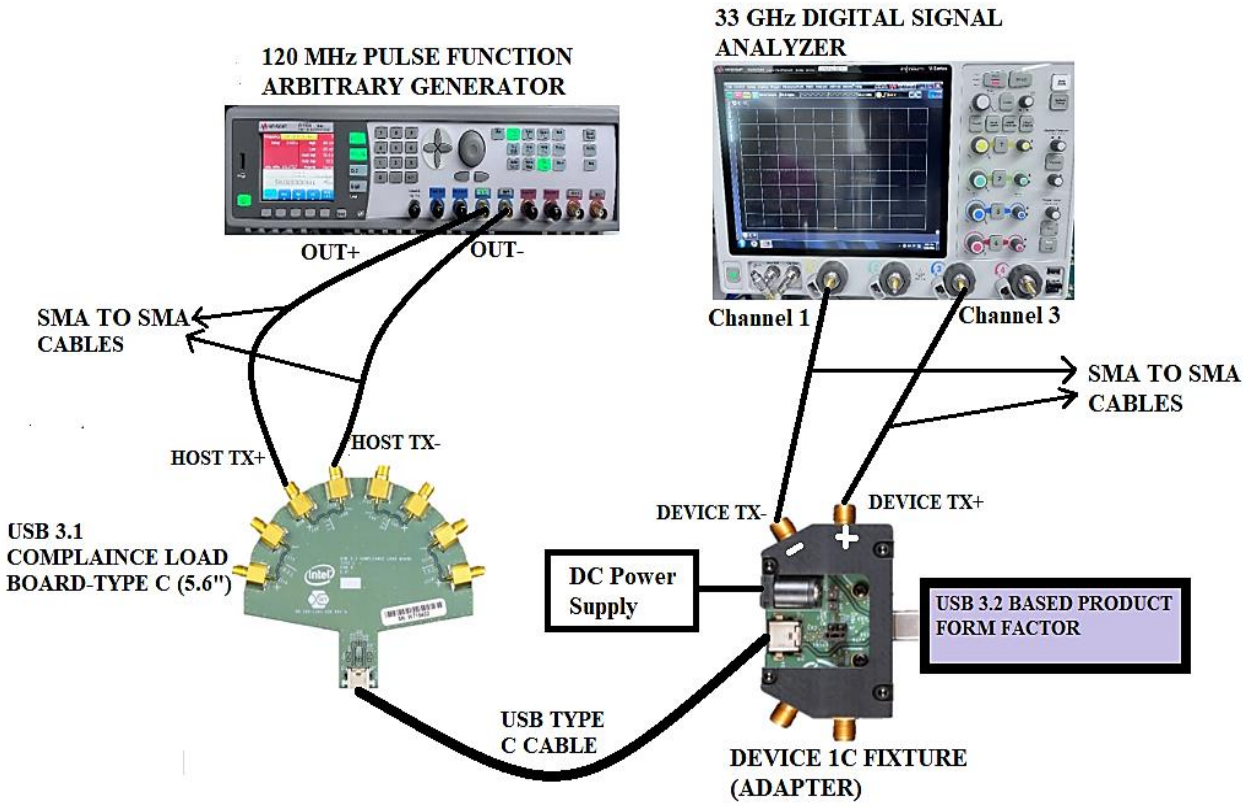


Fig. 6.1. Measurement Setup for Experiment without the ISI channel board connected.

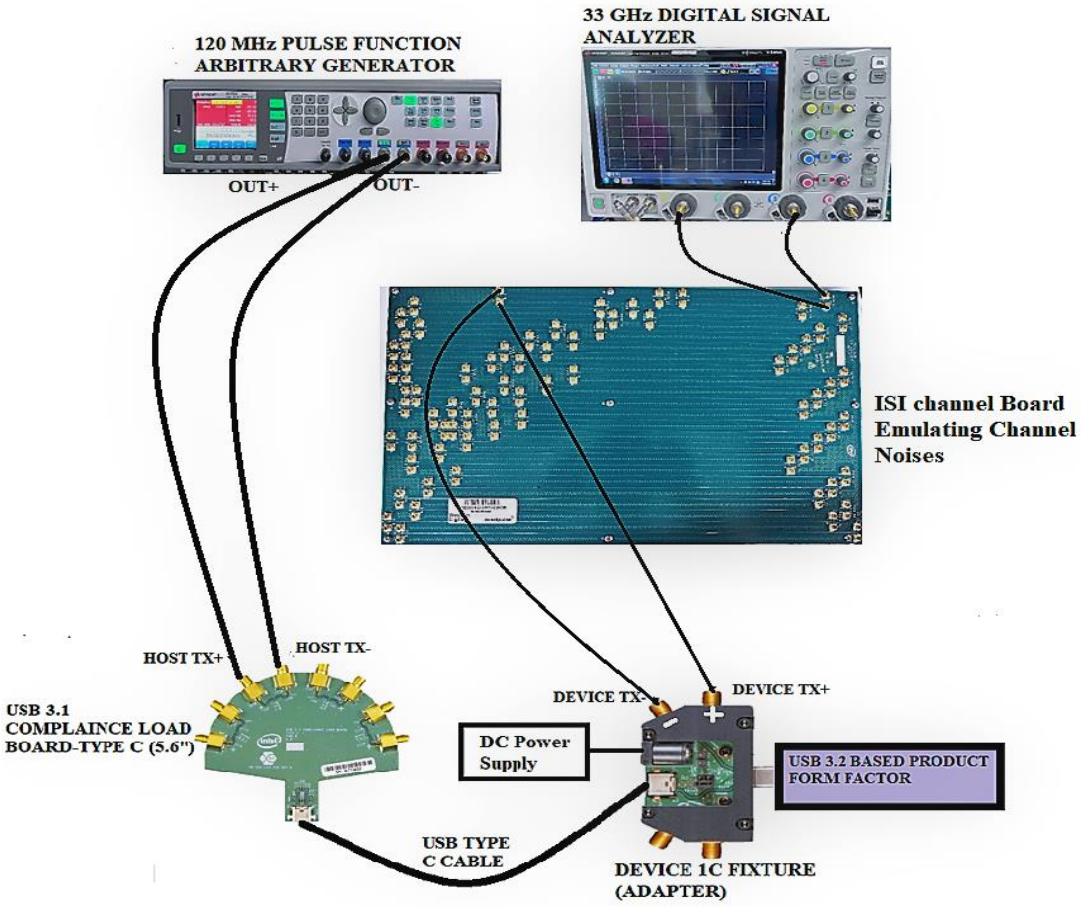


Fig. 6.2. Measurement Setup for Experiment with the ISI channel board connected.

## 6.3 Working of The Measurement Setup

The working of the measurement setup for performing the equalization techniques follows the following steps:

1. The Pulse Function Arbitrary Generator also known as Signal Generator pings the DUT's ASIC to generate Compliance Patterns (CP0-CP15). Compliance Patterns (CP) are predetermined stress patterns consisting of sequence of logical 0s and 1s generated by a test pattern generator. The pinging by the Signal Generator is done by transmitting different Pseudo Random Binary Sequence (PRBS) to the ASIC. These signals inform the ASIC to generate a compliance pattern of specific frequency. For this experiment, CP9 PRBS pattern was used which has a frequency of 10 GHz.
2. Thereafter, the device transmitter (TX) sends these Compliance Patterns (CP9 for this experiment) to the Digital Signal Analyzer which works as the receiver (RX) for our experiment. The Digital Signal Analyzer analyses these signals and plot the received signal in

time domain and the eye-diagram. The required readings are taken from those plotted graphs and eye-diagrams thereafter.

3. For studying the effect of ISI on the received signal, an ISI channel board is used. The ISI channel board emulates a wide range of channel loss with Inter Symbol Interference (ISI) traces with fine resolution. It consists of traces of different lengths that can emulate different levels of noise in the channel. The ISI channel board is connected between the device transmitter (TX) and the Digital Signal Analyzer and then the worst-case effect of noise is observed on the signal at the receiver (RX) end.
4. The Digital Signal Analyzer also enables application of different equalization techniques which are practically applied during post-silicon validation. These equalization techniques can be applied individually or in a combination to open the eye in the eye-diagram enabling the receiver (RX) to interpret the signals in a better way.

## 6.4 Measurement Procedure

The following steps were performed during the experiment to take accurate measurements by ensuring minimum errors:

At first, the oscilloscope and the SMA cables were calibrated following the manufacturer's guideline in order to remove any offset voltages that are present in the cables and ensured that the oscilloscope is aware of the same and sets its voltage levels accordingly. By doing this the accuracy of the measurement was increased and errors in measurements were reduced.

1. Then the Signal generator was programmed to send pings to the DUT until the CP 9 pattern appeared on the oscilloscope monitor. Figure 6.3 Shows the input CP 9 signal, generated by the DUT.

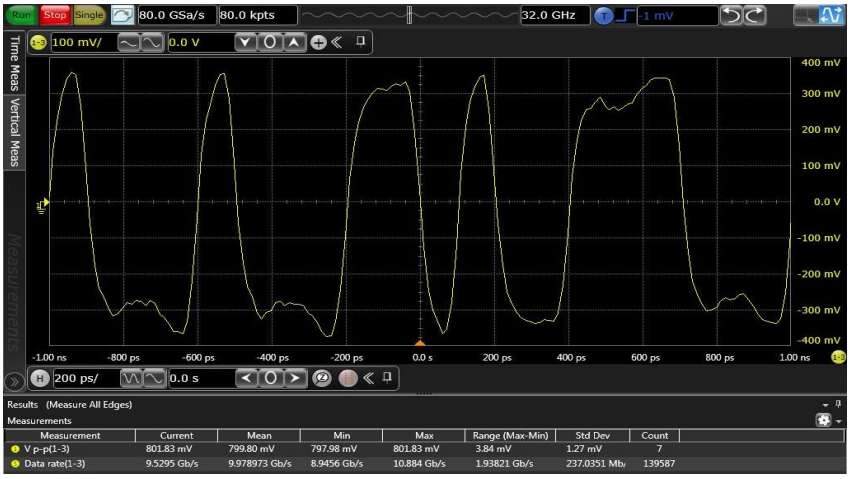


Fig. 6.3. CP9 signal generated by the DUT and sent via channel to the receiver (RX).

2. Then real time eye function was enabled on the oscilloscope and the waveform and eye-diagram of a lossless channel was observed and documented to have a reference of what a lossless line eye-diagram looks refer Figure 6.4. It should be noted that the peak-to-peak voltages ($V_{pp}$) present in all the observations were obtained by subtracting the differential signals in order to have a better Signal-to-Noise ratio, to obtain better data rates and to have clearer eye-diagrams.
3. Then to replicate the -10 dB noise physically, trace number 23 of ISI board was connected to the setup using SMA cables. One end of the trace was connected to the device transmitter (TX) (TX+ and TX-) and the other end of the trace was connected to the input channels 1 and 3 of the Oscilloscope which was emulating the receiver (RX) side of the communication setup. The trace of the ISI channel board emulates a practical high-speed channel with noise in it.
4. After connecting the ISI channel board, the noisy waveform is observed and the degraded eye-diagram carrying information about eye width and eye height were observed and documented.
5. Thereafter, different equalization techniques like CTLE, DFE, FFE, combination of CTLE and FFE and DFE and FFE were applied as a function on the Oscilloscope and their eye-diagrams and waveforms were captured and documented.
6. Steps 4 to 7 were repeated to observe effects of -14 dB loss too. The only difference was the connection in the ISI channel board. To emulate -14 dB loss practically, trace number 35 of ISI board was connected to the setup. One end of the trace was connected to the device transmitter (TX+ and TX-) and the other end of the trace was connected to the input channels 1 and 3 of the Oscilloscope which was emulating the receiver (RX) side of the communication setup.
7. Finally, based on the data on eye width, eye height, high frequency amplitude improvement (peak-to-peak voltage) a conclusion was made on which receiver (RX) equalization technique is the optimal one for obtaining better results during post-silicon receiver (RX) validation.

## 6.5 Observations and Results

In this section, the waveforms and the eye-diagrams that are observed during the experiments conducted are documented. Different equalization techniques and their combination were applied at the receivers where the channel was infused with -10 dB loss and -14dB loss and the time domain waveform and eye-diagrams were obtained which helped to compare and conclude as to which equalization technique or their combination is the optimum when it comes to product validation.

But before that, the behaviour of a loss less channel was also studied in order to have a reference as to how much can losses degrade a signal.

### 6.5.1 Behaviour of Channel with No Loss

Figure 6.4 shows the Time domain waveform and eye diagram of the signal travelling through a loss-less channel as observed at receiver (RX) end. It can be observed that the signal has a very good eye opening with the eye-width being 86.428 ps and eye height being 436.9 mV which means it has a good noise margin and provides good sampling budget. The peak-to-peak voltage ($V_{pp}$) of 821mV is also observed to be which proves the fact that the high frequency components have not being attenuated amplitude wise and there is no effect of ISI in the channel. It can also be observed that the waveforms are transitioning properly across the reference point of 0V which will enable the receiver to properly decode those signals as a binary '1' and '0'.

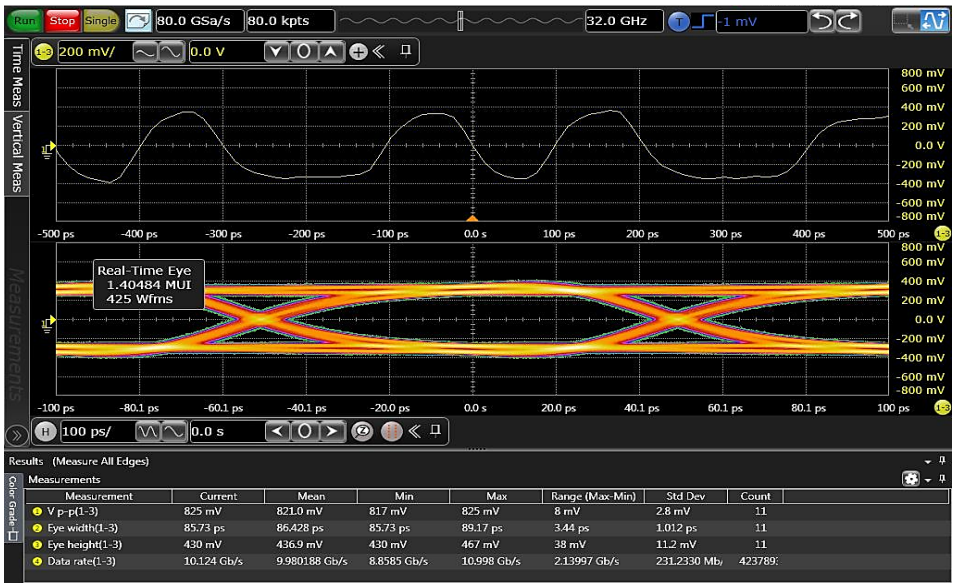


Fig. 6.4. Time domain waveform and eye diagram of the signal travelling through a loss-less channel as observed at receiver (RX) end.

### 6.5.2 CTLE Equalization at Receiver (RX) End

In this section the effect of applying CTLE equalization at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that were physically applied in the channel. The CTLE equalization was applied as a function at the end of the channel near the receiver's (RX) end.

- **Channel with -10dB loss:** When the ISI channel board was connected to the setup, and -10dB loss was physically emulated using the board, the eye-diagrams and amplitude of high

frequency signal ($V_{pp}$) both depleted drastically from what it was in the case of loss less channel (as shown in Figure 6.4). Thereafter, CTLE equalization technique was applied at the receiver end and the results were captured. Figure 6.5 and Figure 6.6 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when CTLE was applied as a function. The parameters and their obtained values are as follows:

a) **$V_{pp}$ before applying CTLE -** 590.37mV
b) **$V_{pp}$ after applying CTLE –** 622.26mV
c) **Eye width before applying CTLE-** 40.601ps
d) **Eye width after applying CTLE-** 69.063ps
e) **Eye height before applying CTLE-** 52.95mV
f) **Eye height after applying CTLE-** 209.80mV

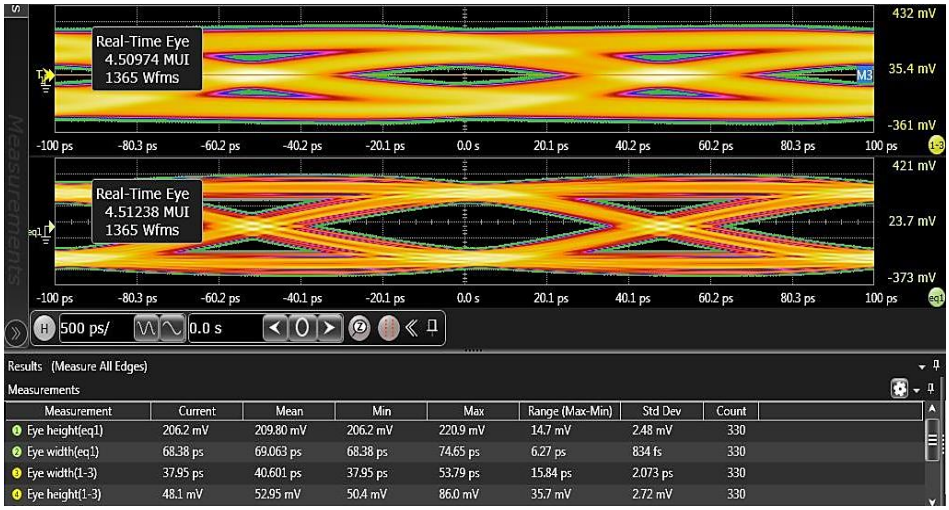


Fig. 6.5. Eye-diagrams observed before applying CTLE (top) and after applying CTLE (bottom) for -10dB channel loss.


Fig. 6.6. Time domain waveform observed before applying CTLE (in yellow) and after applying CTLE (in green) for -10dB channel loss.

- **Channel with -14dB loss:** On applying -14 dB loss on the channel, a full eye-diagram closure was observed with eye width and eye height both becoming 0. Also, a decrease in amplitude of the high frequency components of the signal was observed. On applying CTLE equalization, the eye width and eye height got improved and the eye opened a little. Figure 6.7 and Figure 6.8 shows the captured eye-diagram and time domain waveform. The parameters and their obtained values are as follows:
  a) **$V_{pp}$ before applying CTLE –** 567.26mV
  b) **$V_{pp}$ after applying CTLE –** 583.62mV
  c) **Eye width before applying CTLE-** 0.0s
  d) **Eye width after applying CTLE-** 72.321ps
  e) **Eye height before applying CTLE-** 0.0V
  f) **Eye height after applying CTLE-** 141.57mV

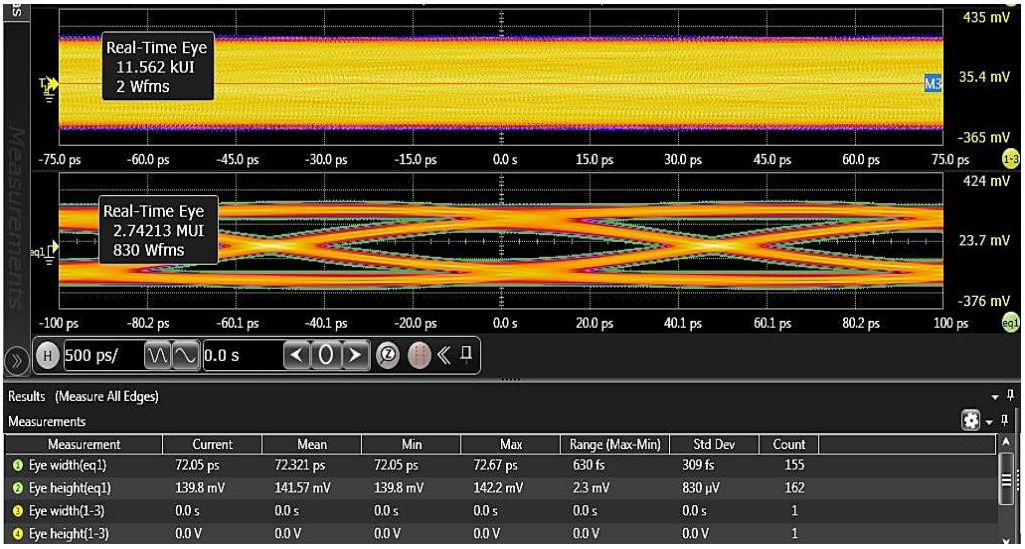


Fig. 6.7. Eye-diagrams observed before applying CTLE (top) and after applying CTLE (bottom) for -14dB channel loss.


Fig. 6.8. Time domain waveform observed before applying CTLE (in yellow) and after applying CTLE (in green) for -14dB channel loss.

### 6.5.3 FFE Equalization at Receiver (RX) End

In this section the effect of applying FFE equalization at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that were physically applied on the channel. The FFE was applied as a function at the end of the channel near the receiver's end results were captured.

- **Channel with -10dB loss:** Figure 6.9 and Figure 6.10 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when FFE equalization was applied as a function to counter -10dB loss applied on the channel. The parameters and their obtained values are as follows:
  a) **$V_{pp}$ before applying FFE –** 599.82
  b) **$V_{pp}$ after applying FFE –** 676.92
  c) **Eye width before applying FFE-** 39.139ps
  d) **Eye width after applying FFE-** 75.151ps
  e) **Eye height before applying FFE-** 53.33mV
  f) **Eye height after applying FFE-** 292.57mV

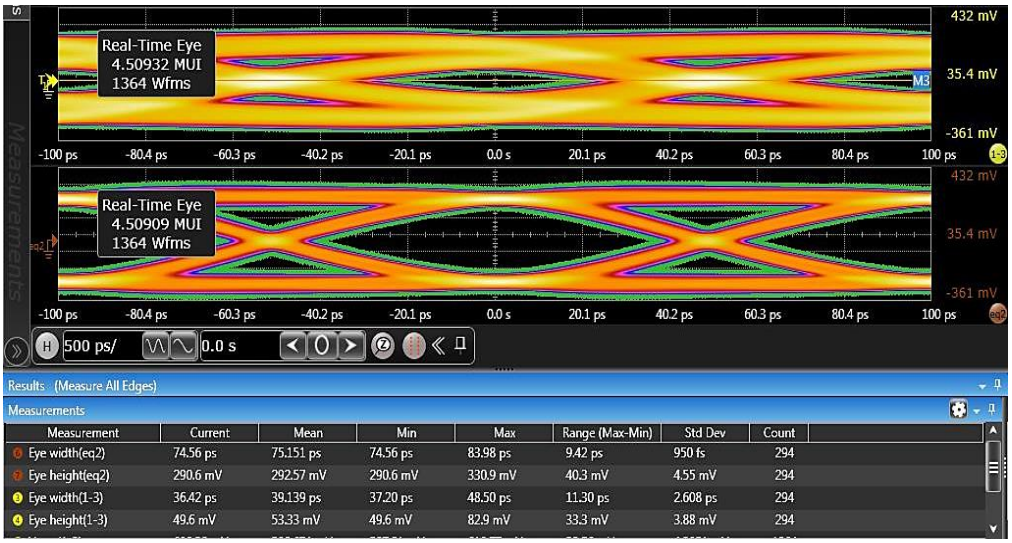


Fig. 6.9. Eye-diagrams observed before applying FFE (top) and after applying FFE (bottom) for -10dB channel loss.


Fig. 6.10. Time domain waveform observed before applying FFE (in yellow) and after applying FFE (in red) for -10dB channel loss.

- **Channel with -14dB loss:** Figure 6.11 and Figure 6.12 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when FFE equalization was applied as a function to counter the -14db loss applied on the channel. The parameters and their obtained values are as follows:

  a) **$V_{pp}$ before applying FFE –** 565.50mV
  b) **$V_{pp}$ after applying FFE –** 639.03mV
  c) **Eye width before applying FFE-** 0.0s
  d) **Eye width after applying FFE-** 71.10ps

**e) Eye height before applying FFE-** 0.0V

**f) Eye height after applying FFE-** 234.4mV

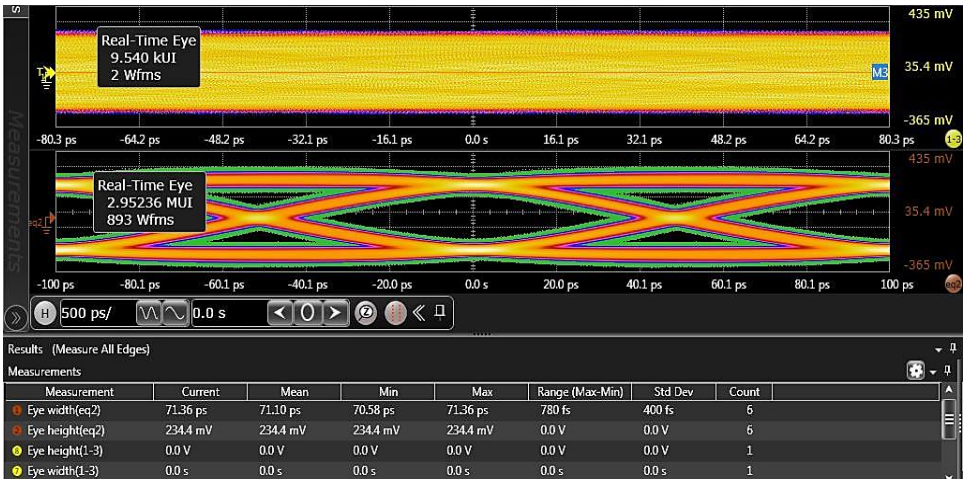


Fig. 6.11. Eye-diagrams observed before applying FFE (top) and after applying FFE (bottom) for -14dB channel loss.


Fig. 6.12. Time domain waveform observed before applying FFE (in yellow) and after applying FFE (in red) for -14dB channel loss.

## 6.5.4 DFE Equalization at Receiver (RX) End

In this section the effect of applying DFE equalization at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that were physically applied in the channel. The DFE was applied as a function at the end of the channel near the receiver's end.

- **Channel with -10dB loss:** Figure 6.13 and Figure 6.14 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when DFE equalization was applied as a

function to counter -10dB loss applied on the channel. The parameters and their obtained values are as follows:

a) **$V_{pp}$ before applying DFE** – 597.29mV
b) **$V_{pp}$ after applying DFE** – 545.56mV
c) **Eye width before applying DFE-** 40.651ps
d) **Eye width after applying DFE-** 72.780ps
e) **Eye height before applying DFE-** 55.06mV
f) **Eye height after applying DFE-** 165.45mV

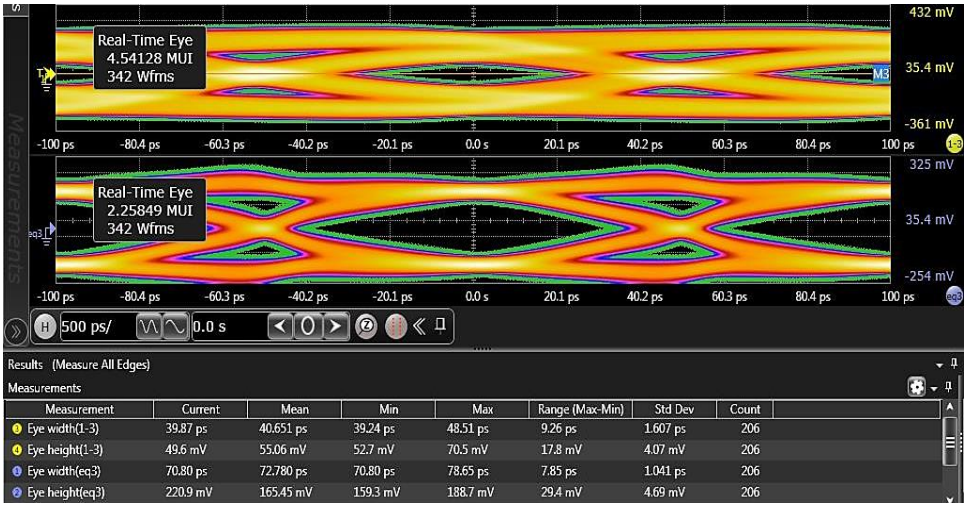


Fig. 6.13. Eye-diagrams observed before applying DFE (top) and after applying DFE (bottom) for -10dB channel loss.


Fig. 6.14. Time domain waveform observed before applying DFE (in yellow) and after applying DFE (in blue) for -10dB channel loss.

- **Channel with -14dB loss:** Figure 6.15 and Figure 6.16 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when DFE equalization was applied as a

function to counter the -14db loss applied on the channel. The parameters and their obtained values are as follows:

a) **$V_{pp}$ before applying DFE** – 568.92mV

b) **$V_{pp}$ after applying DFE** – 490.91mV

c) **Eye width before applying DFE-** 0.0s

d) **Eye width after applying DFE-** 50fs

e) **Eye height before applying DFE-** 0.0V

f) **Eye height after applying DFE-** 0.0V

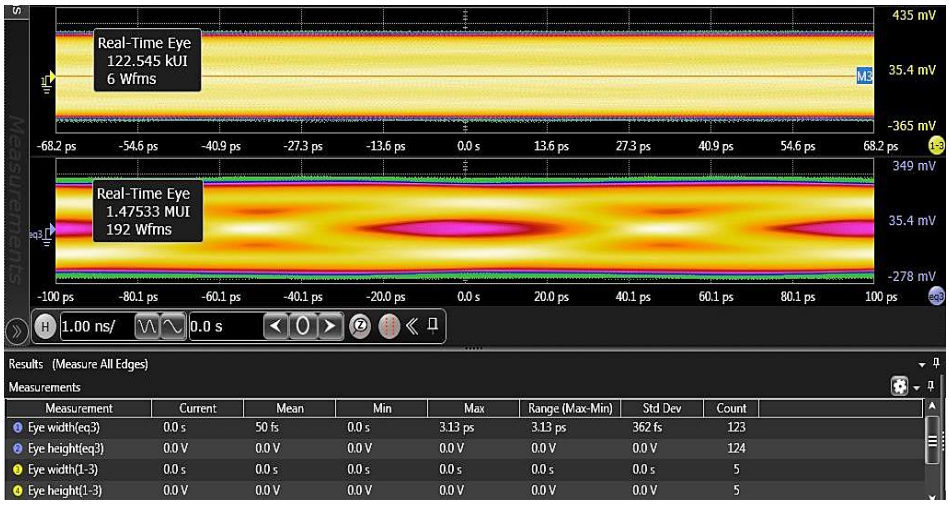


Fig. 6.15. Eye-diagrams observed before applying DFE (top) and after applying DFE (bottom) for -14dBchannel loss.

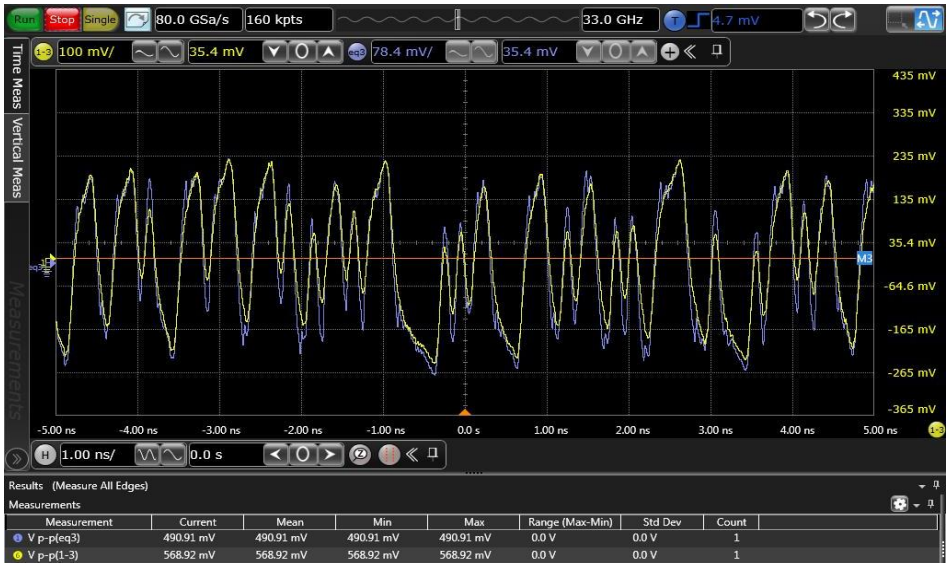


Fig. 6.16. Time domain waveform observed before applying DFE (in yellow) and after applying DFE (in blue) for -14dB channel loss.

### 6.5.5 CTLE & FFE Equalization at Receiver (RX) End

In this section the effect of applying CTLE & FFE equalizations together at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that are physically applied in the channel. The CTLE & FFE were applied together as a function on the same channel near the receiver's end.

- **Channel with -10dB loss:** Figure 6.17 and Figure 6.18 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when CTLE & FFE equalizations were applied together as a function to counter -10dB loss applied on the channel. The parameters and their obtained values are as follows:

**a)** **$V_{pp}$ before applying CTLE & FFE –** 595.79mV

**b)** **$V_{pp}$ after applying CTLE & FFE –** 658.92mV

**c)** **Eye width before applying CTLE & FFE –** 39.771ps

**d)** **Eye width after applying CTLE & FFE –** 68.191ps

**e)** **Eye height before applying CTLE & FFE –** 56.3mV

**f)** **Eye height after applying CTLE & FFE –** 209.37mV

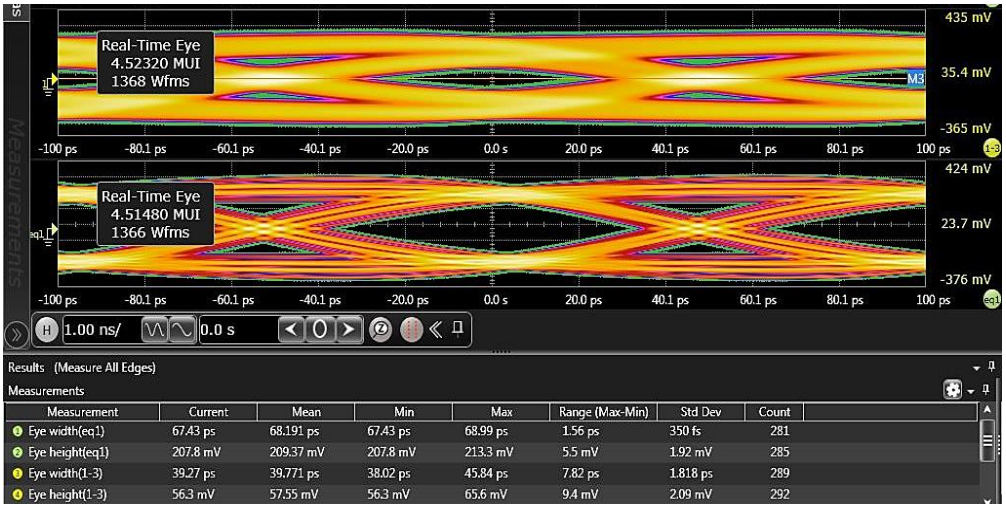


Fig. 6.17. Eye-diagrams observed before applying CTLE & FFE (top) and after applying CTLE & FFE (bottom) for -10dB channel loss.


Fig. 6.18. Time domain waveform observed before applying CTLE & FFE (in yellow) and after applying CTLE & FFE (in green) for -10dB channel loss.

- **Channel with -14dB loss:** Figure 6.19 and Figure 6.20 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when CTLE & FFE equalizations were applied together as a function to counter -14dB loss applied on the channel. The parameters and their obtained values are as follows:
    a) **$V_{pp}$ before applying CTLE & FFE –** 561.93mV
    b) **$V_{pp}$ after applying CTLE & FFE –** 605.47mV
    c) **Eye width before applying CTLE & FFE –** 0.0s
    d) **Eye width after applying CTLE & FFE –** 65.37ps
    e) **Eye height before applying CTLE & FFE –** 0.0mV
    f) **Eye height after applying CTLE & FFE –** 201.6mV

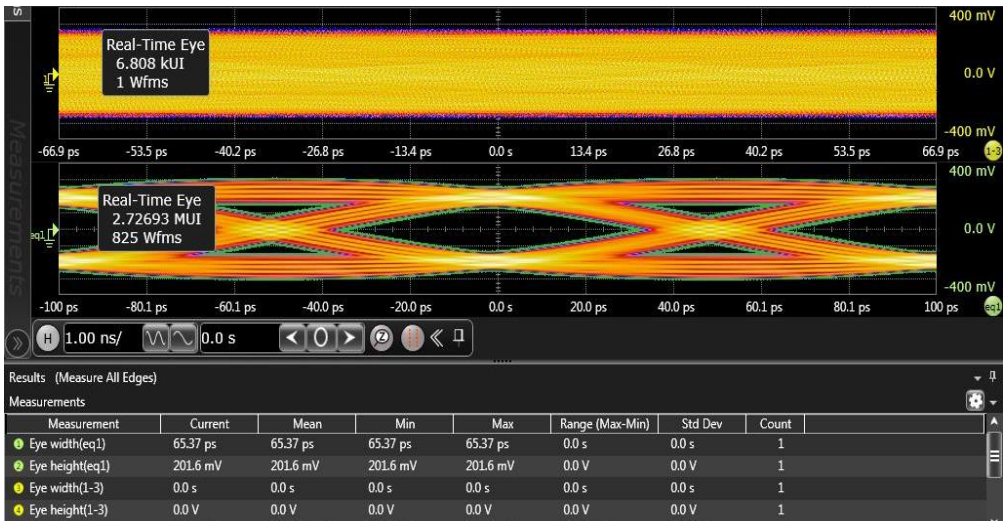


Fig. 6.19. Eye-diagrams observed before applying CTLE & FFE (top) and after applying CTLE & FFE (bottom) for -14dB channel loss.

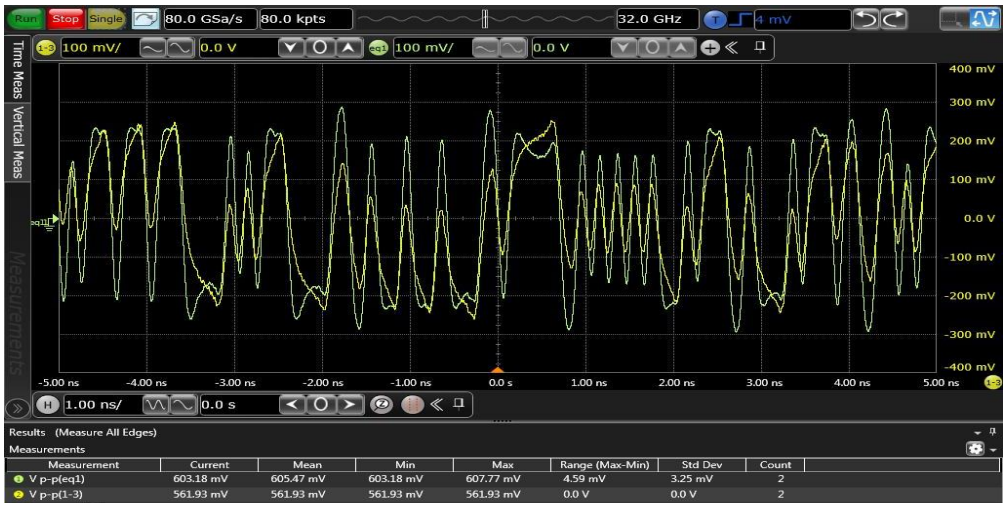


Fig. 6.20. Time domain waveform observed before applying CTLE & FFE (in yellow) and after applying CTLE & FFE (in green) for -14dB channel loss.

## 6.5.6 DFE & FFE Equalization at Receiver (RX) End

In this section the effect of applying DFE & FFE equalizations together at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that were physically applied in the channel. The FFE was applied as a function on one channel of the Oscilloscope and the output of FFE was the input of the DFE on another channel and overall output was the output of DFE.

- **Channel with -10dB loss:** Figure 6.21 and Figure 6.22 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when DFE & FFE equalizations were applied together as a function to counter -10dB loss applied on the channel. The parameters and their obtained values are as follows:
  a) **$V_{pp}$ before applying DFE & FFE –** 602.30mV
  b) **$V_{pp}$ after applying DFE & FFE –** 676.14mV
  c) **Eye width before applying DFE & FFE –** 39.029ps
  d) **Eye width after applying DFE & FFE –** 75.622ps
  e) **Eye height before applying DFE & FFE –** 54.16mV
  f) **Eye height after applying DFE & FFE –** 299.48mV

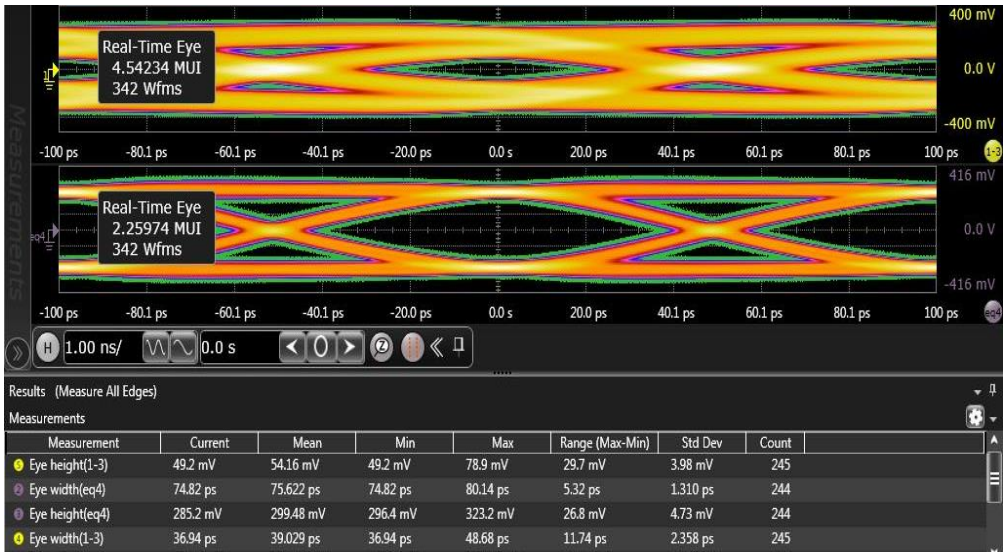


Fig. 6.21. Eye-diagrams observed before applying DFE & FFE (top) and after applying DFE & FFE (bottom) for -10dB channel loss.

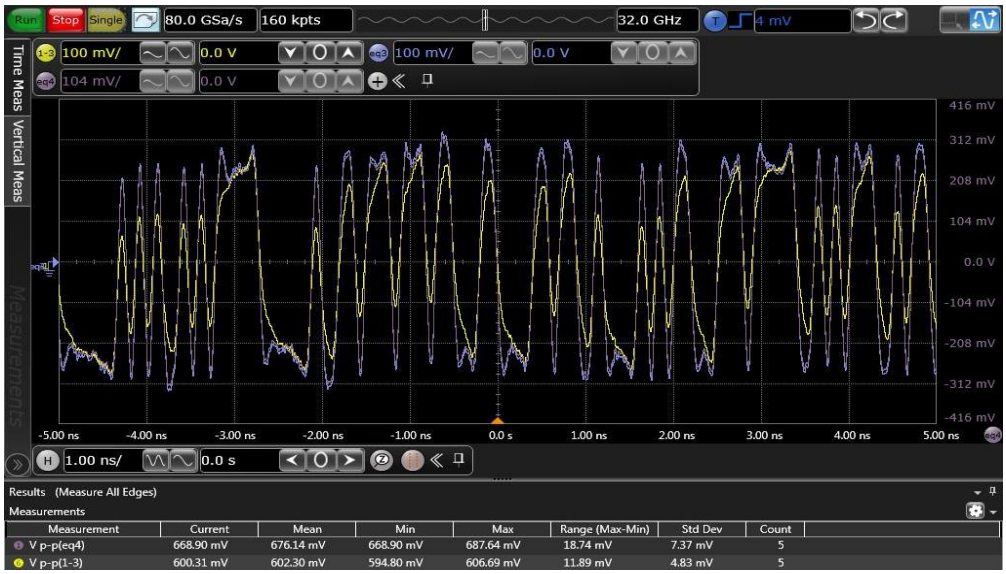


Fig. 6.22. Time domain waveform observed before applying DFE & FFE (in yellow) and after applying DFE & FFE (in purple) for -10dB channel loss.

- **Channel with -14dB loss:** Figure 6.23 and Figure 6.24 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when DFE & FFE equalizations were applied together as a function to counter -14dB loss applied on the channel. The parameters and their obtained values are as follows:
  - **a) $V_{pp}$ before applying DFE & FFE –** 569.50mV
  - **b) $V_{pp}$ after applying DFE & FFE –** 606.72mV
  - **c) Eye width before applying DFE & FFE –** 0.0ps
  - **d) Eye width after applying DFE & FFE –** 66.773ps

**e) Eye height before applying DFE & FFE –** 0.0V

**f) Eye height after applying DFE & FFE –** 172.19mV

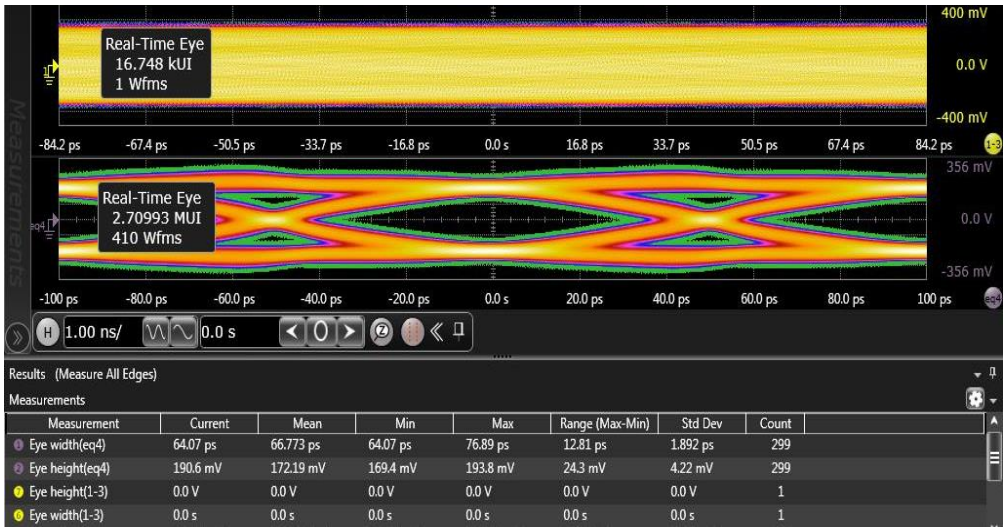


Fig. 6.23. Eye-diagrams observed before applying DFE & FFE (top) and after applying DFE & FFE (bottom) for -14dB channel loss.


Fig. 6.24. Time domain waveform observed before applying DFE & FFE (in yellow) and after applying DFE & FFE (in purple) for -14dB channel loss.

## 6.5.7 CTLE, FFE & DFE Equalization at Receiver (RX) End

In this section the effect of applying CTLE, FFE & DFE equalizations all together at the receiver (RX) end was observed. The readings were taken for both -10dB loss and -14dB loss that were physically applied in the channel. The CTLE and FFE were applied as a function on one channel together and the output of that channel was then fed as input to the DFE, and final equalized output was the output of DFE which was applied on another channel of Oscilloscope.

- **Channel with -10dB loss:** Figure 6.25 and Figure 6.26 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when CTLE, FFE & DFE equalizations were applied together as a function to counter -10dB loss applied on the channel. The parameters and their obtained values are as follows:
  a) **$V_{pp}$ before applying CTLE, FFE & DFE –** 602.58mV
  b) **$V_{pp}$ after applying CTLE, FFE & DFE –** 631.10mV
  c) **Eye width before applying CTLE, FFE & DFE –** 40.950ps
  d) **Eye width after applying CTLE, FFE & DFE –** 68.509ps
  e) **Eye height before applying CTLE, FFE & DFE –** 56.92mV
  f) **Eye height after applying CTLE, FFE & DFE –** 215.72mV

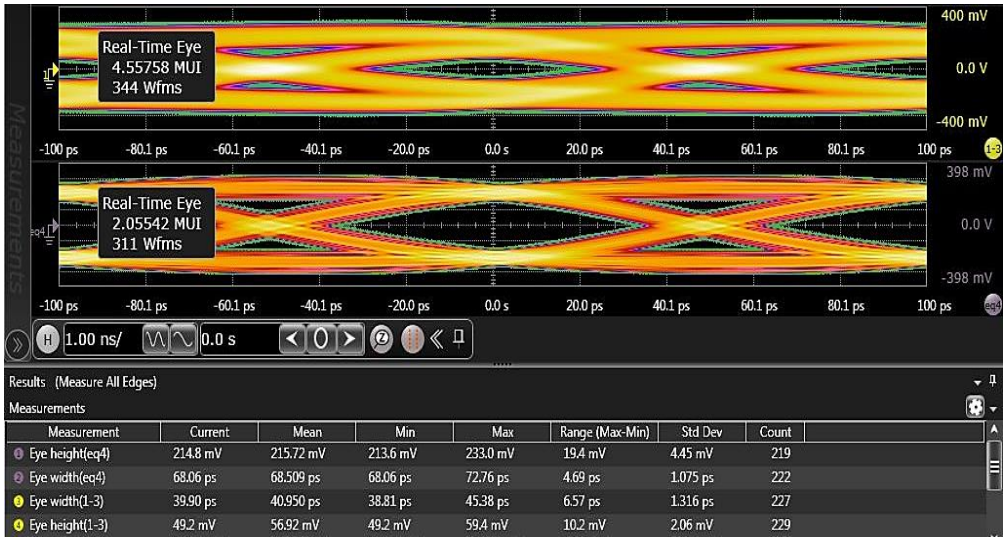


Fig. 6.25. Eye-diagrams observed before applying CTLE, FFE & DFE (top) and after applying CTLE, FFE & DFE (bottom) for -10dB channel loss.


Fig. 6.26. Time domain waveform observed before applying CTLE, FFE & DFE (in yellow) and after applying CTLE, FFE & DFE (in purple) for -10dB channel loss.

- **Channel with -14dB loss:** Figure 6.27 and Figure 6.28 shows the eye diagrams and time domain waveform obtained on the receiver (RX) end when CTLE, FFE & DFE equalizations were applied together as a function to counter -14dB loss applied on the channel. The parameters and their obtained values are as follows:
  a) **$V_{pp}$ before applying CTLE, FFE & DFE –** 573.131mV
  b) **$V_{pp}$ after applying CTLE, FFE & DFE –** 605.911mV
  c) **Eye width before applying CTLE, FFE & DFE –** 0.0ps
  d) **Eye width after applying CTLE, FFE & DFE –** 67.198ps
  e) **Eye height before applying CTLE, FFE & DFE –** 0.0V
  f) **Eye height after applying CTLE, FFE & DFE –** 204.39mV

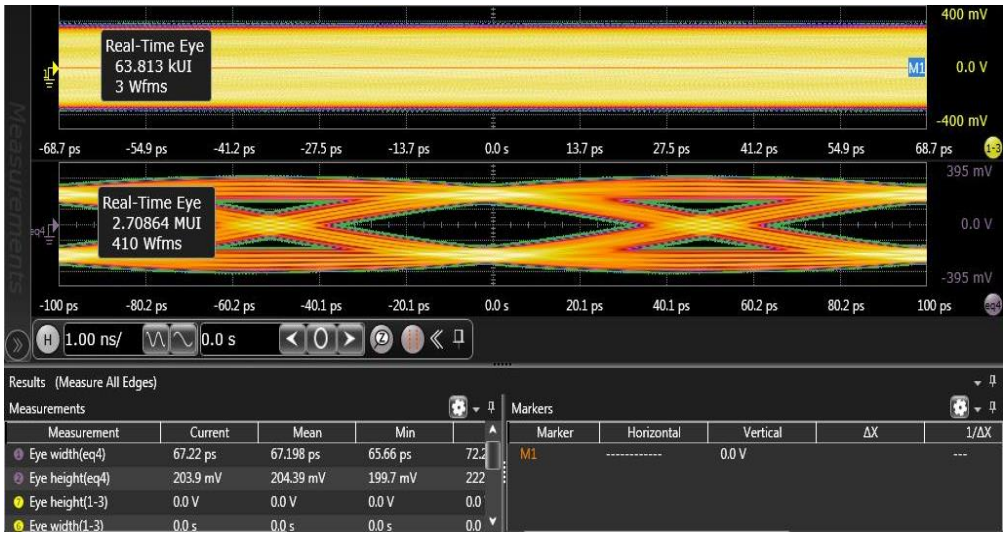


Fig. 6.27. Eye-diagrams observed before applying CTLE, FFE & DFE (top) and after applying CTLE, FFE & DFE (bottom) for -14dB channel loss.

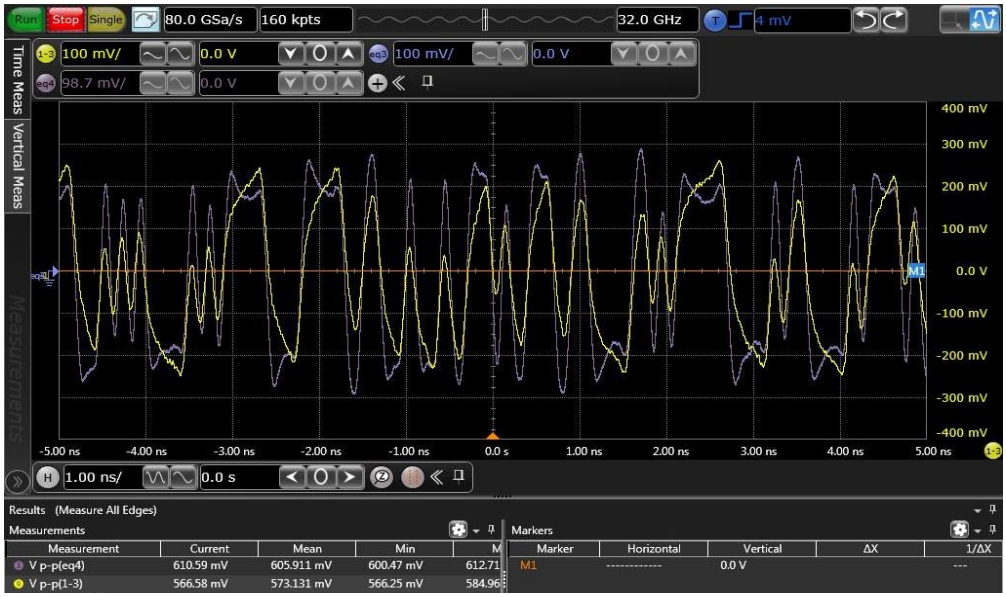


Fig. 6.28. Time domain waveform observed before applying CTLE, FFE & DFE (in yellow) and after applying CTLE, FFE & DFE (in purple) for -14dB channel loss.

## 6.6 Tabulation of Results

This section presents a carefully organized tabulation of experimental findings, aiming to establish a comparative analysis of various receiver (RX) equalization techniques' effectiveness in mitigating channel noises. The comparison focuses on two aspects: the improvement in the eye diagram's openness (represented by enhanced eye width and eye height) and the restoration of the degraded high-frequency component of the signal caused by channel impairments. Table 6.1 and Table 6.2 present the tabulated results for -10dB loss and -14dB loss respectively. In order to enhance comprehension of the impact made by each equalization technique, Figure 6.29 and Figure 6.30 illustrate graphical representations derived from table 6.1 and table 6.2, respectively.

To facilitate an easier comparison, the average values of Vpp, Eye Width (EW), and Eye Height (EH) were calculated for the scenario where no equalization was applied. Since these values were found to be within a similar range, an average value was computed for each parameter to enhance the comparison among all the values obtained when the equalization techniques were implemented.

Within Table 6.2, the comparison of the EW and EH parameters are conducted in terms of magnitude rather than percentage. This approach arises due to the observation that, at a channel loss of -14dB, the eye diagram experiences complete closure, leading to EW and EH values of 0. However, upon the application of equalization techniques, the eye significantly opens up. The reason behind resorting to magnitude comparison instead of utilizing a percentage change formula is the inherent limitation posed by having an initial value of 0. When attempting to calculate the percentage change with a starting value of 0, the computation becomes unattainable. Consequently, the magnitude of the values is employed as a means of comparing the extent of improvement achieved through equalization techniques.

Table 6.1. Observed values for each equalization technique applied on the -10dB loss infused channel and the percentage change they bring to improve the signal at receiver end.

| CHANNEL LOSS | EQUALIZATION TECHNIQUES | PARAMETERS | | | CHANGE IN PARAMETERS | | |
|---|---|---|---|---|---|---|---|
| | | $V_{pp}$(mV) | EW (ps) | EH (mV) | $V_{pp}$ (%) | EW (%) | EH (%) |
| -10 dB LOSS | NO EQUALIZATION APPLIED | 598.025 | 40.098 | 55.095 | 0 | 0 | 0 |
| | CTLE APPLIED AS A FUNCTION | 622.26 | 52.95 | 209.8 | 4.05 | 32.05 | 280.8 |
| | FFE APPLIED AS A FUNCTION | 676.92 | 75.151 | 292.57 | 13.19 | 87.42 | 431.03 |
| | DFE APPLIED AS A FUNCTION | 545.56 | 70.8 | 165.45 | -8.77 | 76.57 | 200.3 |
| | CTLE + DFE APPLIED AS FUNCTIONS | 658.92 | 68.191 | 209.37 | 10.18 | 70.06 | 280.02 |
| | **DFE + FFE APPLIED AS FUNCTIONS** | **676.14** | **76.188** | **299.48** | **13.06** | **90** | **443.57** |
| | CTLE+FFE+DFE APPLIED AS FUNCTIONS | 631.1 | 68.509 | 213.6 | 5.53 | 70.85 | 287.69 |

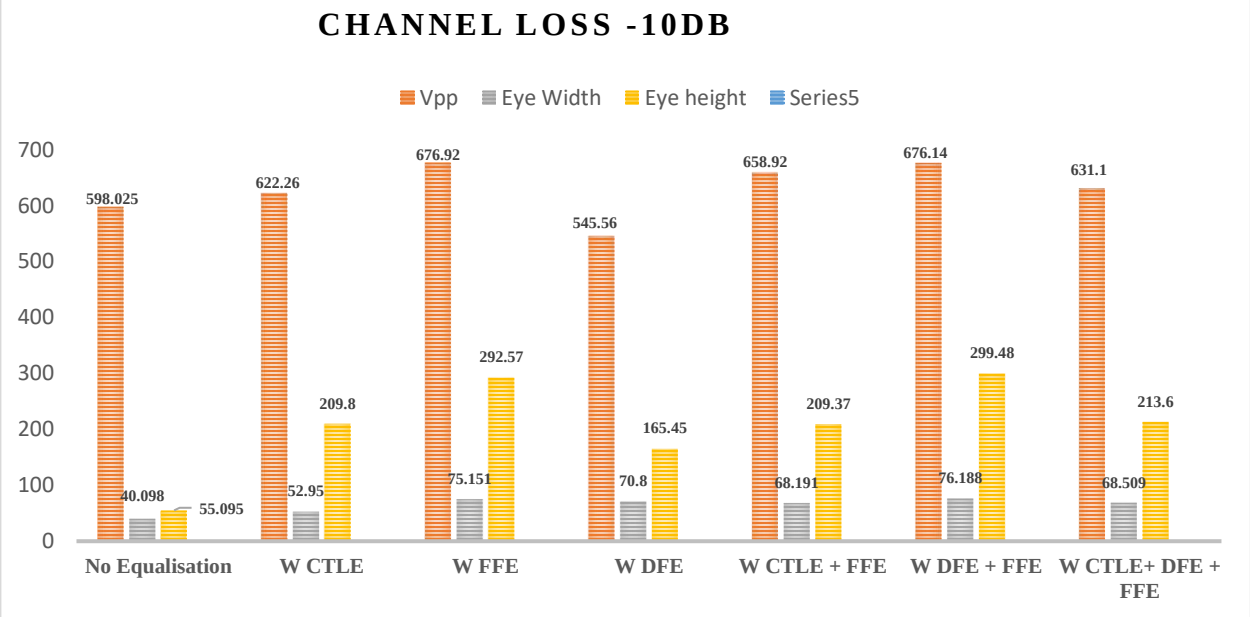


Fig. 6.29. Graph plotted using the data collected from table 6.1.

Table 6.2. Observed values for each equalization technique applied on the -14dB loss infused channel and the percentage change they bring to improve the signal at receiver end.

| CHANNEL LOSS | EQUALIZATION TECHNIQUES | PARAMETERS | | | CHANGE IN PARAMETERS | | |
|---|---|---|---|---|---|---|---|
| | | Vpp (mV) | EW (ps) | EH (mV) | Vpp (in %) | \|EW\| | \|EH\| |
| -14 dB LOSS | NO EQUALIZATION APPLIED | 567.7068 | 0 | 0 | 0 | 0 | 0 |
| | CTLE APPLIED AS A FUNCTION | 583.62 | 72.321 | 141.57 | 2.802487 | 72.321 | 141.57 |
| | **FFE APPLIED AS A FUNCTION** | **639.03** | **71.1** | **234.34** | **12.56275** | **71.1** | **234.34** |
| | DFE APPLIED AS A FUNCTION | 490.91 | 0.05 | 0 | -13.52803 | 0.05 | 0 |
| | CTLE + DFE APPLIED AS FUNCTIONS | 605.47 | 65.37 | 201.6 | 6.651283 | 65.37 | 201.6 |
| | DFE + FFE APPLIED AS FUNCTIONS | 606.72 | 66.773 | 172.19 | 6.871466 | 66.773 | 172.19 |
| | CTLE+FFE+DFE APPLIED AS FUNCTIONS | 605.911 | 67.198 | 204.39 | 6.728964 | 67.198 | 204.39 |

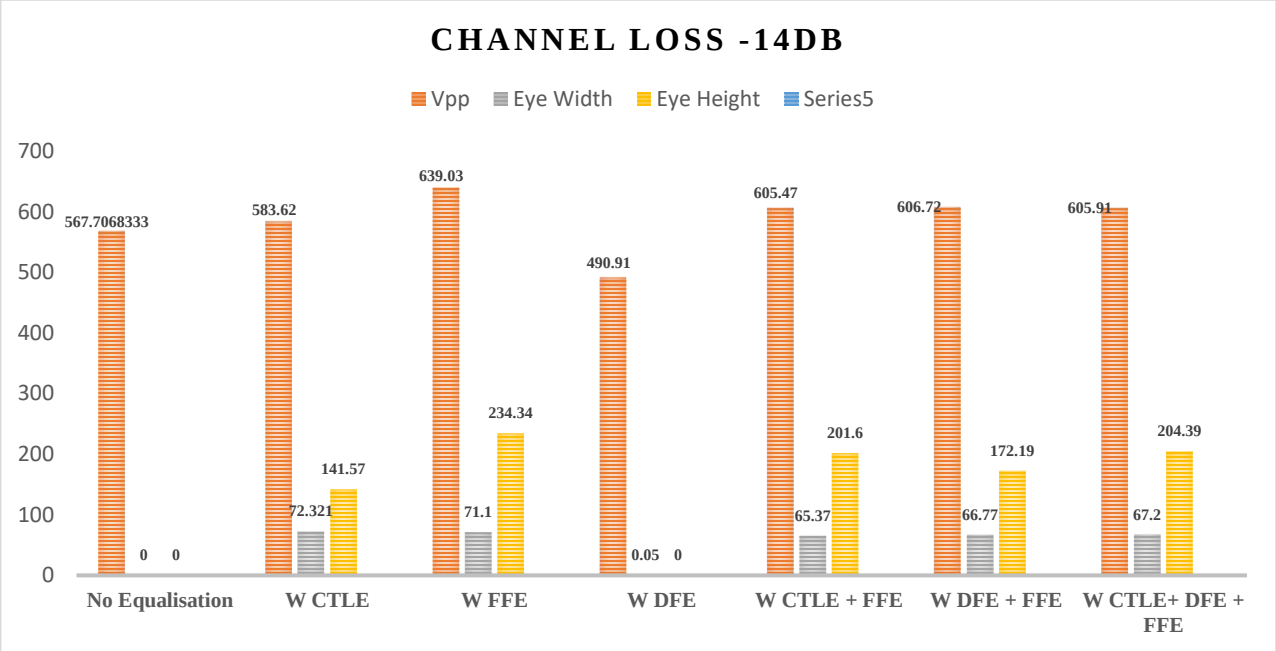


Fig. 6.30. Graph plotted using the data collected from table 6.2.

# Chapter 7

# Conclusion and Future Works

## 7.1 Conclusion

In conclusion, this thesis aimed to evaluate and compare different receiver (RX) equalization techniques used for post silicon validation of USB 3.2 devices, focusing on three key performance metrics: eye width, eye height, and signal amplitude. By conducting experiments and analyzing the results, valuable insights were obtained regarding the effectiveness of these techniques in mitigating channel noises and improving the overall signal quality.

The findings showcased that the implemented equalization techniques played a vital role in enhancing the eye diagram's openness, as demonstrated by an increase in both eye width and eye height. This improvement is particularly significant in the context of USB 3.2 devices, where maintaining a robust and reliable communication channel is crucial. The larger eye width and eye height indicate a greater tolerance to noise and interferences, thereby ensuring more reliable data transmission.

Furthermore, the analysis also considered the impact of equalization techniques on the amplitude of the high-frequency component of the signal, which often experiences degradation due to Channel Impairments. The results revealed notable improvements in signal amplitude when equalization techniques were applied. This signifies the ability of these techniques to effectively combat ISI and restore the integrity of the signal, thus minimizing data errors and improving the overall transmission performance.

Upon careful analysis and comparison of the tabulated data, a clear pattern emerged, highlighting the superior performance of specific receiver equalization techniques for the USB 3.2 device tested. Specifically, the combination of Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE) proved to be the most effective choice when evaluating eye width, eye height, and signal amplitude in the -10dB loss scenario. On the other hand, when confronted with a more challenging channel loss of -14dB, the Feed Forward Equalization (FFE) technique alone showcased exceptional performance.

These findings hold significant implications for practical implementations of receiver equalization techniques, particularly in cases where area constraints are a key consideration. In such instances, the Feed Forward Equalization (FFE) technique emerges as an ideal option for both -10dB and -14dB channel loss scenarios. Moreover, this technique demonstrates versatility, as it can

effectively handle practical noise levels ranging from 3.7dB (representing the minimum expected noise in a practical channel) to the maximum possible noise level of -14dB in a practical channel.

By selecting the appropriate receiver equalization technique based on the specific requirements and limitations of the implementation, designers and engineers can optimize the performance of USB 3.2 communication systems. These findings provide valuable guidance for practical application and underline the importance of tailoring equalization techniques to match the noise characteristics and constraints of the given scenario.

## 7.2 Future Works

In the realm of constantly evolving high-speed serial link architecture, the quest for superior and optimized equalization techniques becomes an undeniable necessity. In the days ahead, several advancements are anticipated to play a pivotal role in meeting these needs.

- Pioneering research studies, such as the one referenced as [35], propose the implementation of a neural equalizer as a potential solution that outshines traditional conversational equalizers in terms of performance. Similarly, [61] introduces an adaptive neural network-based equalizer, paving the way for Artificial Intelligence (AI)-driven equalization techniques that have the potential to revolutionize the validation process for USB devices.
- Additionally, groundbreaking research endeavors, such as the work mentioned in [28], unveil a captivating design showcasing a 7-tap 40 Gb/s feed forward equalizer (FFE). This design exhibits promising results, vowing to enhance eye width and eye height. Furthermore, the research study referenced as [33] introduces a compelling design that combines a continuous-time linear equalizer with a two-tap half-rate/quarter-rate decision-feedback equalizer, ingeniously utilizing charge steering techniques to curtail power consumption. These studies illustrate the potential for future advancements in equalization techniques, either through architectural changes to existing approaches or through the synergistic integration of different available equalization techniques. Such innovations hold the promise of augmenting the validation experience in near future.
- Advancements in AI-driven equalization techniques and research breakthroughs inspire a paradigm shift in optimizing and validating high-speed seril link architectures, elevating the validation process for USB devices to new heights. These innovations enhance performance, reliability, and pave the way for future data communication advancements.

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