Quantum Analytical Modeling of Ultra-Scaled Double-Gate (DG) MOSFET Structure and Explore its Applications

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BY

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This to certify that the thesis entitled **"Quantum analytical modeling of ultra-scaled double-gate (DG) MOSFET structure and explore its applications."** has been carried out by **TYAJODEEP CHAKRABARTI** (**Examination Roll No.: M6VLS22008, Class Roll No.: 001910703008** and **Registration No: 150136 of 2019-20**) under my guidance and supervision and be accepted in partial fulfilment of the requirement for the degree of Master of Technology in VLSI Design and Microelectronics Technology. In my opinion the work fulfils the requirement for which it is submitted. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other organization.

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ABSTRACT

As an ineluctable effect of persistent dimensional scaling of transistors, various short-channel effects have become serious challenge for further miniaturization of device dimensions in semiconductor industry. The scenario becomes more complicated as the 'quantum confinement effects' emerge as an integral part of device characteristics when the 'channel length' is dwindled to deep submicron region. Amongst many other proposed structures in sub-nanometer regime, multiple-gate MOSFET structure have proved to be attractive options because of their inherent immunity to 'short channel effects' (SCE), improved subthreshold characteristics and enhanced current driving capability. Likewise, Double gate MOSFET provides enhanced mobility, better I_{on}/I_{off} ratio and improved sub-threshold slope due to volume inversion of charge in the channel. In 'Double Gate (DG) MOSFET' structure, the vertical field is modified by incorporating dual materials with different work functions in gate, providing a step in potential profile and resulting in enhancement of performance.

In this work, the quantum analytical model of DG MOSFET, based on the self-consistent solution of 1-D Schrodinger equation and 2-D Poisson's equation, for the ultra-scaled 'double-gate (DG) MOSFET' structure is proposed. The quantum mechanical effects have been included in our model to derive the analytical surface potential along the channel and expressions for the electric field. Extensive calculations have been carried out to analyse the quantum mechanical effects on other crucial device performance parameters like: **threshold voltage**, **subthreshold slope,** $\mathbf{I_{ON}/I_{off}}$ for which result obtained are 0.25V, 66 mV/decade, 155521381.315996 respectively.

The two types of MOSFET transistors are fabricated in virtual fabrication lab that is Silvaco Atlas. The fabricated MOSFETs are p-MOS and n-MOS. In both the MOSFET, the two GATEs are considered, which are normally called as 'DG-MOSFET'. The GATEs are made of polysilicon. The source and drain are made of silicon with the length of 15nm each. The doping is done with p type material, Boron in these sources and drain. The source and drain concentrations are 1e20 and 1e18 respectively. The channel concentration is 1e15 and the length is considered 30nm. In this unique structure we use the two layers of Silicon-germanium (SiGe) in the top and bottom of the channel, with the doping concentration of 1e17. Silicon-germanium enables faster and more efficient manufacturing of devices using smaller, less noisy circuits. This Silicon-germanium is commonly used in heterojunction bipolar transistor or in CMOS transistor

for better performance, which has motivated to use in this new novel structure. All the lengths are optimized to get the best possible result. The best solutions are taken in this structure.

Furthermore, a comparative analysis based on the drain current has been presented in this work for the classical as well as for the quantum model. The superiority of this proposed quantum model for the DGMOS structure is verified by the comparison of the results obtained from other device structures.

As an application part, the proposed structure is applied and used for Boolean implementation as **AND gate** and as an **Inverter**. Thus, universal NAND gate can be obtained. Area scaling is a huge issue in today's VLSI industry. In normal scenario, to construct AND gate 6 transistors are required, using the proposed structure it is seen that only 1 PMOS structure exhibits the function of AND, thus giving a huge boost to the number of devices per die and hence in the VLSI technology. In the future scope of work, it can be examined whether the problems that is generally faced in deep sub- micron technology such as supply voltage scaling, short channel effects can be limited due to the mentioned advantages of DGMOSFET.

CHAPTER 1

INTRODUCTION AND ORGANIZATION OF THE THESIS

- Introduction and Motivation of the Present Research
- Technological Limitations for Further Miniaturization
- Working Principal of DGMOSFET
- Thesis Organization

1.1 INTRODUCTION AND MOTIVATION

Introduction:

The smaller device size explorations are the demand of future world. The researchers are involved to explore more and more, smaller handy gadgets, more faster and efficient processors which lead to exploration into the regime of nano scale MOSFETs. The microelectronics semiconductor industry is doing the miniaturization of devices along with the better performance of devices to incorporate the more and more devices in a chip following the Moore's Law. The MOSFET devices are the paramount of VLSI high density integrated circuits. The conventional CMOS in nanometer regime endures from short channel effect (SCE) [1-3] when the 'channel length' of the CMOS becomes the same order of source and drain depletion region. In this condition, the control of gate over the channel characteristics reduces significantly at higher drain bias. Owing to the fact that dimensional scaling of CMOS will eventually approach

fundamental limits, several new alternative structures are being explored in order to sustain the historical integrated circuit scaling. To eliminate the adverse effects in ultra-scaled MOSFET, multiple gate MOSFET structures were introduced.

Down scaling of electronic devices specially MOSFETs in the nano- regime improves device performance, with some constrictions. Due to reduction in size, supply voltage, at drain and gate have also been reduced proportionately [1-5].

1.2 Technological Limitations for Further Miniaturization

With the invention of transistor by John Bardeen, William Shockley and Walter Brattain at the Bell Telephone Laboratories in 1947, a huge mile stone was established for electronics industry. That route has run through the era of LSI (Large–Scale–Integration), VLSI (Very–Large–Scale–Integration) and ULSI (Ultra–Large–Scale–Integration) to fulfill the unappeasable demand of faster, smaller and cheaper electronic devices. Continuous downscaling has made this advancement possible and preserved the Moore's Law. But now, the silicon industry has reached at a cross-road as further progress in conventional CMOS device is obstructed due to a series of challenges [5-9].

With the diminution of channel length, control of gate over the channel weakens due to enhanced proximity between source and drain. As a consequence, Short–Channel–Effects (SCEs) become major problems associated with scaled MOSFETs when the channel length is shrunk to the order of source and drain depletion-layer width. SCEs lead to several reliability issues as the basic device parameters (such as threshold voltage), become dependent on channel length. SCEs subjugate the controllability of the gate voltage over potential distribution in the channel and drain current, leading to reduction of the subthreshold slope and increment of drain off-current. This degradation is attributed to charge sharing by the drain and gate electric fields

in the channel depletion layer as indicated by Poon and Yau's model, which is reported as the first SCE model [4]. Besides, scattering of gate length that is produced during the fabrication process of such small structure, results the diversion of device characteristics. These short-channel effects are mainly ascribed to two physical phenomena [7-11]:

1. Limitation on drift characteristics of electron in the channel.

2. Modification of the threshold voltage due to the shortening channel length.

Five distinct short-channel effects which are considered in particular are:

1. Drain-induced barrier lowering
2. Threshold voltage roll off,
3. Surface scattering,
4. Velocity saturation and
5. Hot electron effect

1.3: How the Field Effect Transistor Works

In the field effect transistor, an electric field is created by a weak electric signal at the bottom of the transistor which is further passed to the other parts of the field effect transistor. The bottom of the transistor is topped off with overabundance of electrons. In the focal or the base locale, the tally of the electrons is excessively less when contrasted with the base piece of the semiconductor. There are different sides discovered, that are known as the source and the channel. The source side is the area structure where the electrons enter inside and also on the other locale, channel, the electrons empty out. Ordinarily the progression of electrons is produced using one side to the next. The flow of current isn't stamped near the base locale. The flow of current is encouraged by a slight channel along the other area. To the base of the semi

conductor, an electrode is connected or joined. A dainty layer of metal oxide isolates this electrode from the rest part. Most normal weighty metal oxide utilized is the silicon dioxide. The terminal is regularly tended to as 'the door'. The gate is where we pass the weak electrical signal into the semiconductor. Because of the appalling activity of the electrons, a depletion zone gets framed at the base district. Passing negative charge will help in totally forestalling the section of power through the semiconductor. In light of the charge gave to the semiconductor, the current moving through the other district can be either more modest or bigger. As there is another voltage associated with it, there are potential approaches to additional make it bigger. The field effect transistors or FET are usually utilized in electrical gadgets like receivers, miniature wave stoves, TVs, radios and surprisingly in vehicles. They have a wide application as charge transporter gadgets. Despite the fact that there are numerous other semiconductors accessible, silicon serves the best to be utilized in field effect transistors [9-14].

1.4 ORGANIZATION OF THE THESIS

My innovative research work has been outlined in ‘five chapters’ including the **1st Chapter** where the Introduction of this work is narrated. In this Introduction Chapter it is illustrated about the ‘Nanoscale DG-MOSFETs’.

In **Chapter 2** an introduction of nanoscale DGMOS devices and their physics is described. The basic, fundamentals, of these devices and brief idea of DG MOSFETs and design and optimization of p-MOS and n-MOS comprising of double source is illustrated. Considering the parameters like doping concentration, work function and channel length the new novel structure of MOSFET is fabricated and characterized.

Chapter 3 has described the analytical model of DGMOSFET and the response graphs are plotted. The conduction current, Electric Field, Energy Band diagram, Current lines, Current

Density, Mobility, Surface Potential, I_d vs. V_{GS} curve, Threshold Voltage, Subthreshold slope, I_{OFF}, I_{ON} and the ratio of I_{ON}/I_{OFF} is illustrated.

In **4th Chapter**, the application of p-MOS as logic circuits of AND gate and Universal NAND gate is illustrated. The transistor level AND gate and NAND gate is realized and observed the advantages over conventional gates area and less number of transistors.

In the **5th chapter**, conclusion of works which are carried out in this 'research work' is described with a summary. The future scope of works on the new novel structure of n-MOS are discussed which can be the extension of this 'research work' in forthcoming time.

In the **6th Chapter** the relevant references are expressed.

CHAPTER 2

Design and Optimization of DG MOSFET, p-MOS and n-MOS Fabrication

2.1. Introduction

CMOS technology has witnessed continuous scaling following the prescripts of Moore's law, thus contributing to the advancement of technology [1] . However, in recent times, this trend has been slowed and is threatened for deep submicron region because below that quantum tunneling effect arises which correspondingly distract the device performance [2]. The microelectronics industry is thus researching for new alternate device structures to enable continued device miniaturization. Researchers have proposed several substitutes to traditional MOS to overcome the problems of associated short channel effects (SCEs) [3-5]. Gate work function engineering, lateral channel engineering, multi gate geometry, hetero dielectric-based Silicon on Insulator /Silicon On Nothing (SOI/SON) FET and Tunneling FETs are some of the emerging contenders that have shown admirable performance as compared to short channel MOSFET. Reconfigurable FETs (RFETs), stands as another interesting option to reduce the number of devices in future circuit because of its reprogrammable operation. The unique feature of switching from MOSFET to TFET and vice versa with the application of appropriate gate voltage makes it highly preferable in device research community with a possible choice to replace fin-shaped FETs, SOI/SON and other planner devices for future generation VLSI circuits. By allowing the same device to behave as MOSFET and TFET, such RFET devices facilitate the implementation of multiple functionalities with a single device rather than reducing the size of the transistor itself, a substitution to classic trend of downscaling.

In this work, a novel dual source quad gate (DS-TG) FET using electrostatically induced reconfigurability property has been proposed, that has capability of providing high drive current (in MOSFET configuration) and low leakage current (in TFET configuration). In the proposed device, DGMOSFET has low off state current of order 10^{12} A/μm and MOSFET has Ion/Ioff ratio of order 10^{6}. Moreover, use of dual source configuration provides higher on current with smaller turn on voltage. For the present device, DGMOSFET technology has been used which makes it immune towards device cross talk with lower junction leakage, increased radiation hardness, and full dielectric isolation of the transistor. Impact of varying parameters including channel doping concentration, distance between the source and drain, work function of gate metals and gate oxide thickness has been investigated on device electrostatics and its reconfigurable property to obtain the optimum device functionality.

2.2 **Working principle of MOSFET**:

It is fabricated by the oxidation of silicon substrates. It works by altering the width of the channel through which the movement of charge carriers (electrons for N-channel and holes for P-channel) occurs from source to drain. The gate terminal is insulated whose voltage regulates the conductivity of the device.

In general, the MOSFET functions as a switch, the MOSFET controls the voltage and current stream between the source and channel. The working of the MOSFET relies upon the MOS capacitor, which is the semiconductor surface beneath the oxide layers between the source and channel terminal. It very well may be rearranged from p-type to n-type, essentially by applying positive or negative gate voltage separately.

At the point when a drain to source voltage (VDS) is associated between the channel and source, a positive voltage is applied to the Channel, and the negative voltage is applied to the Source. Here the PN junction at the channel is converse one-sided and the PN intersection at the

Source is forward one-sided. At this stage, there won't be any current flow between the drain and the source.

If we apply a positive voltage (VGG) to the gate terminal, because of electrostatic attraction the minority charge carriers (electrons) in the P substrate will begin to accumulate on the gate contact which frames a conductive scaffold between the two n+ regions. The number of free electrons gathered at the door contact relies upon the strength of positive voltage applied. The higher the applied voltage more noteworthy the width of the n-channel shaped because of electron collection, this in the end builds the conductivity and the drain current (ID) will begin to stream between the Source and Channel. When there is no voltage applied to the entryway terminal, there won't be any current stream separated from a modest quantity of current because of minority charge transporters. The minimum voltage at which the MOSFET begins leading is known as the threshold voltage [4-7].

2.2.1. Types of MOSFET:

On the basis of Operational Mode, MOSFETs can be classified into two types.

- Enhancement Type MOSFETs
- Depletion Type MOSFETs

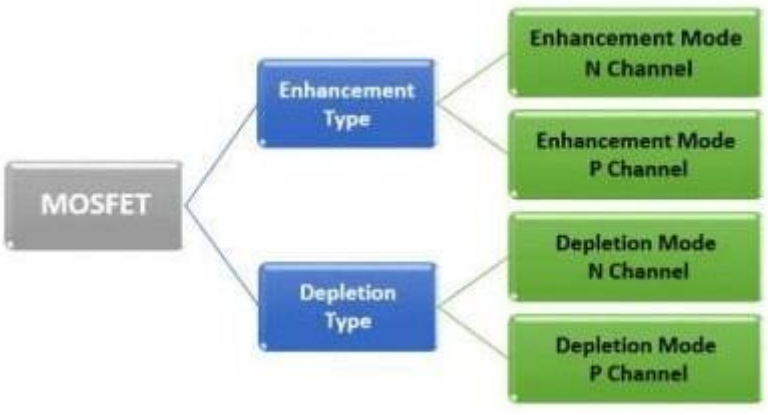

Fig 2.1. Types of MOSFET [4]

2.2.2. Enhancement Type MOSFET

In this mode, there is no conduction at zero voltage which suggests it is shut or "OFF" as a matter of course as there is no current channel. At the point when the gate voltage is expanded more than the source voltage, the charge carriers (holes) move away abandoning the electrons and along these lines a more wider channel is established. The gate voltage is directly proportional to the current i.e. as the gate voltage increases the current increases and vice versa.

2.2.2.1. Types of Enhancement MOSFETs

The Enhancement MOSFETs can be classified into two types depending upon the type of doped substrate (n-type or p-type) used.

- N Channel Enhancement Type MOSFETs
- P Channel Enhancement Type MOSFETs

2.2.3. Operation of MOSFET in Depletion Mode: The operation of MOSFET in depletion mode is same as the operation of the closed switch, it will begin to conduct just if the positive voltage (+VGS) is applied to the gate terminal and the drain current begins to move through the device. The channel width and drain current will increase when the bias 25 voltage increments. In any case, if the applied bias voltage is zero or negative the transistor will stay in the OFF state itself.

2.2.3. VI Characteristics:

VI characteristics of the depletion-mode MOSFET are drawn between the drain current (ID) and the drain-source voltage (VDS). The VI characteristics are divided into three distinct regions, such as ohmic, saturation, and cut-off regions. The cutoff region is the region where the MOSFET will be in the OFF state where the applied bias voltage is zero. At the point when the

bias voltage is applied, the MOSFET gradually moves towards conduction mode, and the slow increase in conductivity happens in the ohmic region. At last, the saturation region is the place where the positive voltage is applied continually and the MOSFET will remain in the conduction state [4-5,15-18].

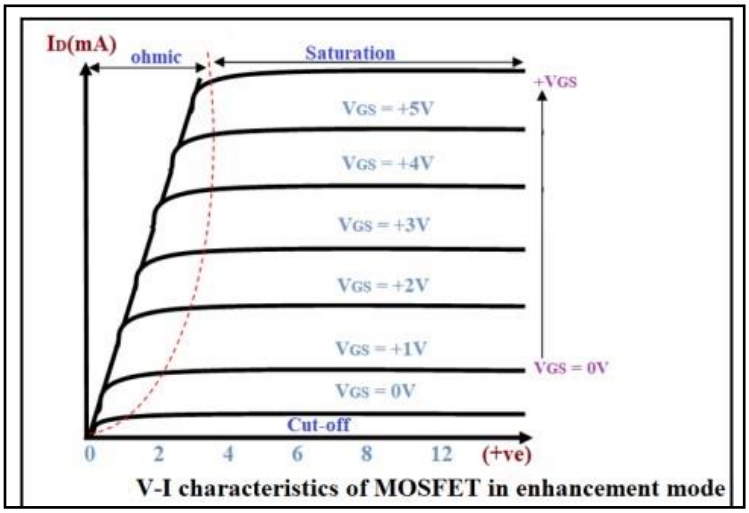

Fig 2.2. V-I Characteristics of MOSFET

2.3. Design and Optimization of DG MOSFET – p-MOS and n-MOS Comprising of Double Source Double Gate

2.3.1. Device Structure and Fabrication Feasibility:

In this work two type of MOSFET transistors are fabricated in virtual fabrication lab that is Silvaco Atlas. The fabricated MOSFETs are p-MOS and n-MOS. In both the MOSFET, the two GATEs are considered, which are normally called as DGMOSFET. The GATEs are made of polysilicon. The source and drain are made of silicon with the length of 15nm each. The doping is done with p type material, Boron in these source and drain. The source and drain concentrations are 1e20 and 1e18 respectively. The channel concentration is 1e15 and the length

is considered 30nm. In this unique structure we use the two layers of Silicon-germanium (SiGe) in the top and bottom of the channel, with the doping concentration of 1e17. Silicon-germanium enables faster and more efficient manufacturing of devices using smaller, less noisy circuits. This Silicon-germanium is commonly used in heterojunction bipolar transistor or in CMOS transistor for better performance, which has motivated to use in this new novel structure. All the lengths are optimized shown in the Table.1. The best solutions are taken in this structure. The schematic representation of the proposed DG MOSFET – p-MOS and n-MOS device is depicted in fig.2.3 and fig.2.4.

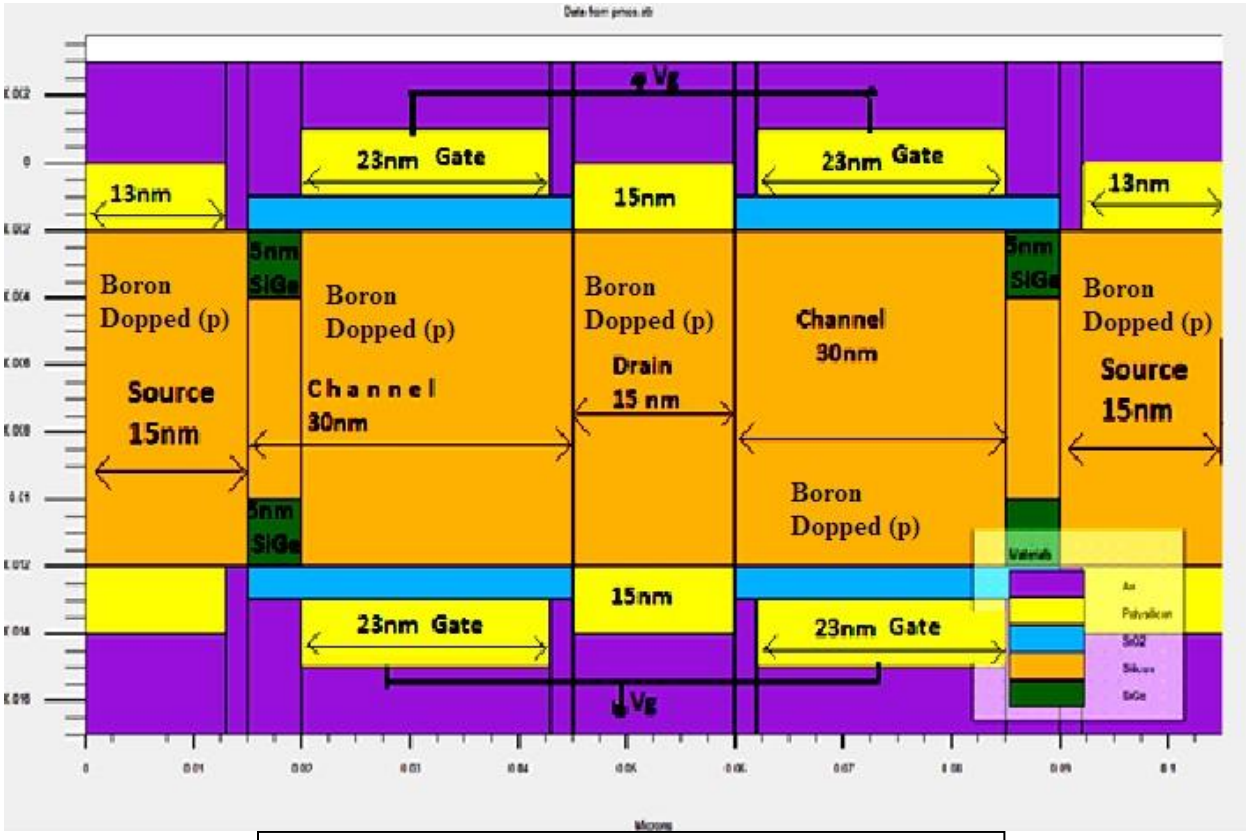

Fig.2.3. Cross Section of Proposed DGMOSFET p-MOS

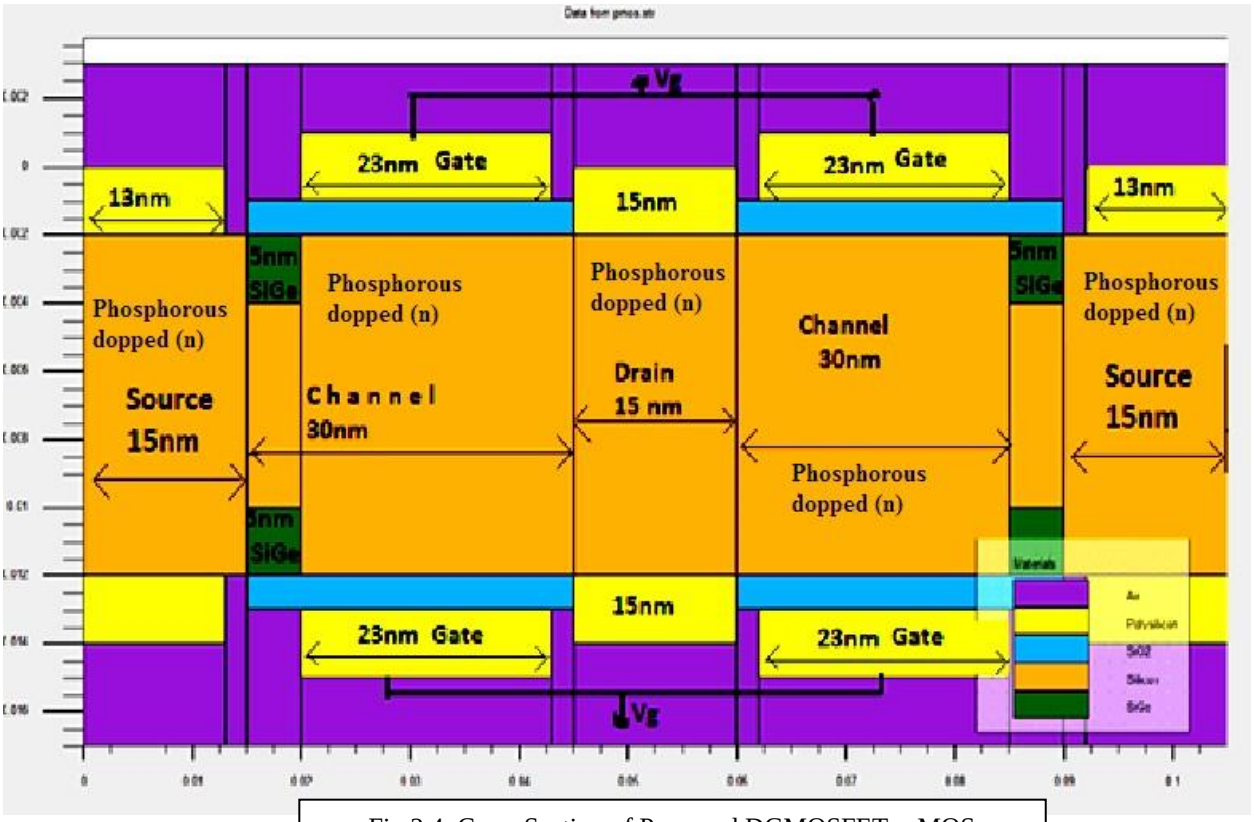

Fig.2.4. Cross Section of Proposed DGMOSFET n-MOS

CHAPTER-3

Analytical Modeling and results of the Proposed DG MOSFET Structure: Quantum approach

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3.1. Introduction

3.2. Surface Potential Modeling

3.3. Electric Field Modeling

3.4. Modeling of Threshold voltage

3.5. Results

Introduction: The basic Metal-On-Semiconductor-Field-Effect-Transistor (MOSFET) has modified itself into work function engineered multi-gate structure using its excellent adaptability. While the underlying operational principal has remained the same, the performance has greatly enhanced by the insertion of additional gates. The motivation behind the introduction of different structures is to maintain the trend of continuous **"scaling" of device dimensions**. In modern MOSFET, the channel length is approaching the mean distance between consecutive carrier collisions, while the oxide layer thickness is reaching the dimension of a few atomic layers [3-5]. To compensate this step-down, the channel doping must be increased. This process might no longer meet the required performance because of the degradation in mobility in the channel due to enhanced doping [7]. Introduction of new material systems as well as new device architectures, in addition to continuous process control improvement are needed to break the scaling barriers [6].

But as the device dimensions are being comparable to electron de Broglie wavelength classical physics is becoming insufficient to understand fully the behaviour of MOSFETs at

these small dimensions. For all these new structures, one of the identified challenges remains the development of compact models taking into account the main physical phenomena governing the devices at this scale of integration [8,9]. Hence quantum confinement effects are needed to be considered in MOSFET design and modelling. In this situation, significant deviation from the classical calculation is observed in the behaviour of MOSFETs, which must be explained by quantum theory.

3.2. Surface Potential Distribution

To study the device characteristics, the distribution of surface potential along the channel must be observed. Just before the onset of strong inversion, the potential distribution in the silicon thin film can be estimated from the Poisson's equation. For n-channel MOSFET with undoped silicon film, the electrostatic potential $\phi(x, y)$ in the silicon is described by the 2-D Poisson's equation:

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = -\frac{qN_A}{\varepsilon_{Si}} \quad ;0<=x<=L \ \& \ 0<=y<=t_{Si} \ \ldots\ldots (2.1)$$

Where, N_A and ε_{Si} are the uniform acceptor concentration (assuming the impurity density in the channel region to be uniform) and the dielectric constant of silicon respectively. Here, the effect of the fixed oxide charges on the electrostatics of the channel is neglected.

As proposed by K.K. Young, at low drain-source voltage V_{ds}, the 2-D potential profile $\phi(x, y)$, can be approximated by a simple parabolic function as [2.17]

$$\phi(x, y) = c_0(x) + c_1(x)y + c_2(x)y^2 \ \ldots\ldots (2.2)$$

This equation basically describes the y-dependence of the potential profile, whereas, the coefficients $c_0(x)$, $c_1(x)$, $c_2(x)$ are functions of x only.

Boundary conditions for potential: -

1. At gate oxide interface, surface potential

$$\phi_s(x, \frac{t_{Si}}{2}) = \phi_s(x) \quad \text{.....2.3}$$

2. Electric field at the center of the channel: -

$$\frac{\partial\phi(x,y)}{\partial y} = 0 \; at \; y = 0 \quad \text{.....2.4}$$

3. Electric field displacement is continuous across channel gate oxide interface

$$\frac{\partial\phi(x,y)}{\partial y} = \frac{C_{ox}}{\varepsilon_{Si}}[V_{GS} - \phi_s(x)] \text{ at } y=\frac{tSi}{2} \quad \text{.....2.5}$$

For finding coefficients $c_0(x)$, $c_1(x)$, $c_2(x)$:-

By solving the boundary conditions, i.e., equations 2.3, 2.4, 2.5 we get

$$c_0(x) = \phi_s(x)\left[1 + \frac{C_{ox}\, t_{Si}}{4\varepsilon_{Si}}\right] - \frac{V_{GS}C_{ox}}{4\varepsilon_{Si}} \quad \text{.....2.6}$$

$$c_1(x) = 0 \quad \text{.....2.7}$$

$$c_2(x) = \frac{Cox[VGS - \phi s(x)]}{t_{Si}\,\varepsilon_{Si}} \quad \text{.....2.8}$$

Similarly, the channel flat band voltages of the p+ poly at the gate would be different and is given as:

$$V_{FB} = \phi_M - \phi_{Si} \text{.....2.9}$$

ϕ_M→ Metal work function

ϕ_{Si} is the silicon work function, which is given by

$$\phi_{Si} = \chi_{Si} - \frac{E_g}{2q} + \phi_F \quad \text{..... (2.10)}$$

With, χ_{Si} = The electron affinity of silicon

E_g = The silicon bandgap at 300 K

ϕ_F = The Fermi potential

q = The electron charges

Now it is evident that the Poisson's equation must be solved front gate materials using the boundary conditions given below:

1) $\phi_s(x,0) = \phi_s(x) = c_0(x)$.....2.11

2) Electric field at front gate(y=0)

$$\frac{\partial\phi(x,y)}{\partial y} = \frac{s_{ox}}{\varepsilon_{Si}}\left[\frac{\phi_f(x) - V_{GS}}{t_{ox}}\right] = c_1(x) \quad at\ y = 0 \text{.....2.12}$$

3) Electric field at back gate ($y=t_{si}$)

$$\frac{\partial\phi(x,y)}{\partial y} = \frac{s_{ox}}{\varepsilon_{Si}}\left[\frac{\phi_b(x) - V_{GS}}{t_{ox}}\right] = c_1(x) \quad at\ y = t_{si} \text{.....2.12}$$

As front and back gate are same, thus $\phi_f(x) = \phi_b(x)$

Last two equations stand for continuity of electric flux at the front gate–oxide interface of the DMG. ε_{ox} is the dielectric constant of oxide (SiO_2) and t_{Si} is the oxide thickness at front gate.

$V'_{G1} = V_{GS} - V_{FB1}$ Where, V_{GS} is the gate-to-source bias voltage,

The second and third equations express continuity of electric flux at the back gate–oxide and back-channel interface. Here, ε_{ox} is the dielectric constant of the oxide (air is taken as the back gate oxide for DG MOS structure), t_{Si} is back oxide thickness, $\phi_B(x)$ is the potential function along the back gate oxide -silicon interface, $V'_{GSb} = V_{GS} - V_{FBb}$ where, V_{FBb} is the back gate flat-band voltage and is same as that of V_{FB2} .

V_{bi} is the built in potential across the body-source junction given by :

$V_{bi} = V_T \ln(N_A N_D / n_i^2)$ Where, n_i is the intrinsic carrier concentration.

These boundary conditions (1st to 4th of (2.7)) are applied to find the coefficients, which are:-

$$c_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi_{S1}(x) - V'_{GS1}}{t_f}$$

$$c^{12}(x) = \frac{V'_{GSb} - \phi_{s1}(x) \left[1 + \frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right] + V'_{GS1} \left[\frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right]}{t_{Si}^2 \left[1 + 2\frac{C_{Si}}{C_b}\right]} \quad \text{.....(2.8)}$$

$$c_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{-\phi_{S2}(x) - V^F_{GS2}}{t_f}$$

The solutions which will give the expressions of surface potentials will be of the form

$$\phi_{S1}(x) = Ae^{\eta x} + Be^{-\eta x} - \frac{\beta_1}{\alpha} \quad \text{..... (2.12)}$$

Substituting the values of constants in equations (2.1) & (2.2), we get

$$\frac{d^2\phi_f(x)}{dx^2} - \frac{1}{\lambda^2}[\phi_f(x) + V_{GS}] = -\frac{qN}{\varepsilon_{Si}} \quad \text{..... (2.8)}$$

$$\boldsymbol{\lambda} = \sqrt{\frac{\varepsilon_{Si} t_{ox} t_{si}}{\varepsilon_{ox}}} \quad \text{..... (2.9)}$$

$$\phi(x) = \phi_f(x) - V_{GS} - \frac{qN\lambda^2}{\varepsilon_{Si}} \quad \text{..... (2.10)}$$

And

Equation 2.8 simplifies to

$$\frac{d^2\phi_f(x)}{dx^2} - \frac{1}{\lambda^2}[\phi(x)] = 0 \quad \text{..... (2.11)}$$

Now, applying boundary conditions in 2.11 at source side.

$$\phi(x = 0) = -V_{bi} - \sigma = \phi_s \quad \text{.....(2.12)}$$

At the drain side

$$\phi(L) = V_{ds} + V_{bi} - \sigma = \phi_d \quad \text{.....(2.13)}$$

Solving 2.11 by using 2.12 and 2.13:-

We get the surface potential in the 1st channel(15nm<=x<=45nm in the structure):-

$$\phi(x) = \frac{\phi_s(e^{(L-x)/\lambda} - e^{-(L-x)/\lambda}) + \phi_d(e^{(x)/\lambda} - e^{-(x)/\lambda})}{e^{(L)/\lambda} - e^{-(L)/\lambda}} \text{ ; for 15nm<=x<=45nm.....(2.14)}$$

Similarly for the 2nd channel(60nm<=x<=90nm) surface potential obtained is

$$\phi(x) = \frac{\phi_d(e^{(L-x)/\lambda} - e^{-(L-x)/\lambda}) + \phi_s(e^{(x)/\lambda} - e^{-(x)/\lambda})}{e^{(L)/\lambda} - e^{-(L)/\lambda}} \text{ ; for 60nm<=x<=90nm.....(2.15)}$$

The electric-field distribution along the channel length can be obtained by differentiating the surface potential given by (2.14) and (2.15).

$$\frac{\partial\phi(x)}{\partial x} = E_x = \frac{\phi_s(-\frac{1}{\lambda}e^{(L-x)/\lambda} - \frac{1}{\lambda}e^{-(L-x)/\lambda}) + \phi_d(\frac{1}{\lambda}e^{(x)/\lambda} + \frac{1}{\lambda}e^{-(x)/\lambda})}{e^{(L)/\lambda} - e^{-(L)/\lambda}}; \quad \text{for15nm<=x<=45nm……(2.15)}$$

$$\frac{\partial\phi(x)}{\partial x} = E_x = \frac{\phi_d(-\frac{1}{\lambda}e^{(L-x)/\lambda} - \frac{1}{\lambda}e^{-(L-x)/\lambda}) + \phi_s(\frac{1}{\lambda}e^{(x)/\lambda} + \frac{1}{\lambda}e^{-(x)/\lambda})}{e^{(L)/\lambda} - e^{-(L)/\lambda}}; \quad \text{for 60nm<=x<=90nm……(2.16)}$$

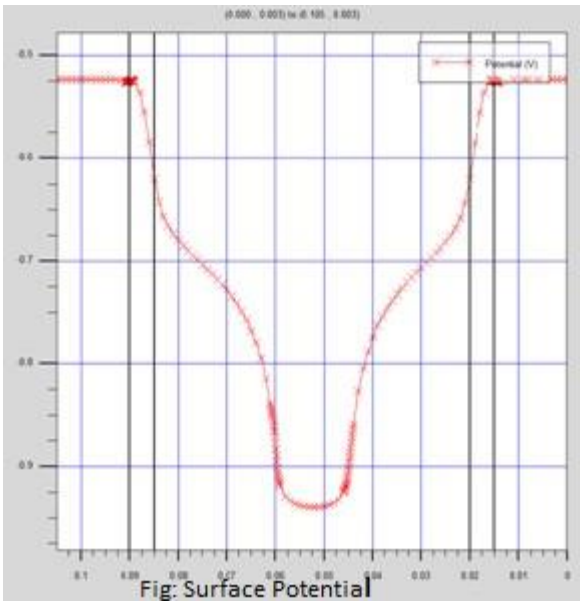

Fig3.1. Potential curve of DGMOSFET

Graphical representations of surface potential distribution and electric field in a general DG MOSFET structure.

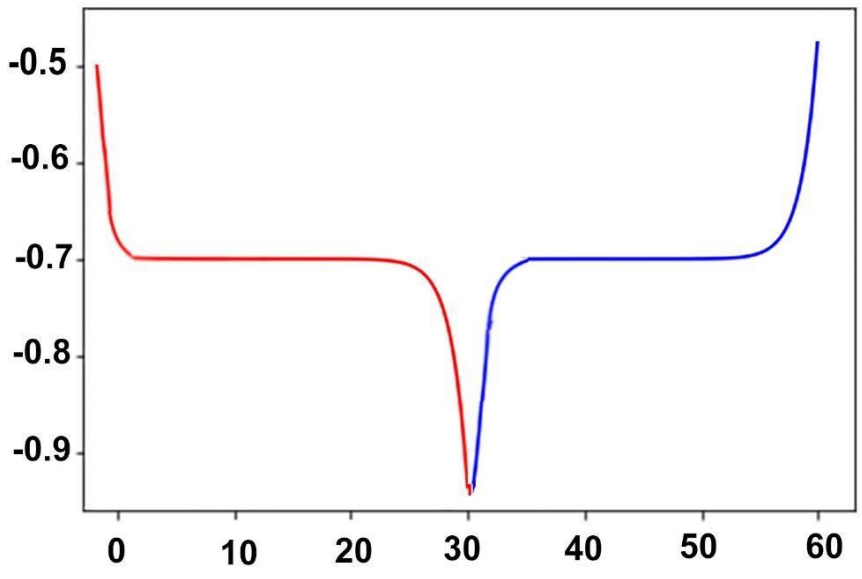

Fig. 3.2. Distribution of surface potential along the channel length obtained from analytical model

The results obtained from their research are shown in Fig.3.1 & Fig. 3.2 which represents the calculated and simulated surface-potential profiles of DG MOSFETs at the silicon–oxide interface. It is clearly observed that the DG structure exhibits a step function in the surface potential along the channel. The step is generated almost at the midpoint of the channel. Due to this stair like feature, the area under the p+ poly front gate is essentially screened from the drain-potential variations; resulting a minimized effect of the drain potential on the drain current after saturation [19]. This means a significant reduction in the drain conductance and DIBL.

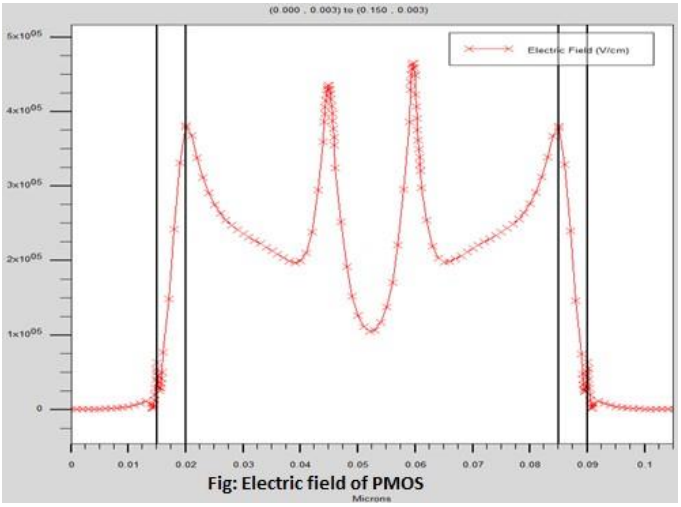

Fig. 3.3. Distribution of electric field along the channel length.

The calculated and simulated values of the electric field along the channel length at the drain end for the DG MOSFET and the simulated values for the DG MOSFET for the same channel length are shown in Fig. 3.3 [14]. This result establishes the fact that, due to the presence of discontinuity in the surface potential of the DG structure, the peak electric field at the drain is reduced substantially, by approximately 40%, when compared with that of the DG structure. This reduction results a reduced hot carrier effect.

Formulation of Threshold Voltage: -

Threshold voltage is one of the most basic and authoritative electrical parameters of any MOSFET device. As proposed by G. Venkateshwar Reddy and M. Jagadesh Kumar in [8], the threshold voltage for the DG MOSFET structure can be calculated from the graphical approach, as has been done for DG MOSFETs by K. Suzuki and T. Sugii [17]. When they studied the potential distribution dependence on the gate voltage, it was found that first an inversion layer is formed on the inside surface of the back gate n+ polysilicon. After this condition, the potential distribution changes linearly while the surface potential remains fixed. Then an inversion layer is formed on the inside surface of the p+ polysilicon and the potential distribution in the channel becomes invariable. The applied voltage is sustained by both the gate oxides. At the threshold voltage, the control gate will be turned on with two adjacent screen gates and the full channel conduction will take place accordingly. In this case the subthreshold behavior of the device will be determined by the position of minimum central potential. The position of the central position will be determined under high work function of gate metal; i.e., M_1 at $x=x_{min}$

At $x= x_{min}$ the electric field is assumed to be zero. So,

$$x_{min} = \frac{\lambda}{2} \ln \left(\frac{\phi_d}{\phi_s}\right)$$

Therefore, minimum central potential

$$\emptyset_c = 2\sqrt{\alpha\beta} + \sigma$$

The threshold voltage is defined as the required gate voltage for which the minimum central potential can be equated as twice the difference between the Fermi potential and the intrinsic Fermi level in the bulk region of the conducting channel. Thus, we get $\emptyset_c = 2\emptyset_f$.

Solving these, the formula for threshold voltage is obtained as

$$V_{th} = \frac{-Y + \sqrt{Y^2 - 4XZ}}{2X}$$

Where

$$X = \left\{ \exp\left(\frac{L}{\lambda}\right) + \exp\left(\frac{-L}{\lambda}\right) - 2 \right\}$$

$$- \left\{ \left[\exp\left(\frac{L}{\lambda}\right) + \exp\left(\frac{-L}{\lambda}\right) \right]^2 \right\}$$

$$Y = J_1 + J_2 + J_3 + J_4 + J_5$$

The threshold voltage obtained is 0.25V, which is in consonance with the result obtained from simulation results.

Graphs and results of p-MOS:-

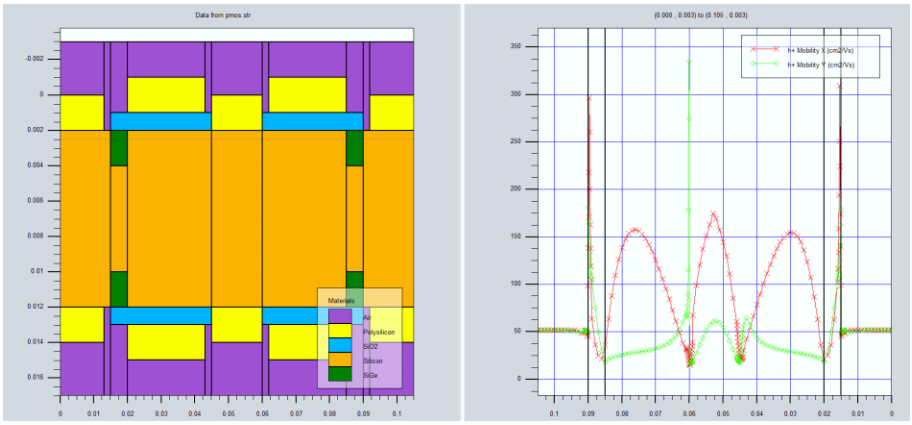

Fig 3.4: Hole Mobility characteristics seen in pMOS

Thus, mobility is expected to degrade in the thinner devices due to a greater phonon scattering rate and this fact can be found in the Fig.3.4 . As the dimensions of CMOS transistors are scaled to deep submicron region, device scaling is becoming extremely difficult due to many physical and technological problems. To maintain the scaling trends, new materials and device

structures have to be introduced. Recently, silicon–germanium (Si−Ge) has been considered as a promising device conduction layer for sub micrometer CMOS channel engineering. Many researches have proved that compressively strained-SiGe or strained-Ge channels could provide a significant mobility gain for long-channel PMOS devices. The mobility gain under the biaxial compressive strain is attributed to the reduction of the hole effective mass as well as the splitting between the degenerated heavy hole, light hole, and spin-orbit split-off hole bands. On the other hand, various local-strain technologies have been extensively implemented in CMOS devices to improve device performance.

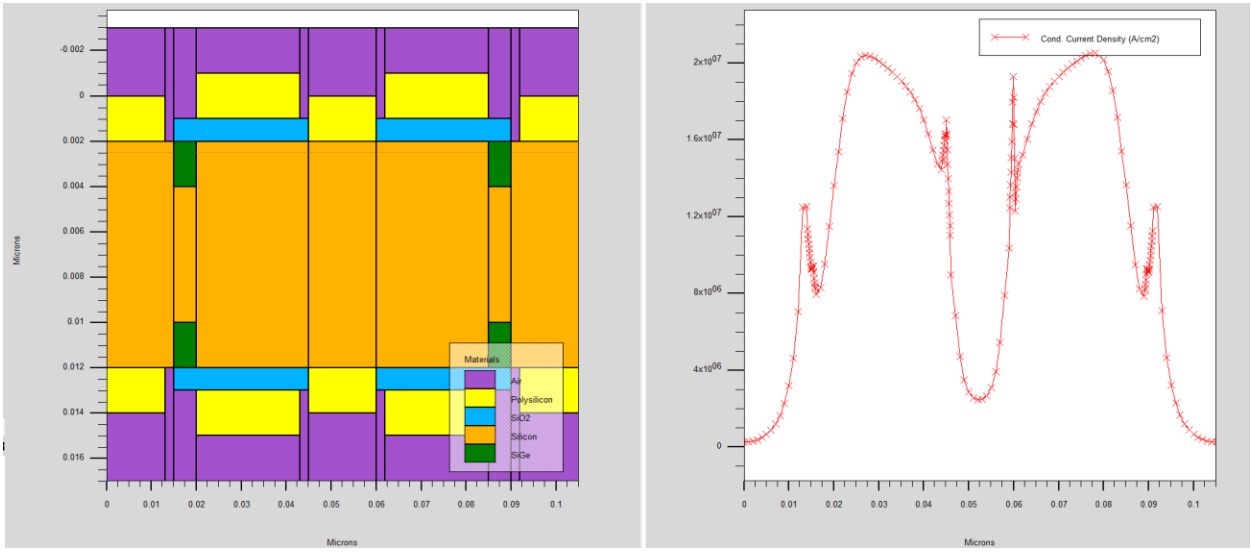

Fig 3.5 Conduction Current as seen inside p-MOS

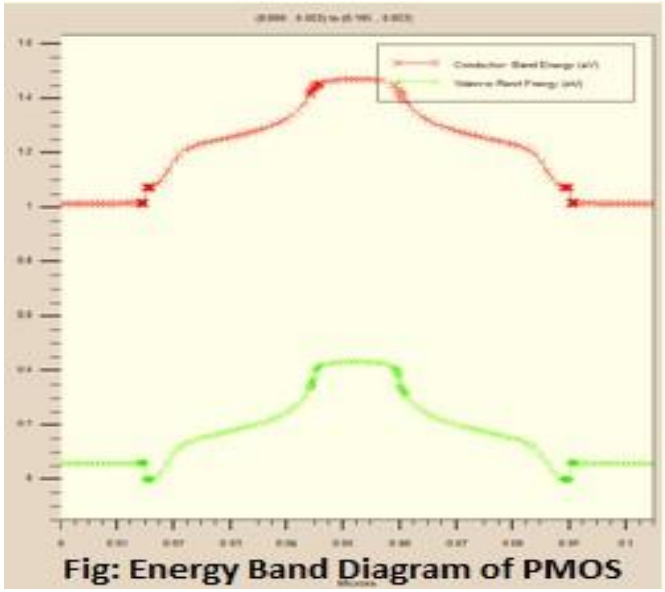

Fig 3.6. Energy Band Diagram as seen after simulation

Usually, the system has a large number of atoms and the higher energy levels tend to unite into two separate bands of allowed energies, called the Conduction band and the Valence band, respectively. The Conduction band – is the upper band, where energy levels are almost empty. Energy level Ec – is the bottom of the conduction band. The Valence band – is the lower band where energy levels are full. Energy level EV – is the top of the valence band. The difference between two of these levels is called the bandgap energy (Eg)

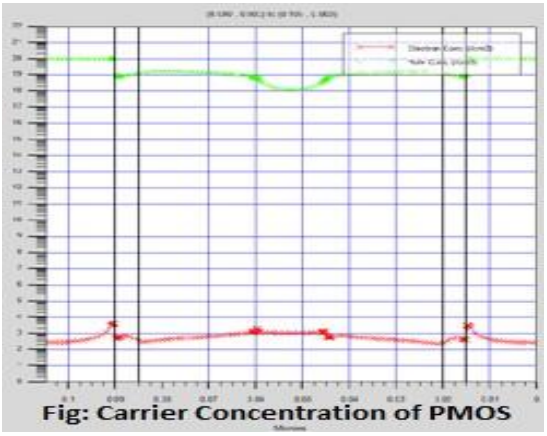

Fig 3.7. Carrier Concentration as seen in simulation

Large numbers of states are allowed in the conduction and valence band. However, there would not be many electrons in the conduction band for an intrinsic semiconductor because electrons prefer states with lower energy that are in the valence band. Therefore, an electron can occupy one of these upper states with a very small probability. Most of the allowed states in the valence band will be occupied by electrons. Hence, the electron can occupy one of these states with a probability near one. Unoccupied electron states in the valence band are referred to as holes.

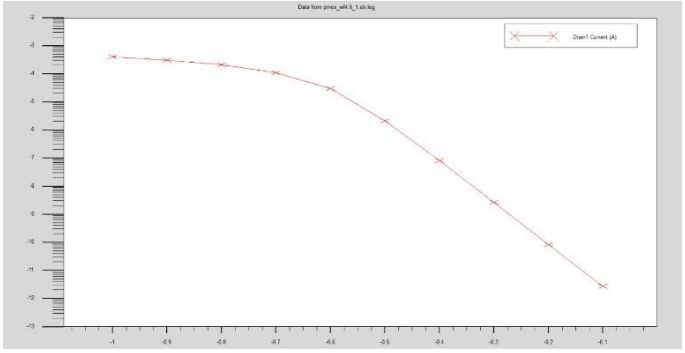

Fig 3.8. Characteristics curve of p-MOS as seen after simulation

Calculation Result for PMOS

Vt→0.345243104077909

SS→0.0667955502246567

Ioff→-2.733267114e-12

Ion→-0.0004073026083

Ioff/Ion→149016745.509957

Results obtained for NMOS:

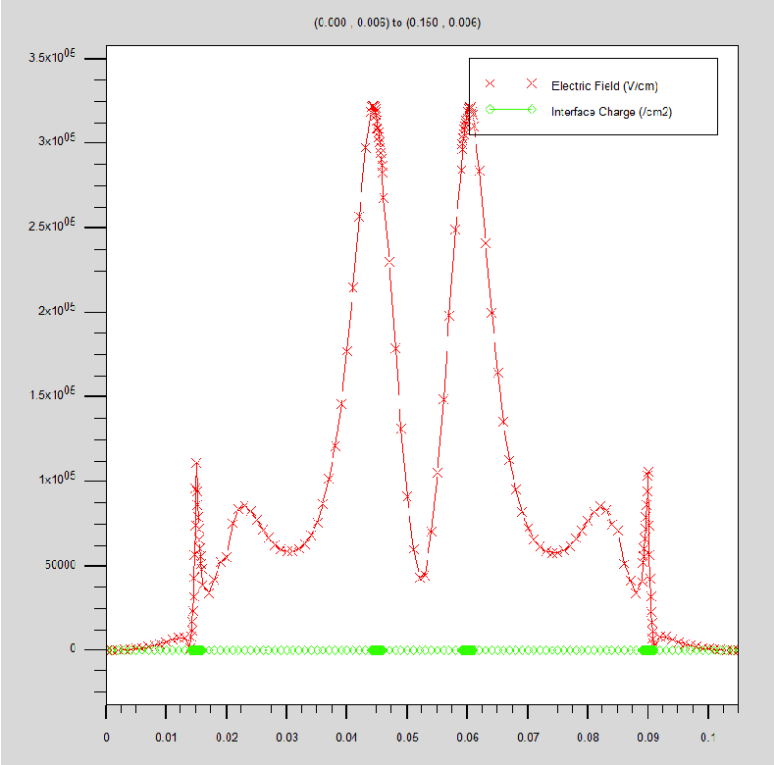

Fig 3.9 Electric Field in NMOS as obtained from simulation

The Electric field across the length of the channel of NMOS transistor is established due to the voltage between the drain and source and is represented as E = VDS/L or Electric field across the length of the channel = Voltage between drain and source/Length of the Channel. The voltage between drain and source is applied positive voltage between drain and source, having induced a channel & The length of the channel, L, which is the distance between the two n+-p junctions

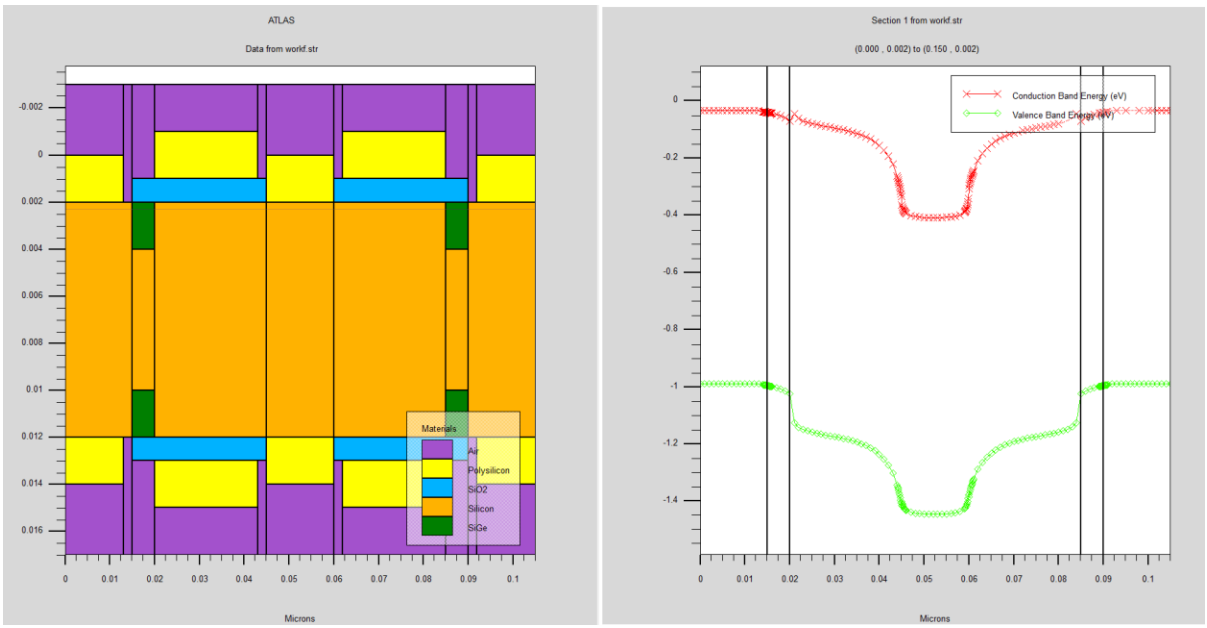

Fig 3.10. Band energy diagram as obtained for NMOS

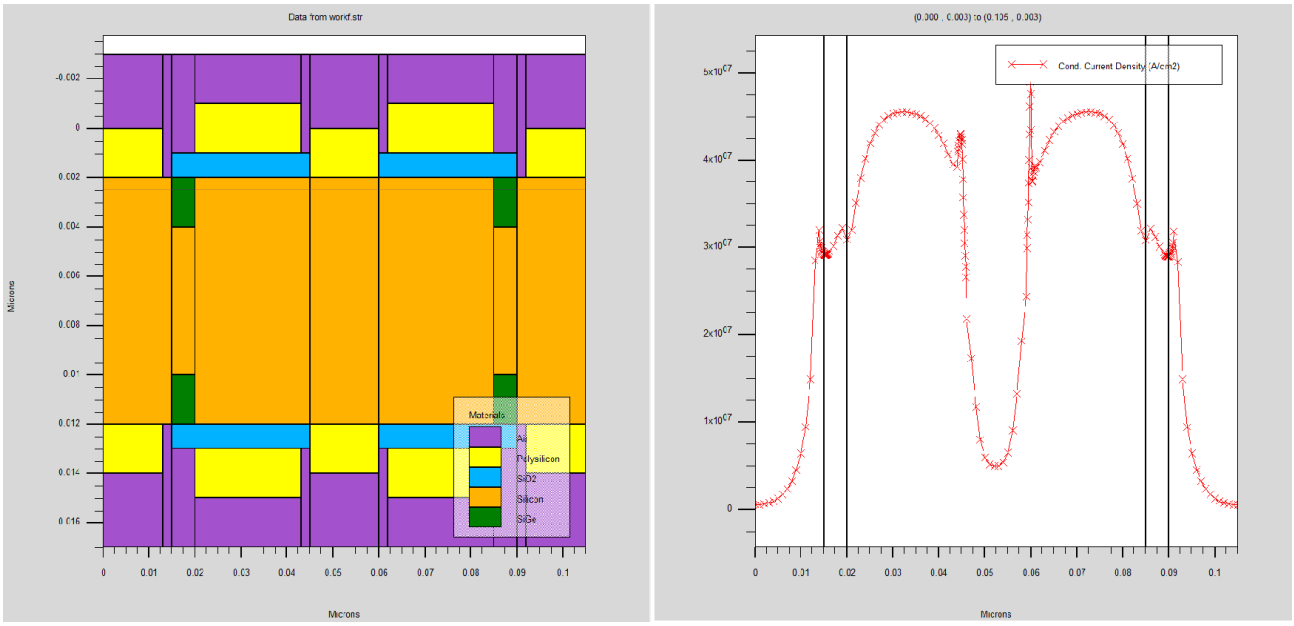

Fig 3.11. Conduction Current Density as seen in simulation result

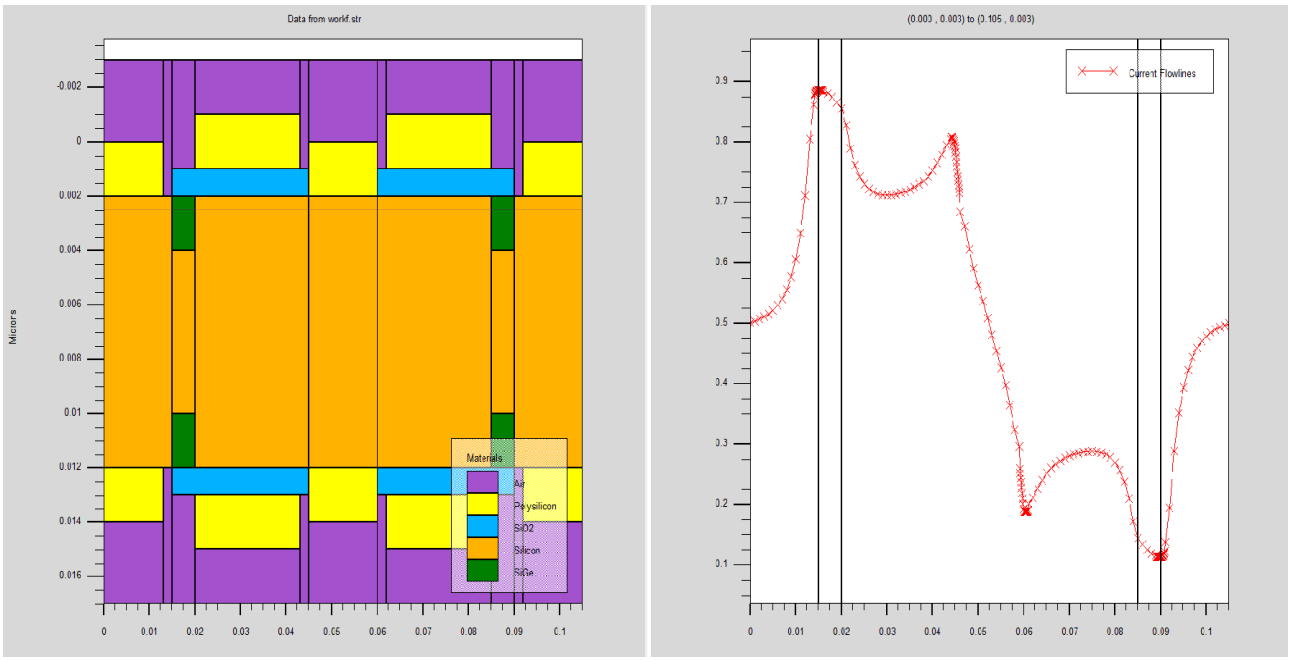

Fig 3.12. Current flowlines n-MOS

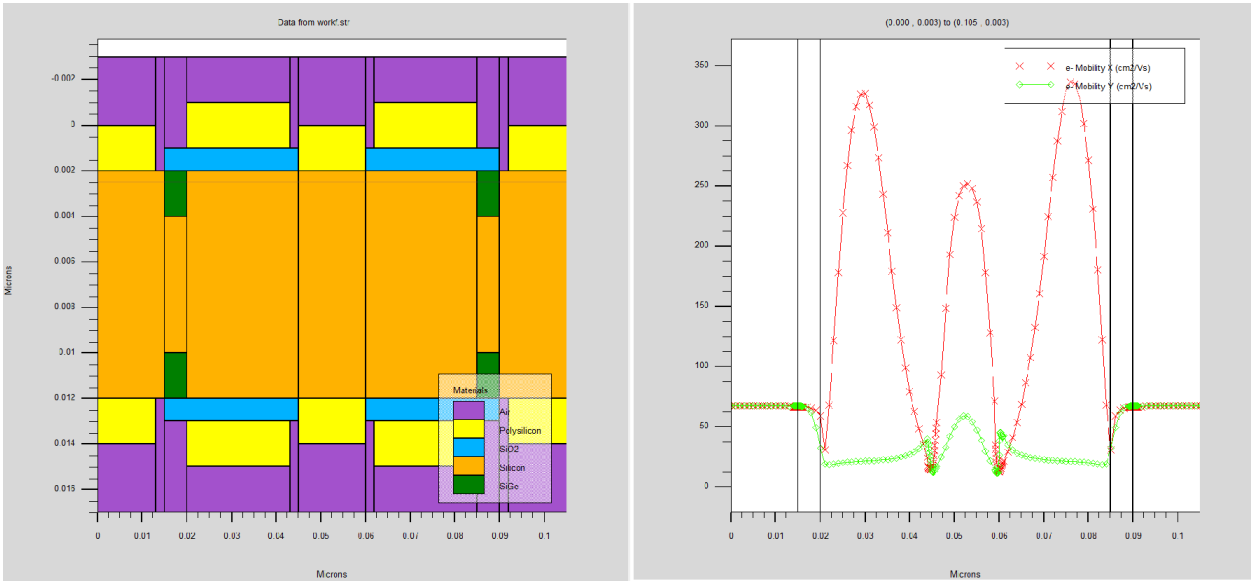

Fig 3.13. Electron Concentration of n-MOS

In the proposed structure SiGe doping is done in the channel which infuses more electron carrier into the channel and thus increase the mobility.

The n-MOS structure is also fabricated in similar mode that is in Silvaco Atlas, which is shown in fig.2. This n-MOS structure is made with two Gates using polysilicon. The source and drain are made of Silicon and doped with Phosphorous. The concentration of doping materials in source, drain and channels are 1e20, 1e18 and 1e15 respectively.

Impact on Mobility:

In MOSFET structures, regardless of the potential well, the movement of the carriers is limited by the silicon film thickness (due to the SiO_2 barriers that surround the silicon). As an example, in thin film DG MOSFETs, the potential well is defined by both the front and back gates. Here the mobile carriers are confined due to:-

(i). Electrical confinement:- strong electric field at the interface leading to quantum confinement (EC-QM) and

(ii) Structural confinement:- t_{si} induced quantum confinement (SC-QM) due to the narrow potential well defined by the silicon film.

In such devices, when the silicon film thicknesses are comparable to their de Broglie wavelength, quantum size effects become considerable in the whole bias range, even at very low inversion charge concentrations. Once the potential distribution, inversion and depletion charge concentrations in the structure have been calculated, the electron dynamics are simulated by the one-electron Monte Carlo method [22]. Here, a quantum-mechanical calculation is applied to calculate the spatial and energy distribution of electrons in this structure. Poisson and Schrödinger equations have to be solved self-consistently assuming a simple non-parabolic band model for the silicon.

By the extensive research carried out by Francisco G´amiz et al. [23] it has been shown that for the same inversion-charge concentration, the thinner the Si layer, the electrons are more confined resulting larger charge concentration. Therefore, the phonon scattering rate is increased significantly.

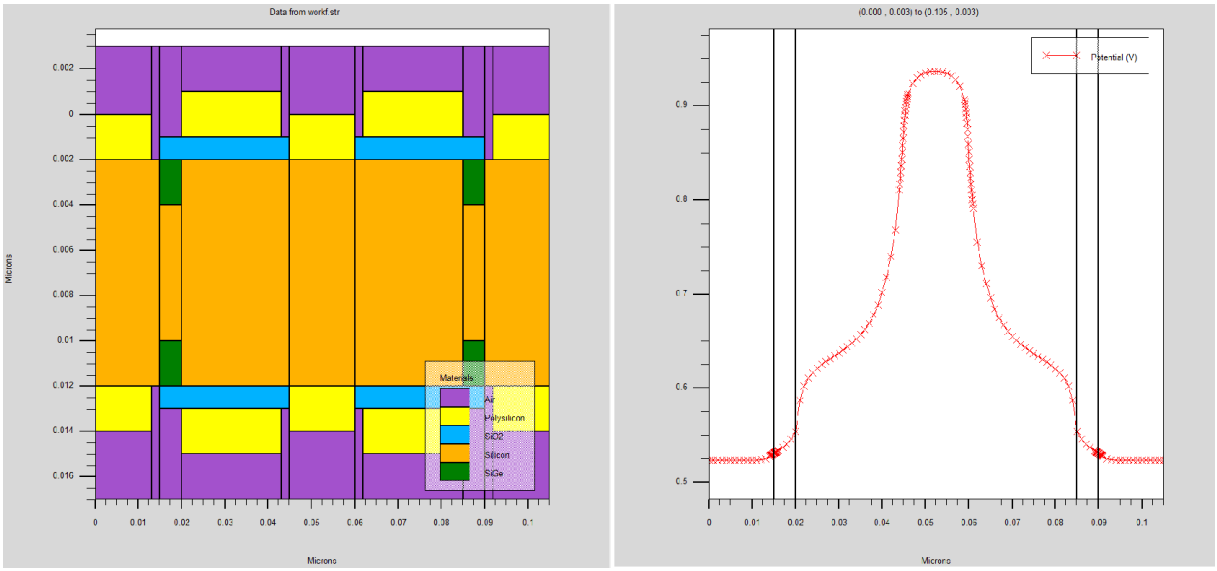

Fig 3.14. Potential curve along the channel for NMOS

Surface Potential is the difference between the voltage at the surface of the MOSFET capacitor — (the top layer of polysilicon or metal above the oxide layer) — and the voltage in the *bulk* of it. It is significant because the (gate-to-source) threshold voltage is determined by this relation.

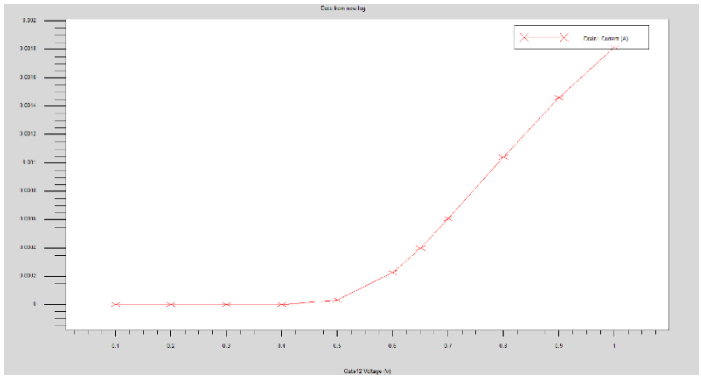

Fig 3.15. Characteristics curve for NMOS

Calculation Result for n-MOS

Vt→ 0.310660249648588V

SS→ 0.0689874201343345mV/decade

Ioff→ 8.727364165e-11

Ion→ 0.001816040145

Ioff/Ion→ 20808583.5808309

CHAPTER-4

Boolean Implementation of proposed p-MOS structure as AND & NAND

4.1. Introduction:

Complementary metal oxide semiconductor (CMOS) technology has been used over the past four decades to realize digital circuits since it provides excellent performance, extremely small standby power consumption, low cost, and good reliability characteristics. However, the continued downscaling of device dimensions has caused the conventionalmetal oxide semiconductor field-effect transistor (MOSFET)-based devices to exhibit undesirable characteristics, such as high leakage current. Consequently, the threshold voltage of the transistors and the supply voltage of the digital circuits cannot be further reduced in MOSFETs without degrading the performance and the energy efficiency. Therefore, researchers have been exploring devices based on different operating principles. Among these exploratory devices, DGMOSFETs have attracted a great deal of attention [4], [9], [13]. Although the application of a DGMOSFET in digital circuits is challenging due to low ON-state current and a high ambipolar current, certain digital circuits, such as inverters, and arithmetic circuits have been demonstrated in the literature. In this article, the implementation of Boolean functions, such as AND, NOT, NAND have been shown to be realized using a single double-gate MOSFET (DGMOSFET) requiring fewer transistors in comparison to the conventional CMOS-based implementations [21], [24]. It is shown that, when the architecture of a DGMOSFET is slightly modified, and the device parameters are appropriately chosen, the

DGMOSFET can implement the required two-input Boolean functions. Using these inhibition functions,the implementation of the DGMOSFET-based AND function is demonstrated.

4.2. Logic AND Gate & NAND Gate

In this work one p-MOS transistor is used to validate the AND gate using simulation tools. The two terminals of the proposed DGMOSFET are biased independently to realize the two inputs Boolean Functions such as AND & NAND gate. By modifying the architecture of double gate MOSFET slightly and appropriately choosing device parameters, the Boolean functions AND, NAND gate can be implemented using one transistor instead of 6 transistors.

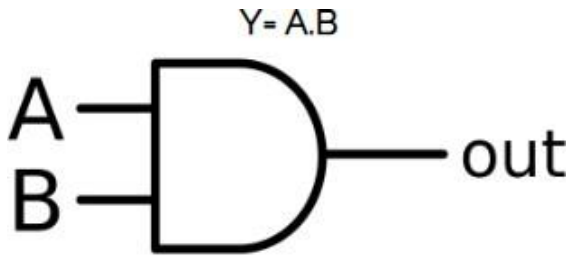

Fig. 4.1: Logic symbol of AND gate

Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Table.4.1. Truth Table of AND gate

The logic AND gate is an electronic circuit that gives a high output (y=1) only if all its inputs are high (A=1 & B=1). A dot (.) is used to show the AND operation i.e. A.B or can be written as AB. A simple 2-input logic AND gate can be constructed using 6 PMOS with two NMOS in series and 2 PMOS in parallel connection and output of it connected to CMOS inverter to get the desired output. The proposed structure replaces this 6 transistors thus saving on area and helping to boost the VLSI technology to a great extent.

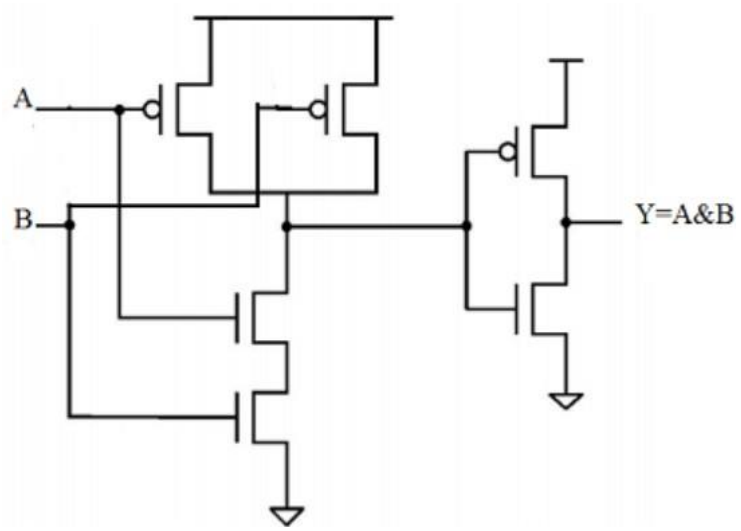

Fig.4.2. Conventional AND Gate using 6 transistors

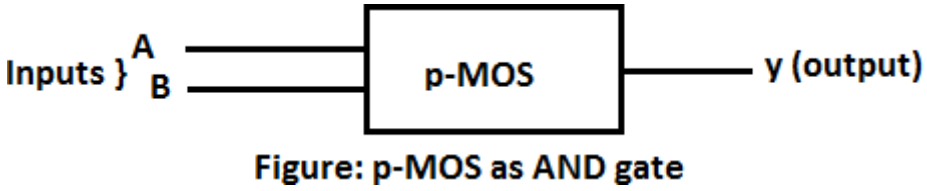

Figure: p-MOS as AND gate

Fig.4.3. p-MOS as AND Gate

NOT gate

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A that is A with a bar over the top, as shown at the outputs $\bar{A}$

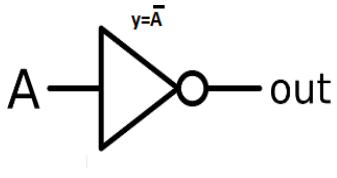

Figure Logic Symbol of NOT Gate

Fig 4.4

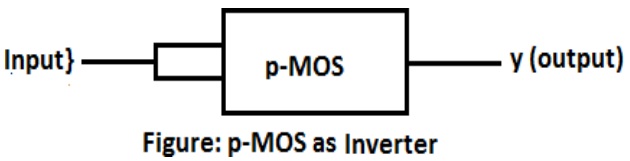

Figure: p-MOS as Inverter

Fig 4.5: NOT gate using proposed structure

Input	Output
A	Y
0	1
1	0

Truth Table of NOT Gate

Table 4.2

The NOT gate can be realised using the proposed structure of DG MOS. The two input terminals are shorted that is same input is given to the both terminals, and the inverted output will satisfy the logic.

NAND gate:

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

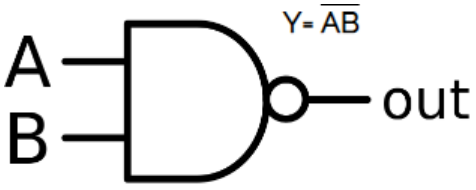

Figure Logic Symbol of NAND Gate

Fig.4.6

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure Truth Table of NAND Gate

Table 4.3

A simple 2-input logic NAND gate can be constructed using 4 MOSFET transistors with 2 NMOS in series and 2 PMOS in parallel connection thus helping in saving area to a great extent [21-22].

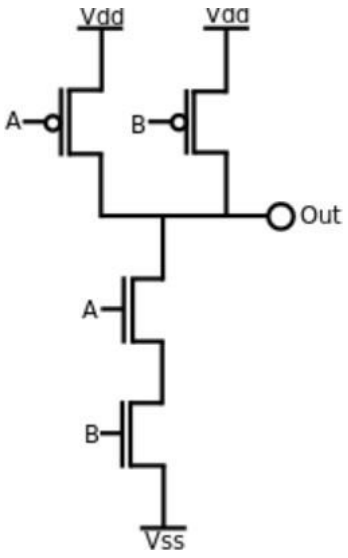

Table 4.7: Conventional NAND gate using 4 transistors

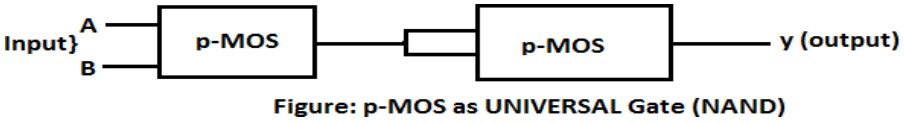

Figure: p-MOS as UNIVERSAL Gate (NAND)

Fig 4.8: NAND using proposed structure

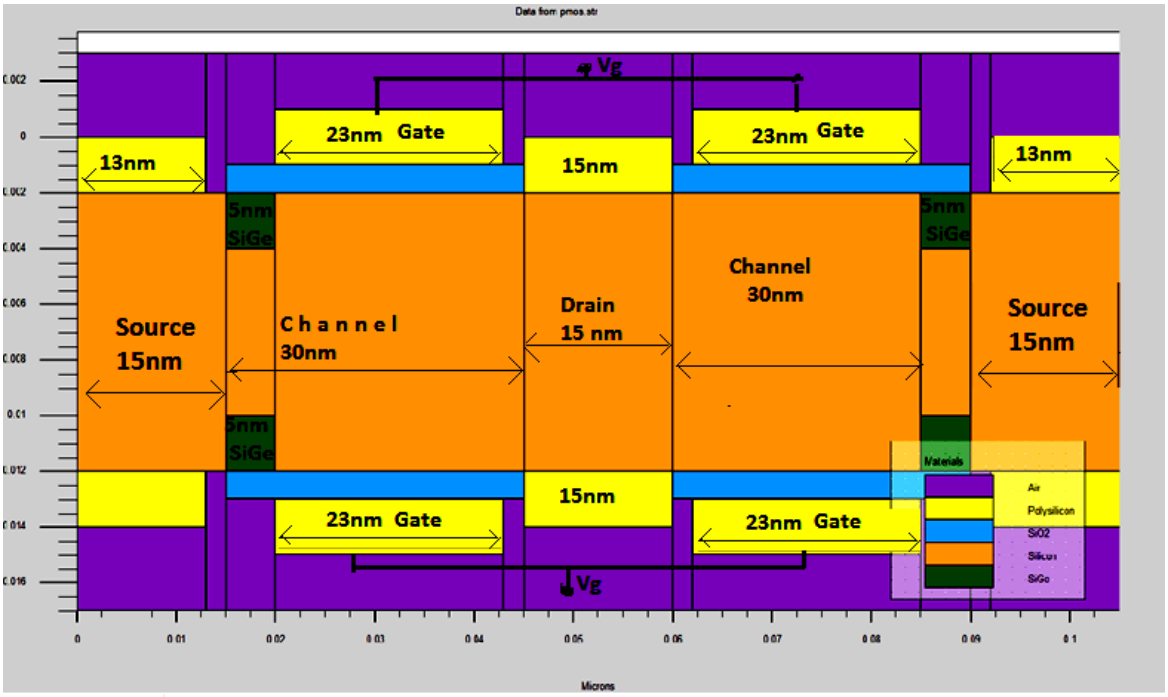

Fig 4.9 : Proposed DG MOSFET

The above Figure shows the cross-sectional view of an p-type DGMOSFET. The top gate is called $G1$, and the bottom gate is called $G2$. Conventionally, the two gates are tied together to boost the ON-state current. However, in the DGMOSFET -based Boolean function implementation, the two gates are biased independently at the voltages: V_A and V_B.

In this work, we treat the voltage V_{DD} (D0:5 V) and ground (D0 V) as logic ``1" and logic ``0," respectively. When the gates of the DGMOSFET are biased at logic A and B, respectively, the input to the function can be represented as ``AB." There-fore, four possible inputs are ``00," ``01," ``10," and ``11." The drain current owing through the device corresponding to the input ``AB" is denoted as I_{AB}. In these logic function realizations, the magnitude of drain current I_{AB} owing through the device depends on the input to the function (``AB") and is modulated in accordance with the intended functionality. Table shows the input to the functions and the corresponding current owing through the device, $I_{AB}$ in the Supplementary Material. When the expected output is logic ``0" for the function, a low current through the DGMOSFET and is termed I_{OFF}, and when expected out- put is logic ``1" for the function, a high current through the DGMOSFET and is termed $I_{ON}$. For DGMOSFET based logic function realizations, it is desirable to achieve a sufficient $I_{ON}$=$I_{OFF}$ ratio to differentiate between logic ``0" and logic ``1." In this work, all simulations have been carried out using Silvaco TCAD (ATLAS) [21-24].

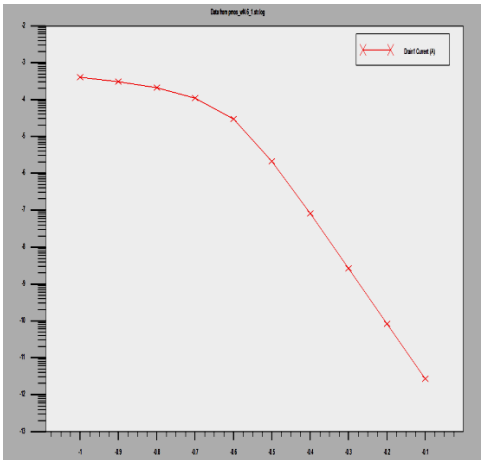

Fig 4.10: Characteristics curve resembling that of VTC curve for an inverter

The p-MOS acts as AND gate when two gates are given voltages and acts as inverter when two gates are short circuited. Y=A.B

Input=A	**Input=B**	**Y=output= AB**	**I_{ON}**	**I_{OFF}**
0	0	0	$\sim 10^{-10}$	2.733267114e-12
0	1	0	0.0004073026083	2.733267114e-12
1	0	0	0.0004073026083	2.733267114e-12
1	1	1	0.0008171284041	5.254121478e-12

Table4.4: Simulated results

CONCLUSION

As technology spreads over the scaling roadmap, the miniaturization of device dimensions has been the elemental factor leading to improvements in IC performance and reduction of cost. Owing to the fact that dimensional scaling of CMOS is eventually approaching fundamental limits, several new alternative structures are being explored in order to sustain the historical integrated circuit scaling. Amongst many other proposed structures in deep submicron technology, multiple gate MOSFET have become attractive options. Double gate (DG) MOSFET provides enhanced mobility, better I_{on}/I_{off} ratio and improved sub-threshold slope due to volume inversion of charge in the channel.

In this work it is considered that the structure using the two layers of Silicon-Germanium (SiGe) in the top and bottom of the channel, with the doping concentration of 1e17. Silicon-germanium enables faster and more efficient manufacturing of devices using smaller, less noisy circuits. This Silicon-germanium is used for better performance of this new novel structure.

As the device dimensions are getting comparable to the de Broglie wavelength, quantum mechanical effects (QMEs) become a significant factor and are required to be considered. The charge density is redistributed in the channel creating an entirely different profile. In this situation, the behaviors of MOSFETs are substantially deviated from the classical calculation and these discrepancies must be explained by quantum theory.

In this proposed model, a p type DG MOSFET structure has been chosen with channel length as short as 30 nm and thickness 10 nm. Carrier quantization has been taken into consideration by using self-consistent solution of 2D Poisson's equation and 1D Schrödinger equation. Based on the potential and charge distribution, a complete analytical drain current model is developed under drift-diffusion transport mechanism both in subthreshold and inversion region. For this ultra-scaled DG MOSFET structure, quantum confinement has been

included as an integral part of the model derivation. The electric field distribution, current-voltage characteristics, sub threshold slope, threshold voltage and I_{ON}/I_{OFF} are thoroughly studied for variations of major device parameters. In DGMOS structure, the electric field at the drain end is considerably lower. Therefore, DG MOSFET experiences much reduced short channel effects and increased carrier injection into the channel. These two properties ensure the acceptability of DG MOS structure in ultra-scaled CMOS technology. The comparison between quantum and classical drain current affirms the fact that threshold voltage is elevated under quantum confinement. The present analysis also predicts that, the implementation of this model in practice will be able to offer superior current voltage characteristics compared to that of DMG structures.

The proposed structure is applied and used for Boolean implementation as **AND gate** and as an **Inverter**. Thus, universal NAND gate is obtained. In normal scenario, to construct AND gate 6 transistors are required, using the proposed structure it is seen that only 1 PMOS structure exhibits the function of AND.

Future Aspects

In the future scope of work, it can be examined whether the problems that is generally faced in deep sub- micron technology such as supply voltage scaling, short channel effects can be limited due to the mentioned advantages of DGMOSFET. The present model describes a compact quantum analytical model for drain current in DG MOSFET structure. It is reasonable and adequate enough to predict electric field, current voltage and voltage gain characteristics. However, the following issues are excluded in this model for the sake of simplicity:

- The expressions in the model have been derived using 2D Poisson equation and 1D Schrödinger equation. 3D Poisson equation along with 2D Schrödinger

equation can be solved self-consistently to verify the overall potential charge profile even more accurately.

- In this model, the concept of DG MOSFET is used in the structure. Another novel structure may be proposed using DMG MOSFET in the back and front gate.
- To incorporate the quantum confinement effects more accurately in the model, inter sub-band scattering can be considered, when the higher sub-bands in the potential wells are expected to be populated.
- The idea of work function engineering can be extended to "spatially graded binary metal gates" for this DG structure as well as the scope of it can be examined in the DMG structure.
- Here the DG MOSFET structure has been applied as an AND gate, in future it is to be seen whether the DMG MOSFET or tunnelling effect can be used to harness more effectively the Boolean applications.

CHAPTER-6

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