Analytical Model of the 2-D Electron Gas Density (2DEG) of a Dual Channel MOS-HEMT

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MASTER OF TECHNOLOGY IN VLSI DESIGN AND MICROELECTRONICS TECHNOLOGY

BY

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CERTIFICATE OF EXAMINATION

This is to certify that **Tapanika Pal** has satisfactorily completed the thesis entitled **"Analytical Model of the 2-D Electron Gas Density (2DEG) of a Dual Channel MOS-HEMT"** under the guidance of **Dr**. **Chandrima Mondal**, Department of Electronics and Telecommunication Engineering, Jadavpur University. We recommend that her dissertation is fully adequate in scope and quality for the partial fulfillment of the requirement for the degree of **MASTER IN TECHNOLOGY INVLSI AND MICRO ELECTRONICS ENGINEERING,** in the Department of Electronics and Telecommunication Engineering, Jadavpur University,Kolkata-700032.

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This is to certify that the Master Thesis entitled "**Analytical Model of the 2-D Electron Gas Density (2DEG) of a Dual Channel MOS-HEMT**" is hereby approved as a creditable study of an engineering subject carried out and presented in a manner satisfactory to warrant its acceptance as prerequisite to the degree for which it has been submitted. It is understood that by this approval the undersigned do not necessarily endorse or accept every statement made, opinion expressed or conclusion drawn therein but approve the thesis only for the purpose for which it has been submitted.

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DECLARATION OF ORIGINALITY AND COMPLIANCE OF ACADEMIC ETHICS

I hereby declare that the M.Tech thesis entitled "**Analytical Model of the 2-D Electron Gas Density (2DEG) of a Dual Channel MOS-HEMT**" submitted to Faculty of Engineering & Technology, Jadavpur University as part of partial fulfilment of degree of Master of Technology in VLSI Design and Microelectronics Technology is an original work carried out by undersigned. All information in this document have been obtained and presented in accordance with academic rules and ethical conduct. The matter embodied in this project is a genuine work done by the undersigned and has not been submitted to any other University/Institute for the fulfilment of the requirement of any course of study.

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CHAPTER-1

1. INTRODUCTION

In 1947, invention of the transistor became a major achievement for the evolution of Modern electronics. Transistors are the unavoidable key component of all most all electronic circuits. Later on, semiconductor industry needed mass production of highly efficient transistor circuits. So the researchers tried to explore the study of new material system rather than the conventional one. If we produce higher performance transistor, we can achieve more energy efficient and more reliable system and can reduce product volume as well.

In 1979, Invention of "GaAs", as "high electron mobility transistor" was a very big breakpoint of electronic history [1]. HEMT was offering very high sheet carrier density and mobility.

GaN, a wide band-gap III-V compound is the latest invention for the high power applications. In 1994, first AlGaN/GaN HEMT is found by Khan *et all* [2].

1.1GaN High Electron Mobility Transistor:

GaN HEMT has been very promising research topic for its superior properties over the conventional transistor. As GaN is a wide band gap semiconductor material, it can stand at very extreme environment such as high temperature and voltages. Radiation hardness of GaN is comparable with SiC and higher than GaAs. Some important properties of GaN are listed below in Table 1.

property	Si	GaAs	4H-SiC	6H-SiC	GaN
Bandgap(eV)	1.12	1.42	3.47	3.02	3.4
Breakdown Electric field (MV/cm)	0.3	0.4	3	3.2	3.3
Relative Dielectric Constant	11.7	12.9	9.7	9.66	8.9
Thermal Conductivity k, (W/cm-K)	1.3	0.55	3.7	4.9	1.3
Electron Mobility μ_n, (cm^2/V-s)	1400	8500	900	400	1000
Hole Mobility	450	400	120	90	200

(cm^2/V-s)					
Saturated Electron Drift Velocity(x10^7 cm/s)	1	1	2	2	2.5
Melting Point, K	1415	1238	2827		2791

Table 1: Important properties of different semiconductor material

Two types of structures are popular for GaN HEMT: lateral structure and Vertical structure. For lateral structure AlGaN/GaN HEMT are the most promising device of Power application, as shown in Figure 1.

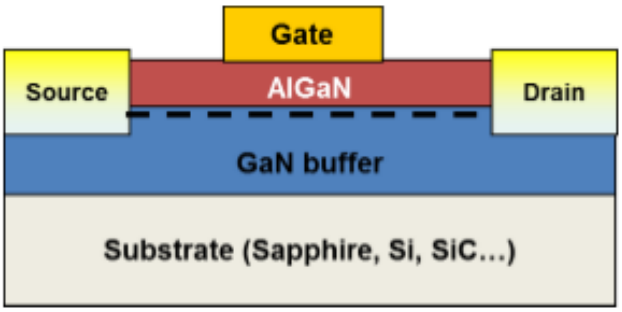

Figure 1.1: A typical lateral AlGaN/GaN HEMT

This structure generates a Two dimensional Electron Gas (2DEG) at AlGaN/GaN interface of an AlGaN/GaN heterostructure. AlGaN/GaN heterostructure has very high electron mobility(~ 2000 cm^2/Vs). Due to strong polarization effect (piezoelectric and spontaneous) in group III- nitride materials a high sheet charge density (higher than 1x10^{13} cm^{-2}) occur in AlGaN/GaN structure. Due to high charge carrier density and high electron mobility AlGaN/GaN HMET has low on-Resistance.

As Wide Band gap material and high electric field of GaN allows high break down voltage of AlGaN/GaN HEMT. Theoretical value of Breakdown Voltage(V_B) and On Resistance(R_{on}) is calculated Using the equation:

$$R_{on} = \frac{V_B^2}{\mu_c \epsilon_s {E_c}^3}$$

Where μ_c is the channel mobility and E_c is critical electric field.

At the same time, Vertical structure is also very use full for low on Resistance and Power applications. A vertical structure is shown in Figure 2.

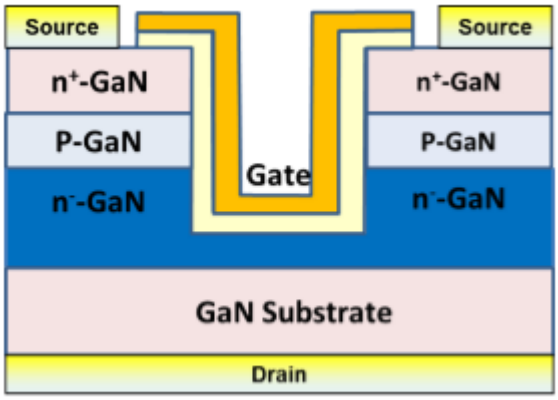

Figure 1.2: A power device structure -- GaN vertical MOSFET

Some variations are there in both Vertical and Lateral structure but a basic difference in unchanged which is in vertical structure current flows vertically where in lateral structure current flows near the surface.

There are some basic advantages and disadvantages of lateral device as compared to vertical structure which are as follows:

Advantages:

1) Lateral devices are formed of un-doped AlGaN/GaN, so it has Low parasitic capacitance .Due to 2DEG formation device has low conductance losses and low switching losses.

2) Fabrication process of Lateral structure is also simpler than vertical devices. Therefore simple fabrication of more complex device can be possible using lateral structure. And Si also can be used for growth of the lateral HEMT.

3) Bi-directional switching can be obtained very easily using Lateral GaN HEMT.

Disadvantages:

1) The high breakdown voltage for lateral HEMTs leads to an increase of distance between gate and drain areas, the chip size will be larger. On the other hand, the increase of breakdown voltage in vertical structures will increase the thickness of the buffer layer. Vertical structures have the higher power density over lateral HEMT for high breakdown voltage devices.

2) As current flows laterally in the lateral HEMT devices, the resistance and the current capacity of the electrodes puts restrain on the device performances.

3) In lateral HEMT, current flows near the surface compared to the bulk region in vertical devices, so the current collapsing and increase in dynamic on resistance is more serious in lateral HEMT.

1.2 Hetero-Structure Fundamentals:

Energy Bands in Abrupt Heterojunctions: Heterojunction pairs, which is illustrated in Fig 3, is called type I heterojunctions. Here both the conduction band and the valance band of the smaller band gap semiconductor lie completely inside the band gap of wider band gap semiconductor. To form "Heterojunction Pairs of group III-V" compounds , either band-gap of the group III or group V element differs to form type I heterojunctions. Examples are AlGaAs/GaAs, and AlGaN/GaN heterojunctions.

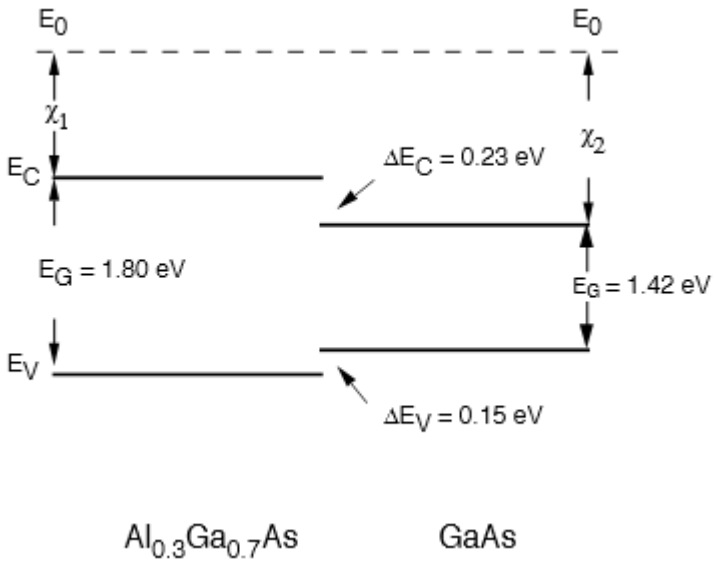

Fig 1.3: Type I heterojunctions.[3]

From Fig 3,

$$\Delta E_c = \chi_2 - \chi_1$$

This is known as "Electron affinity Rule". For this kind of Heterojunction it is also apparent,

$$\Delta E_G = \Delta E_c + \Delta E_v$$

Figure 4 shows Type III heterojunctions(also known as type II misaligned heterojunction),here group III and group V differ (e.g. GaSb/InAs) to form type III heterojunction. In this type, conduction band of one semiconductor is below the valance band of another semiconductor. Transport is challenging in this case because, as electrons pass the heterojunction, their wave

function switches from that of an electron to that of a hole. The interface is known as a type II interface (also known as type II staggered heterojunction).if there is less electron affinity difference such that the conduction and the valence bands of the smaller band gap semiconductor cross across the valence band of the larger band gap semiconductor. Examples are In_xGa_1-xAs / Ga_xSb_1-xAs and AlxIn1-xAs / InP systems.

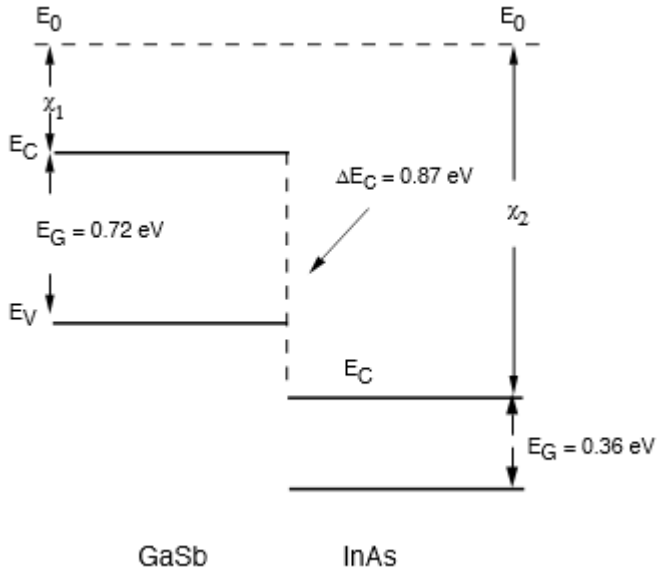

Fig 1.4:Type III heterojunctions, also known as Type II misaligned heterojunctions,.[3]

1.3 GAN BASED ENHANCEMENT-MODE DEVICES:

Because of their normally-off and high power switching capabilities at RF frequencies, Enhancement mode GaN devices are in high demand in electronics market. Here we will explain the technologies which are presently used to fabricate Enhancement mode Devices.

1.3.1 Barrier Thinning Using Etching Techniques:

One of the most easy and common way to achieve E-Mode operation to from the conventional AlGaN/GaN structure is, thinning the barrier layer, till it reaches the critical thickness and channel acts as an open circuit under the Gated region and that enables the normally off operation. The basic of this technique is, it doesn't produced 2DEG formation below a certain barrier thickness, which is commonly known as critical barrier thickness (t_{cr}).

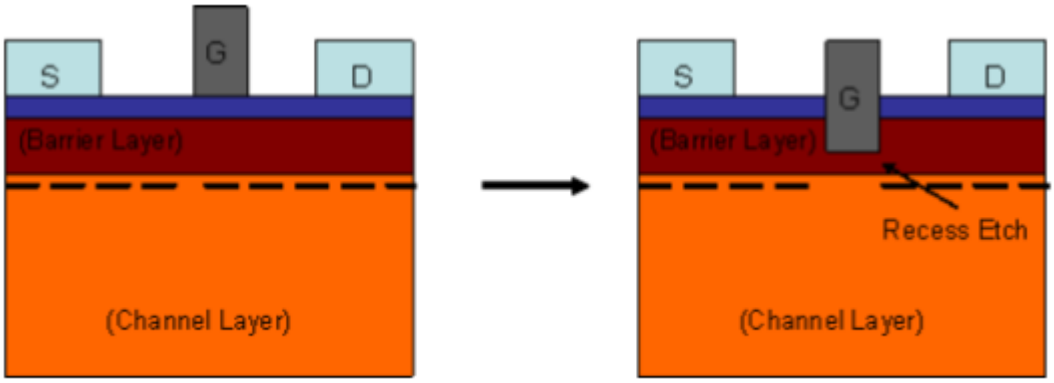

Fig 1.5: E-mode or normally-off operation using recess etching technique.[4]

Generally etching of the barrier is done under the gated region using an etch-resistant mask material like SiO_2 or SiN etc. The process will continue upto the thickness, when it becomes equal or less than the critical barrier thickness so that there is no such formation of the 2DEG under the gated region.

1.3.2 Double HEMT Structure With Etch-Stop Layer:

Hetero-structures with two active barrier layers are used in the etch-stop layer method for making E-Mode devices. Until the etch-stop layer is reached, the top active layer can be selectively etched using dry or wet etching methods. The 2^{nd} layer is this etch-stop layer. The same basic idea is used in this technique to create E-Mode devices. The etch stop layer's thickness is below the critical thickness needed for 2DEG to develop at the interface. Once it reaches the etch-stop layer, the etching operation will come to an end.

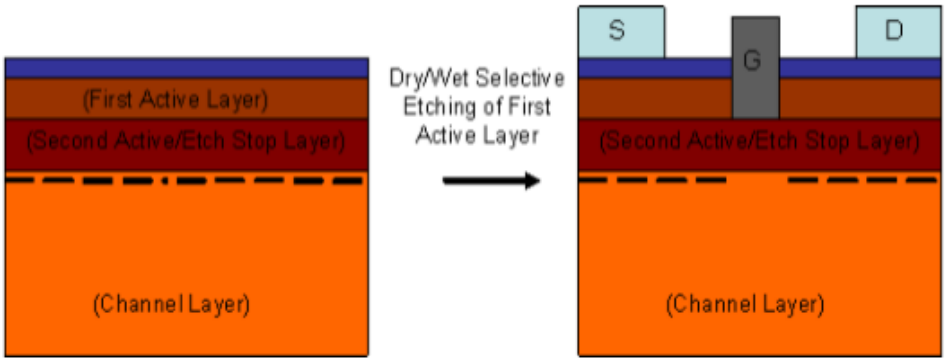

Fig 1.6: E-mode operation using selective barrier etching technique.[4]

The main disadvantages of the etch-stop layer fabrication technique is that it lacks variability in options of the layer structure. In the family of GAN semiconductors only Aluminium Nitride (AlN) can be selectively and chemically etched using warm (>60˚C) AZ400K developer solution over

other III-N materials, which limits the device structure to make only AlN as the top active layer. And on the other side procedures involves dry recess etching technique for the etch-stop layer, which is only limited to Indium (In) related chemistries, such as InN, InGaN or InAlN as they require a very high table-temperature for etching.

1.3.3 Fluorine Ion Implantation Technique:

Ion implantation is a technique in which ions from one material are inserted into another, altering the latter's material properties. This procedure calls for an ion source to produce the appropriate ions, which are then accelerated at high voltage to interact with the target material. Currently, very negative Fluorine (F) ions are used in a confined ion implantation approach to produce GaN-based E-Mode devices. Fluorine ions are implanted in the barrier layer using a high-energy source.

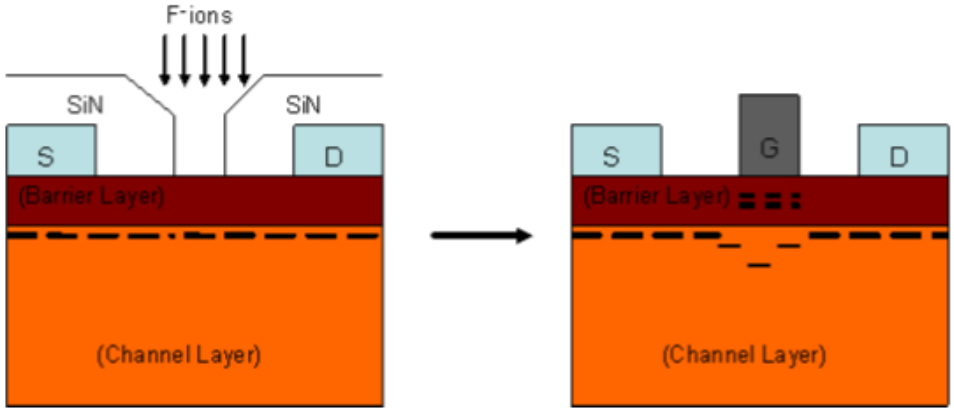

Fig 1.7: E-mode operation using Ion Implantation technique[4]

This process eliminates the dry etch problems incurred from recess RIE technique. But the implanted Fluorine ions have tendency to move around inside the GaN crystal lattice, which makes the devices very unstable and also degrades the drain breakdown voltage of the devices and hence reliability issue occurs.

1.3.4 P-Type Doping:

In this method, an Undoped AlGaN/GaN structure is placed over a Mg doped (p-type) AlGaN or GaN based layer to produce a p-n diode underneath the Gated area. In order to achieve normally-off operation, the p-type layer raises the channel's potential by producing the p-n junction, which results in a depletion zone beneath the channel. With the increase of the gate voltage in the positive

direction the diode starts to operate in forward bias allowing injection of holes in the barrier layer, which in turn attracts a lot of free electrons at the channel and allows conduction.

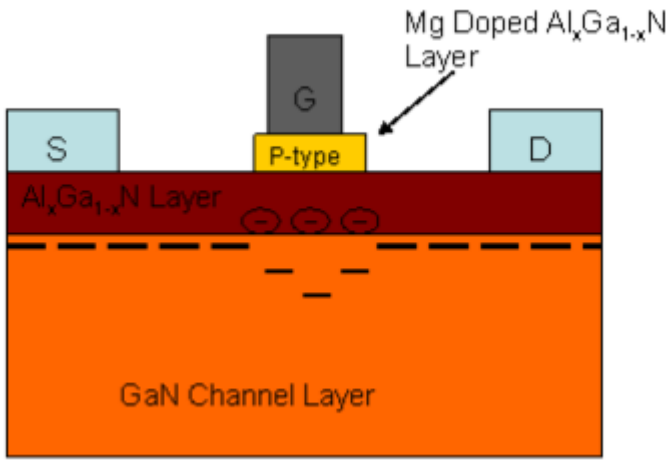

Fig 1.8: E-mode operation using P-Type doped localized barrier layer[4]

The main disadvantage of this method is the need to selectively develop or etch the p-type layer in order to make the p-type AlGaN or GaN layer behind the gate. It can be difficult to selectively grow another layer on top of the sample after growth because there is a significant risk of contaminating the growth chamber. Furthermore, since adequate etch recipes for specifically etching p-type AlGaN or GaN films are not easily accessible, controlling the etch depth is practically difficult.

CHAPTER-2

2.1 LITERATURE SURVEY:

A "GaN-based field effect transistor" (FET) on a "silicon substrate" is a promising device for next-generation power devices because of its high breakdown electric fields and inexpensive substrate. Because of high carrier mobility of two dimensional electron gases (2DEG) at the hetero interface, it is anticipated that GaN FETs adopting an AlGaN/GaN hetero-junction structure will attain the low-power-loss and high-speed switching performance. For power electronics applications, a normally-off operation and a low on resistance is strongly required to replace Si-based power devices such as metal-oxide semiconductor field effect transistor(MOSFET) and Insulated gate bipolar transistors(IGBTs).

NORMALLY-OFF power transistors are particularly important for power switching applications.To create normally-off GaN power switching devices, a number of methods have been suggested, including the p-cap gate [5], [6], fluorine plasma ion implantation [7], the recessed gate [8], etc. Because the MOS-gate is compatible with the common gate driver ICs [9], [10], MOS-HEMTs with partially or totally recessed gates are regarded as a potential candidate among them. Although Fully recessed gate has a greater positive V_{th} and better process tolerance than a partially recessed gate, the fully recessed gate construction is preferred despite of having a high MOS-channel resistance.

In paper [11] Al_2O_3/GaN MOSFETs are typically made using a straightforward postgate-recess tetramethyl ammonium hydroxide (TMAH) procedure. With the"gate length" of 2.5 µm, the TMAH-treated device displayed outstanding device performances, including a "threshold voltage" of 3.5 V, a maximum "drain current" of 336 mA/mm, and a "breakdown voltage" of 725 V, as well as an incredibly small gate leakage current of about 109 A/mm at V_{gs} = 15 V, which is roughly six orders lower in scale than that of the device without TMAH treatment.

In paper[12],inside a high-performance normally-off Al_2O_3/AlN/GaN MOS-channel-high electron mobility transistor (MOSC-HEMT) , a "monocrystalline AlN interfacial layer" is added between the "amorphous Al_2O_3 gate dielectric" and the "GaN" channel. As a result of the AlN interfacial layer, the GaN surface is well shielded from oxygen, and harmful Ga-O bonds are not formed. Due to increased interface quality, "frequency-dispersion" in C-V characteristics and "threshold voltage hysteresis" are successfully controlled. The new MOSC-HEMTs have minimal dynamic ON-resistance degradation, a "high ON/OFF drain current" ratio of 1010, a "maximum drain current" of 660 mA/mm, and "field effect mobility" of 165 cm^2/V-s.

Even after significant improvements to maximize the recess process and because of careful design of the interface, the decreased channel mobility brought on by etching-induced damage and the poor "dielectric/GaN" interface quality when compared to the heterojunction-interface are to reason for this high resistance. As a result, new methods are preferred to produce low on-resistance, normally-

off MOS-HEMTs. To realize a “recessed gate normally-off GaN FET with high threshold voltage” (V_{th}) uniformity and low on-resistance, a novel PNT (piezo neutralization technique) structure was proposed [13].Figure 2.1, shows the “schematic” cross-sectional view of the developed “GaN metal-insulator-semiconductor field effect transistor (MISFET)” with the proposed PNT structure.

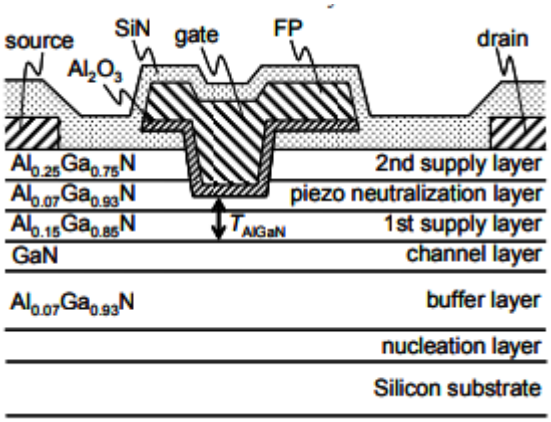

Fig 2.1:The cross-sectional view of the normally-off GaN MISFET with a piezo neutralization (PNT) structure.[13]

In this paper,they have effectively established a recessed gate normally-off GaN FET which has “high threshold voltage” (V_{th}) and “low on-resistance” on a silicon substrate. A novel V_{th} control strategy, which we refer to as the "piezo neutralisation technique," is suggested in order to achieve high V_{th} consistency. This method includes the formation of a piezo neutralisation (PNT) layer at the base of the “gate recess”. The polarisation charges underneath the gate are neutralised by the PNT layer, and thus V_{th} is unaffected by gate-to-channel span. The produced “normally-off GaN FET” with “PNT structure” exhibits an extraordinary V_{th} uniformity ((V_{th})=18 mV), an advanced combination of the specific on-resistance and the “breakdown voltage” (V_B>1000 V).The “normally-off GaN FETs” with PNT structure demonstrate excellent potential as power devices.

In addition, great care must be taken for the recess depth because even a small over-etch (by a few nanometres) can cause an interruption between the 2DEG access areas and the MOS-channel because of the “high parasitic resistance” at the “gate-recess corners”. New methods are therefore needed to produce “low on-resistance E-mode MOS-HEMTs” with reliable gate recess control.

In paper [14] an “E-mode GaN double-channel MOS-HEMT” (DC-MOS-HEMT) is proposed. The device has a “lower heterojunction channel” spaced a few nanometers below the upper MOS channel. At zero gate bias both channels are pinched off as the gate recess terminates at the top channel, enabling E-mode operation. The bottom channel's “high electron mobility” is preserved since it is separated from the etched GaN surface. The DC-MOS-HEMT produces a “positive threshold voltage”, a sharp sub-threshold swing, a low on-resistance with a high breakdown voltage, and negligible dynamic R_{on} degradation. The device's performance exhibits greater process tolerance since it is less sensitive to the recess depth.

The DC-MOS-HEMT has strong control over the gate recess depth due to the 6-nm GaN top channel layer. As long as the etch stops in the upper GaN channel layer, V_{th} is unaffected by the depth of the recess, because of the conduction band of the upper channel is flat at the pinch-off state, which causes V_{th} to be lowered by a small amount of 17.4 mV for every 1-nm over etch.

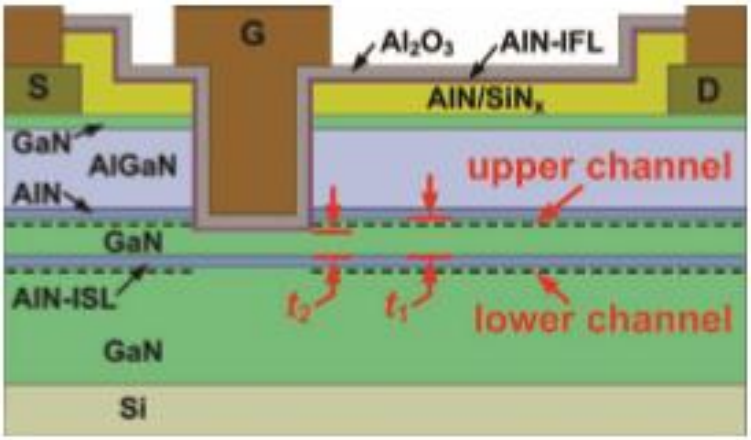

Fig 2.2: Construction of the DC-MOS-HEMT, Which have an upper MOS-channel layer and a lower heterojunction channel layer. The barrier consists GaN(cap)/AlGaN/AlN (3/17/1.5 nm). The AlN insertion layer (ISL) is 1.5 nm. An ultrathin PEALD AlN interfacial layer (IFL) and 18 nm Al_2O_3 are used as gate dielectric.[14]

In paper [15],they have discovered that without careful consideration of the electrical coupling between the two channels, the double-channel construction can't have a low R_{on} . A high channel-to-channel (C2C) coupling between the two channels is necessarily required to reduce R_{on} in the DC-MOS-HEMT by utilising both channels at the access region and allowing currents to merge into the hetero-junction lower channel at the gate area. Apart from that, with a weak C2C coupling, the high-resistivity MOS-channel segment at the gate area prevents conduction across the upper channel. The manufactured DC-MOS-HEMT has a significantly lower R_{on} than that with a C2C distance (t_{c2c}) of 11.5 nm. Further investigation demonstrates that when compared to the "sheet resistance" of the DC-heterostructure itself, the latter has higher sheet resistance at the access area. For the purpose of analysing the C2C coupling in the DC-heterostructure, a modified TLM characterisation is suggested. For the purpose of analysing the "C2C coupling" in the DC-heterostructure, a modified TLM characterisation is put forth. The DC-heterostructure with t_{c2c} = 7.5 nm has strong C2C coupling, whereas that with t_{c2c}= 11.5 nm has comparatively poor C2C coupling, it has been confirmed.

It is important to create analytical models of the device since they can be used to guide device design and provide physical insights into the DC-MOS-operating HEMT's mechanism. Despite being widely established, analytical modelling of the charge distribution and gate control in "GaN single-channel HEMTs" in [16]-[19].

CHAPTER-3

3.1 DUAL CHANNEL-MOSHEMT

In the concerned study, we have discussed the analytical modelling of DC-MOSHEMT. The systemic analytical investigation is performed for the mentioned structure. The main attribute of this heterostructure is the presence of AlN-ISL layer. Table 2 is containing the measurement, used to model the structure.

$t_{AlN\text{-}ISL}$	Thickness of AlN-ISL	1.5 nm
t_{ua}	Thickness of upper channel at access region	variable
t_{ug}	Thickness of upper channel at gated region	variable
$t_{AlN\text{-}MEL}$	Thickness of AlN-MEL	1.5 nm,3nm,4.5nm,6nm
t_{AlGaN}	Thickness of AlGaN Barrier	17 nm
X_{AlGaN}	Al composition of AlGaN Barrier	0.25
$t_{GaN\text{-}Cap}$	Thickness of GaN cap	3nm
t_{Al2o3}	Thickness of Al_2O_3 gate dielectric	18nm
n_{buf}	Density of space charge in the buffer	$0.6x10^{12}$ Cm^{-2}
n_{it}	Density of effective interface charges	$1.5x10^{13}$ Cm^{-2}
ϕ_{acc}	Surface barrier height at access region	0.7 eV
ϕ_G	Surface barrier height at gated region	3.47 eV

Table 2: The main parameter as applied in the paper

As shown in the Figure 3.1, on a silicon substrate, the "double-channel heterostructure" is made up of a barrier layer, a GaN upper channel layer, an AlN-ISL, and a GaN buffer/transition layer. AlGaN, GaN cap, and AlN mobility enhancement layers(AlN-MEL) make up the barrier layer in addition. The main parameters are used in the paper, are listed above in the Table 2. And Default values are assigned using [20],[21].The thicknesses of the "upper channel layer" in the access region (t_{ua}) and in the "gated region" (t_{ug}) are prone to change.

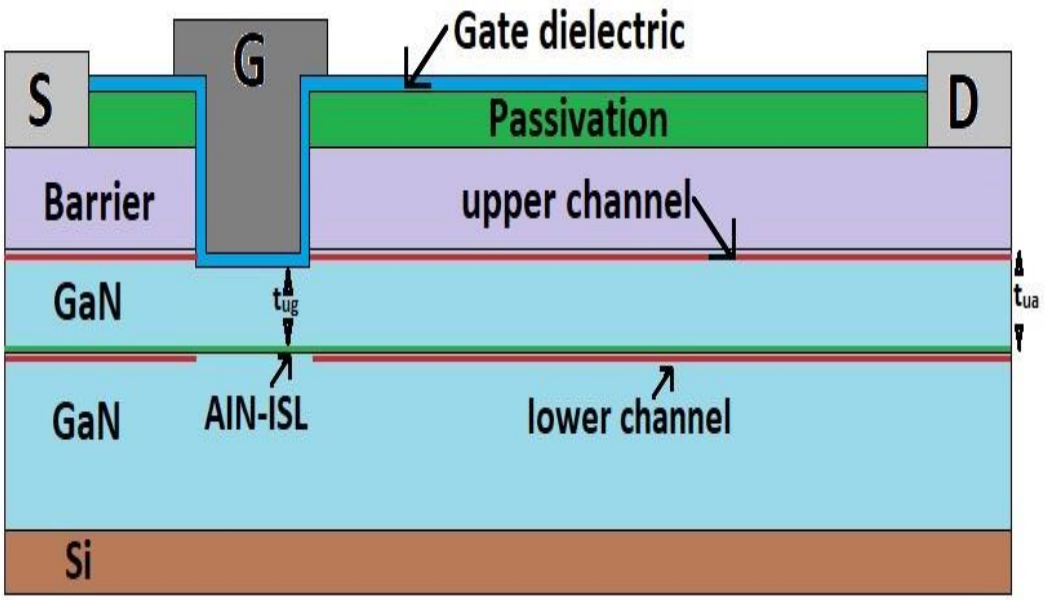

Fig 3.1. :Double channel MOS_HEMT

3.2 DEVICE STRUCTURE AND OPERATING MECHANISM:

The 4-inch Si substrate was used to create the experimental DC-HEMT wafer by MOCVD. It included a barrier made up of a 3-nm GaN cap, a 17-nm AlGaN layer, and a 1.5-nm AlN insertion layer (ISL), as well as 6-nm GaN upper channel and 4µm GaN buffer/transition layers (Figure 3.1).Due to the strong polarisation of AlN- ISL, a lower channel forms at the junction with the underlying GaN, while the "2DEG density in the upper channel" decreases. A recess depth of approximately 23 nm is attained in the "gate region". This shows that the barrier has been completely removed, along with 1.5 nm of the "upper channel" layer in GaN. To assure thorough removal of the "barrier layer", a 1.5-nm over-etch was carried out.

When V_{gs}= 0V, both channels are pinched off. With the V_{gs}=2V, lower channel is turned on, while upper channel is still off. With the increase of the gate voltage, a larger voltage of V_{gs}=6V made upper channel on. As long as the etching process stops inside the upper GaN channel layer, it is anticipated that the threshold voltage of the DC-MOS-HEMT will be unaffected by the over-etch depth. According to simulations, V_{th} is decreased by a negligible amount of 17.4 mV for every 1-nm over-etch because the electrical field of the GaN layer is weak when the device is close to pinch off.

3.3 DEVICE FABRICATION AND CHARACTERIZATION:

According to Hall measurements, the as-grown wafer has an overall 2DEG density of $8.6x10^{12}$ cm^{-2} and a channel mobility of 2080 $cm^{2/}$(V-s).The evaporation of Ti, Al, Ni, and Au was the first step in the fabrication process. A 30-second quick thermal annealing step at 850 ℃ in $N_2$was then performed. For the passivation layer, a stack of AlN/SiNx (4/50 nm) was deposited using PEALD/PECVD. Planar isolation was then achieved through the implantation of fluorine ions. The gate recess was created using a hybrid dry-/digital-etching method that involved removing the

passivation layers in the gate window using ICP, followed by 5 cycles of plasma-oxidation/HCl-dip digital etching to remove a thin surface layer that had been exposed to plasma during the dry etch. To remove the native oxide, an *in situ* remote plasma pre-treatment was used in the PEALD chamber. Next, an ultrathin AlN and 18-nm Al_2O_3 as the gate dielectric were deposited, with the "AlN interfacial layer" (IFL) being added to help suppress the interface traps. To improve the standard of the gate dielectric, a subsequent post-deposition anneal was performed at 500 ℃ in an oxygen environment. To finish the transistor fabrication flow, a Ni/Au metal gate was deposited and patterned. The ohmic contact resistance was calculated using the "transfer length method" (TLM) and was found to be 0.58 Ω- mm, slightly higher than the value seen in a single-channel control sample(0.52 Ω-mm).In C-V characteristics, two rising edges are noticed and linked to the emergence of the upper MOS-channel and the lower heterojunction channel, much like the Schottky diode. A high-quality MOS interface is indicated by both the low G/ω values and the minimal frequency dispersion.

Analytical modelling of the device is important to fulfil the ultimate prospect of the "DC-MOS-HEMT" since it offers physical insights into how it works and provides direction for device design. Despite being widely established, analytical modelling of the "charge distribution" and "gate control" in "GaN single-channel" HEMTs in [16][19].In this article, the DC-MOS-HEMT is the subject of a rigorous analytical analysis.

3.4 ANALYTICAL MODEL OF DC-MOSHEMT

3.4.1. Analytical Expressions in Double - Channel MOSHEMT:

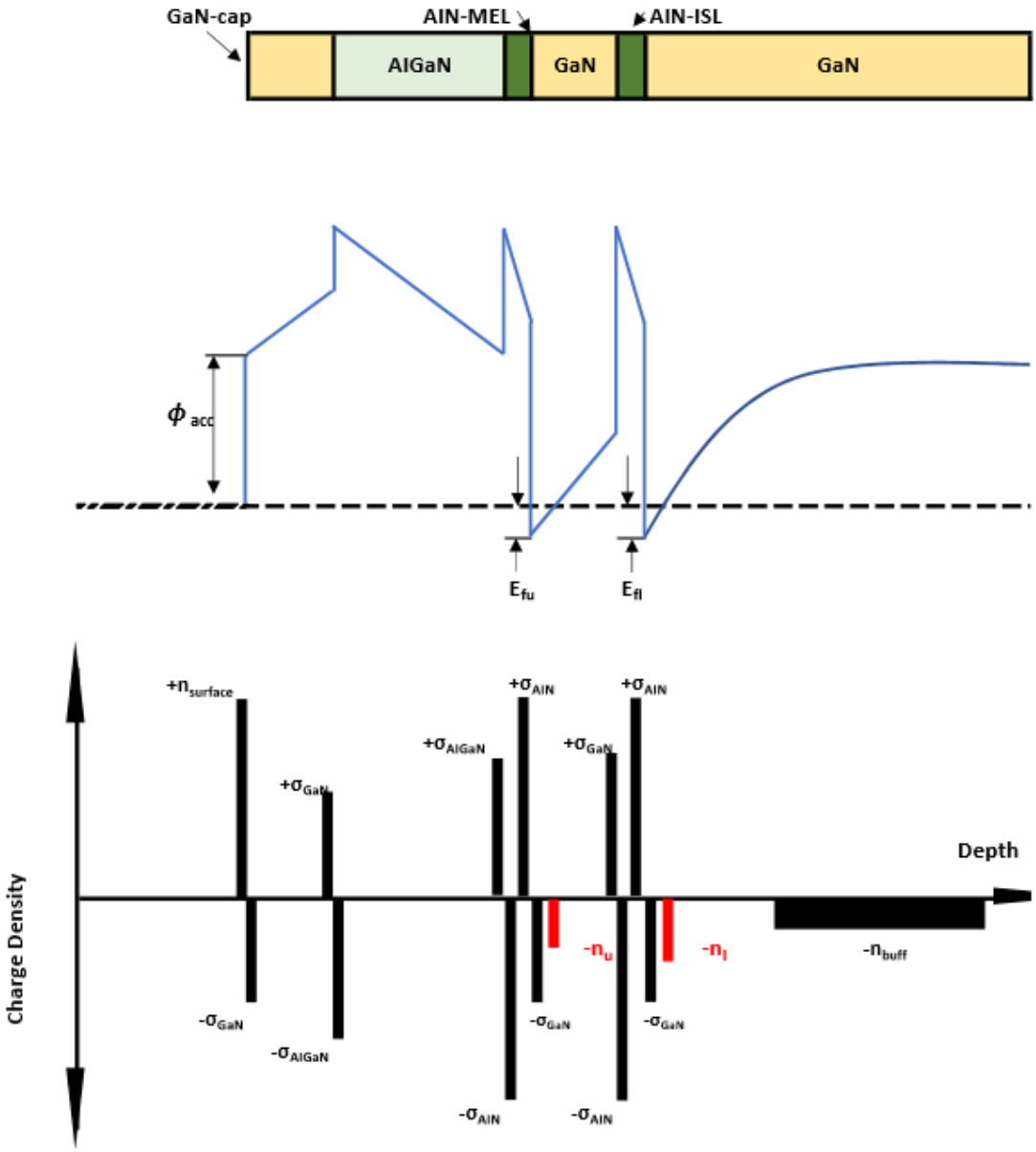

Figure 3.2. . "Conduction band" diagrams and "charge distributions" at the access region of the DC-MOS-HEMT. The surface barrier (φ_{acc}) can be determined by where the Fermi level is pinned. n_{it} is the density of ionized surface/interface traps. There is a critical thickness of the upper channel layer $t_{ua\text{-}crit}$. When $t_{ua} > t_{ua\text{-}crit}$, two channels exist.

Applying Gauss's Law from the lower channel to the upper channel, we obtain

$$-E_{fl} + \Delta Ec_{-AlN/GaN} + \frac{q^2(\sigma_{AlN}-\sigma_{GaN}-n_l-n_{buf})}{\epsilon_{AlN}}.t_{AlN-ISL} - \Delta Ec_{-AlN/GaN} + \frac{q^2(-n_l-n_{buf})}{\epsilon_{GaN}}t_{ua} + -E_{fu} = 0$$

or

$$(n_l)\left\{\frac{(-q^2)}{\epsilon_{AlN}}(t_{AlN-ISL}) - \frac{q^2}{\epsilon_{GaN}}(t_{ua})\right\} + (n_{buf})\left\{\frac{-q^2}{\epsilon_{AlN}}(t_{AlN-ISL}) - \frac{q^2}{\epsilon_{GaN}}t_{ua}\right\} = -E_{fl} + -E_{fu} + \left\{\frac{q^2\sigma_{GaN}}{\epsilon_{AlN}}.t_{AlN-ISL}\right\} - \{\frac{q^2\sigma_{AlN}}{\epsilon_{AlN}}.t_{AlN-ISL}\}$$

or

$$\left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-ISL} - \frac{q^2}{\epsilon_{GaN}}t_{ua}\right)(n_l + n_{buf}) = -E_{fl} + E_{fu} + \{\frac{q^2(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}}.t_{AlN-ISL}\}$$

or

$$n_l = \left[\frac{\left\{\frac{q^2(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}}t_{AlN-ISL}+E_{fu}-E_{fl}\right\}}{\left\{\left(\frac{q^2}{\epsilon_{GaN}}.t_{ua}\right)+\left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-ISL}\right)\right\}}\right] - n_{buf} \quad \text{.....(1)}$$

Where, n_l is the "2DEG Density" in lower channel. The Fermi energies E_{f1} and E_{fu} are defined as the energy differences between the "Fermi level" and the conduction band minimum at the lower and upper channels, respectively.

Again Gauss's Law is applied from the upper channel to the surface of the GaN cap layer,

$$-E_{fu} + \Delta Ec_{-AlN/GaN} + \frac{q^2(\sigma_{AlN}-\sigma_{GaN}-n_l-n_u-n_{buf})}{\epsilon_{AlN}}t_{AlN-MEL} - \Delta Ec_{-AlN/AlGaN} + \frac{q^2(\sigma_{AlGaN}-\sigma_{GaN}-n_l-n_u-n_{buf})}{\epsilon_{AlGaN}}.t_{AlGaN} - \Delta Ec_{-AlGaN/GaN} + \frac{q^2(n_l-n_u-n_{buf})}{\epsilon_{GaN}}t_{GaN-cap} - \varphi acc = 0.$$

Since, $\Delta E_{cAlGaN/GaN} = \Delta E_{c\ AlN/GaN} - \Delta E_{c\ AlN/AlGaN}$

$$(-n_l - n_u - n_{buf})\{\left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-MEL}\right) + \left(\frac{q^2}{\epsilon_{AlGaN}}.t_{AlGaN}\right) + \left(\frac{q^2}{\epsilon_{GaN}}.t_{GaN-Cap}\right) = E_{fu} + \varphi acc - \left[\frac{q^2(\sigma AlN-\sigma GaN)}{\epsilon_{AlN}}.t_{AlN-MEL}\right] - [\frac{q^2(\sigma AlGaN-\sigma GaN)}{\epsilon_{AlGaN}}.t_{AlGaN}]$$

Or

$$n_u = \frac{\left\{\left(\frac{q^2(\sigma AlN-\sigma GaN)}{\epsilon_{AlN}}.t_{AlN-MEL}\right)+\left(\frac{q^2(\sigma AlGaN-\sigma GaN)}{\xi AlGaN}.t_{AlGaN}\right)-E_{fu}-\varphi acc\right\}}{\{\frac{q^2}{\epsilon_{AlN}}.t_{AlN}+\frac{q^2}{\epsilon_{AlGaN}}.t_{AlGaN}+\frac{q^2}{\epsilon_{GaN}}t_{GaN-cap}\}} - n_l - n_{buf} \text{.....(2)}$$

Where, n_u is the 2DEG Density in upper channel.

3.4.2 . <u>Critical Thickness for the Upper Channel</u>:

From equation (1) and (2), $n_t(=n_l + n_u)$ is independent of t_{ua}. In contrast, a smaller t_{ua} directs more electrons to the lower channel, as

$E = \frac{V}{d}$, as the electric-field rises, the charge density will increase in the channel and vice versa. The "2DEG" in the upper channel disappears and just the lower channel remains when t_{ua} falls to a critical value, $t_{ua\text{-}crit}$. So, when $t_{ua}=t_{ua\text{-}crit}$, $n_u=0$ and $E_{fu}=0$,

Now the "2DEG Density" in the lower channel is,

From equation (2),

$$n_l = \frac{\left\{\left(\frac{q^2(\sigma AlN-\sigma GaN)}{\epsilon_{AlN}}.t_{AlN-MEL}\right)+\left(\frac{q^2(\sigma AlGaN-\sigma GaN)}{\epsilon_{AlGaN}}.t_{AlGaN}\right)-E_{fu}-\varphi_{acc}\right\}}{\left\{\frac{q^2}{\epsilon_{AlN}}.t_{AlN}+\frac{q^2}{\epsilon_{AlGaN}}.t_{AlGaN}+\frac{q^2}{\epsilon_{GaN}}t_{GaN-cap}\right\}} - n_{buf} \quad \text{.....(3)}$$

To find out the critical thickness of the tua, From equation (1)

$$n_l = \left[\frac{\left\{\frac{q^2(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}}t_{AlN-ISL}+E_{fu}-E_{fl}\right\}}{\left\{\left(\frac{q^2}{\epsilon_{GaN}}.t_{ua}\right)+\left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-ISL}\right)\right\}}\right] - n_{buf}$$

Here, $E_{fu}=0$,so

$$\left(n_l + n_{buf}\right)\left(\frac{q^2}{\epsilon_{GaN}}t_{ua-crit} + \frac{q^2}{\epsilon_{AlN}}t_{AlN-ISL}\right) = \left[q^2\frac{(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}}t_{AlN-ISL} - E_{fl}\right]$$

Or

$$\left(n_l + n_{buf}\right)\left(\frac{q^2}{\epsilon_{GaN}}t_{ua-crit}\right) = \left[\left(q^2\frac{(\sigma_{AlN}-\sigma_{GaN}-n_l-n_{buf})}{\epsilon_{AlN}}t_{AlN-ISL}\right) - E_{fl}\right]$$

Or

$$t_{ua-crit} = \frac{\epsilon_{GaN}}{q^2(n_l+n_{buf})}\left[\frac{q^2(\sigma_{AlN}-\sigma_{GaN}-n_l-n_{buf})}{\epsilon_{AlN}}t_{AlN-ISL} - E_{fl}\right] \quad \text{.....(4)}$$

Here After putting all the values from Table 2, we obtain $t_{ua\text{-}crit}$=2.7 nm.

3.4.3. 2DEG Density When Only Lower Channel Exists:

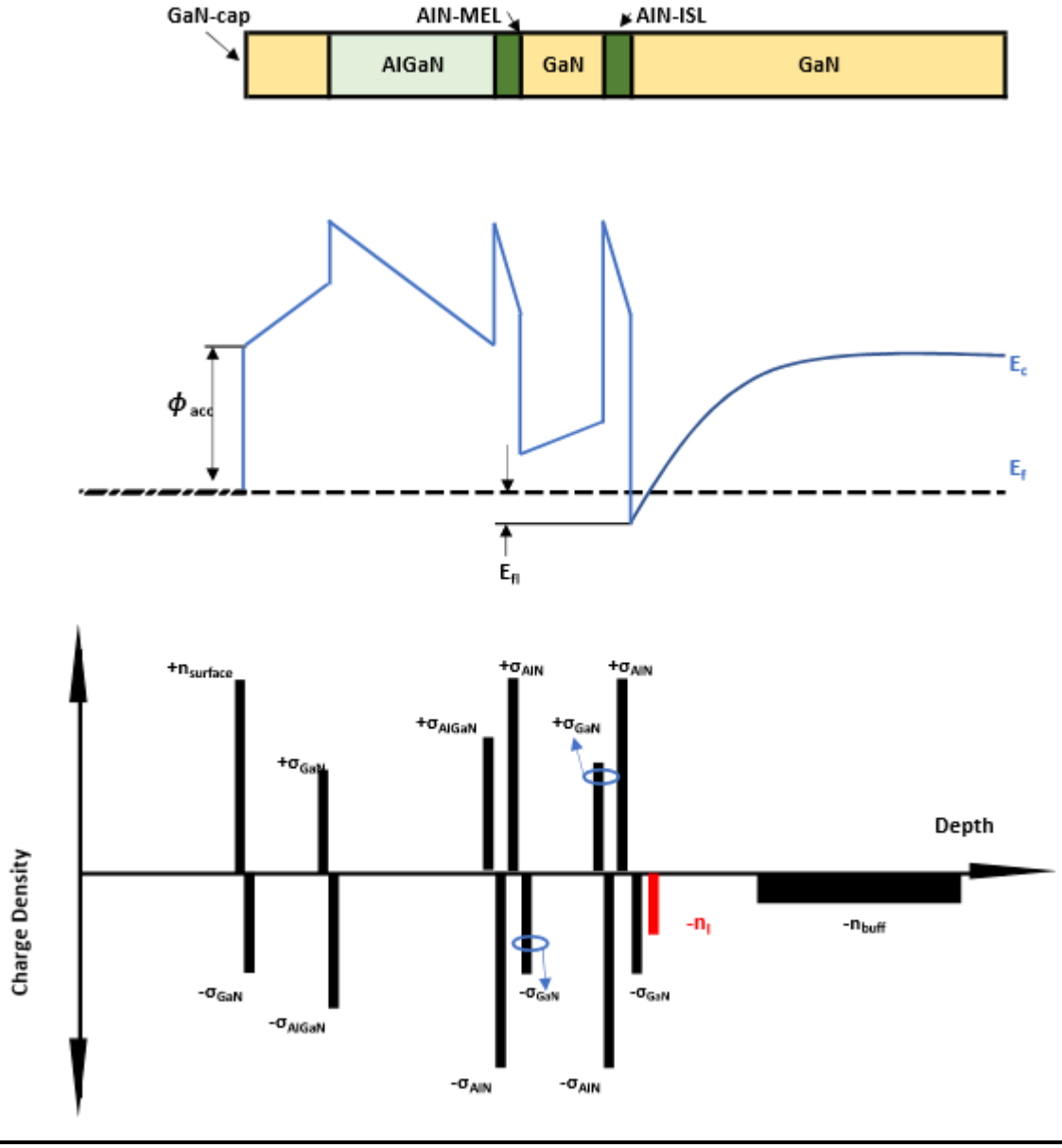

Figure 3.3. Schematics of "conduction band" diagrams and "charge distributions" at the access region of the DC-MOS-HEMT.

The surface barrier φ_{acc} is decided according to where the Fermi level is fixed. For an ungated region, it depends on the condition of the surface/interface. n_{it} surface is the density of ionized surface/interface traps. There is a "critical thickness" of the "upper channel layer" $t_{ua\text{-}crit}$. When $t_{ua} \leq t_{ua\text{-}crit}$, only the "lower channel" is formed.

The conduction band diagram and the charge distribution are illustrated in Fig. 3.3. Above expression (1) and (2) are not valid for $t_{ua} \leq t_{ua\text{-}crit}$. In this case only the lower channel exists. By applying Gauss's Rule from the "lower channel" to the surface of the GaN-cap layer, the electrostatic equation is obtained,

$$-E_{fl} + \Delta Ec_{-AlN/GaN} + \frac{q^2(\sigma_{AlN} - \sigma_{GaN} - n_l - n_{buf})}{\varepsilon_{AlN}} . t_{AlN-ISL} - \Delta Ec_{-AlN/GaN} + \frac{q^2(-n_l - n_{buf})}{\varepsilon_{AlN}} \cdot t_{ua} + \Delta Ec_{-AlN/GaN} + \frac{q^2(\sigma_{AlN} - \sigma_{AlN} - n_l - n_{buf})}{\varepsilon_{AlN}} \cdot t_{AlN-MEL} - \Delta Ec_{-AlN/AlGaN} + \frac{q^2(\sigma_{AlGaN} - \sigma_{GaN} - n_l - n_{buf})}{\varepsilon_{AlGaN}} . t_{AlGaN} - \Delta Ec_{-AlGaN/GaN} + \frac{q^2(-n_l - n_{buf})}{\varepsilon_{GaN}} \cdot t_{GaN-cap} - \varphi_{acc} = 0.$$

or

$$\left(\frac{q^2}{\varepsilon_{AlN}} t_{AlN-ISL}\right)(n_l + n_{buf}) + \left(\frac{q^2}{\varepsilon_{GaN}} t_{ua}\right)(n_l + n_{buf}) + \left(\frac{q^2}{\varepsilon_{AlN}} t_{AlN-MEL}\right)(n_l + n_{buf}) + \left(\frac{q^2}{\varepsilon_{AlGaN}} t_{AlGaN}\right)(n_l + n_{buf}) + \left(\frac{q^2}{\varepsilon_{GaN-cap}} t_{GaN-cap}\right)(n_l + n_{buf}) = [\left(\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\varepsilon_{AlN}} t_{AlN-ISL}\right) + \left(\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\varepsilon_{AlN}} t_{AlN-MEL}\right) + \left(\frac{q^2(\sigma_{AlGaN} - \sigma_{GaN})}{\varepsilon_{AlGaN}} t_{AlGaN}\right) - E_{fl} - \varphi_{acc}$$

Or

$$n_l = \frac{\left[\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\varepsilon_{AlN}} \cdot t_{AlN-ISL} + \frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\varepsilon_{AlN}} \cdot t_{AlN-MEL} + q^2 \frac{(\sigma_{AlGaN} - \sigma_{GaN})}{\varepsilon_{AlGaN}} \cdot t_{AlGaN} - E_{fl} - \varphi_{acc}\right]}{\frac{q^2}{\varepsilon_{AlN}} t_{AlN-ISL} + \frac{q^2}{\varepsilon_{GaN}} t_{ua} + \frac{q^2}{\varepsilon_{AlN}} t_{AlN-MEL} + \frac{q^2}{\varepsilon_{AlGaN}} t_{AlGaN} + \frac{q^2}{\varepsilon_{GaN-cap}} t_{GaN-cap}} - n_{buf} \quad .....(5)$$

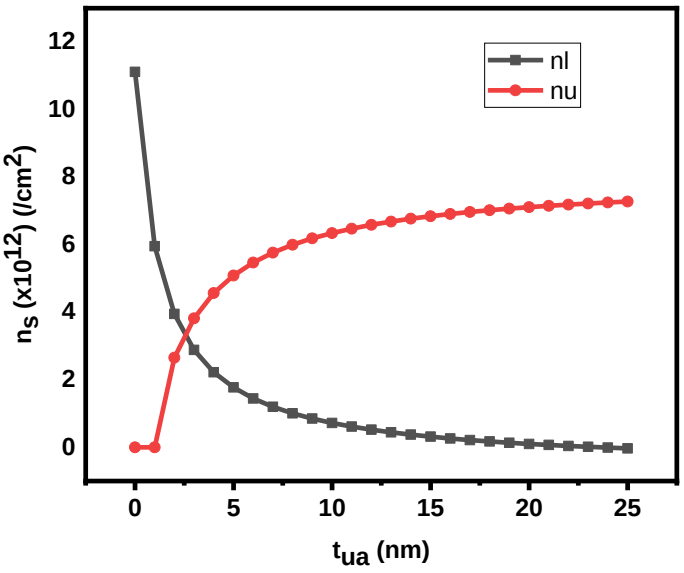

Figure 3.4. 2DEG densities in the access region of the DC-MOS-HEMT by analytical modelling and TCAD numerical simulation

Figure 3.4 shows , when $t_{ua} \leq t_{ua\text{-}crit}$, n_u= ~0. And n_l is calculated using (5).when $t_{ua} > t_{ua\text{-}crit}$, equation (2) and (3) are using for n_l and n_u calculation. So numerical model agrees with the analytical model.

A charge dipole is added to the heterostructure by the AlN-ISL.The upper surface of AlN- ISL has a negative charge, which lowers the "2DEG density" in the "upper channel" while raising the "2DEG density" in the bottom channel. When the AlN-ISL is close to the upper channel, according to equation (2), (3), and (5), a significant portion of electrons are in the lower channel. More electrons are assigned to the upper channel as the distance between the AlN-ISL and the upper channel (t_{ug}) is increased. When $t_{ua}>t_{ua\text{-}crit}$, the combined 2DEG density of the two channels (n_t) nearly remains constant, which is consistent with equation (2).However, as expected from the relationship between t_{ua} and $t_{ua\text{-}crit}$, n_l becomes a considerably stronger function of t_{ua} (5).This makes sense from an electrostatics perspective. The heterostructure has zero net charges throughout its depth. The change in the ionisation of surface traps is the primary cause of the change in n_t. The AlN-ISL dipole causes more surface traps to be ionised when there is only the "lower channel" present, and an equal increase in electrons in the "lower channel" to offset the shift in surface charges. Thus, n_t is raised. The Fermi level at the "upper channel" is attached close to the "conduction band" when the upper channel forms. Because of the top channel's screening effect, the ionisation rate of the surface traps is thus unaffected, leading to a practically constant n_t.

3.5 CHARGE DISTRIBUTION AT THE GATED REGION:

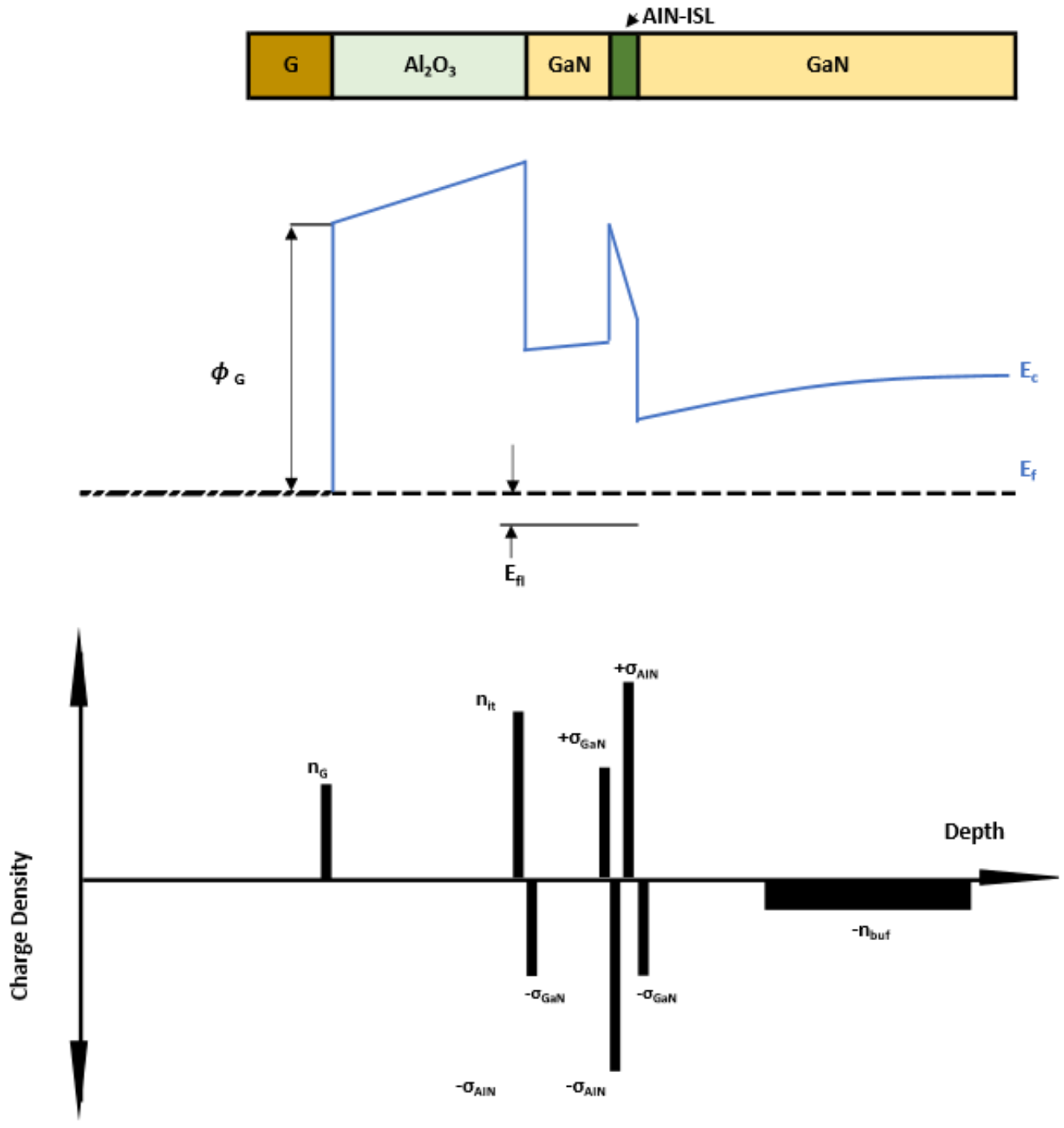

Fig 3.5.:Schematic "band diagrams" and "charge distributions" at the recessed gate region of the normally-off DC-MOS-HEMT, when V_g=0, both channels are pinched off.

3.5.1 .2DEG Density when both channels turned on:

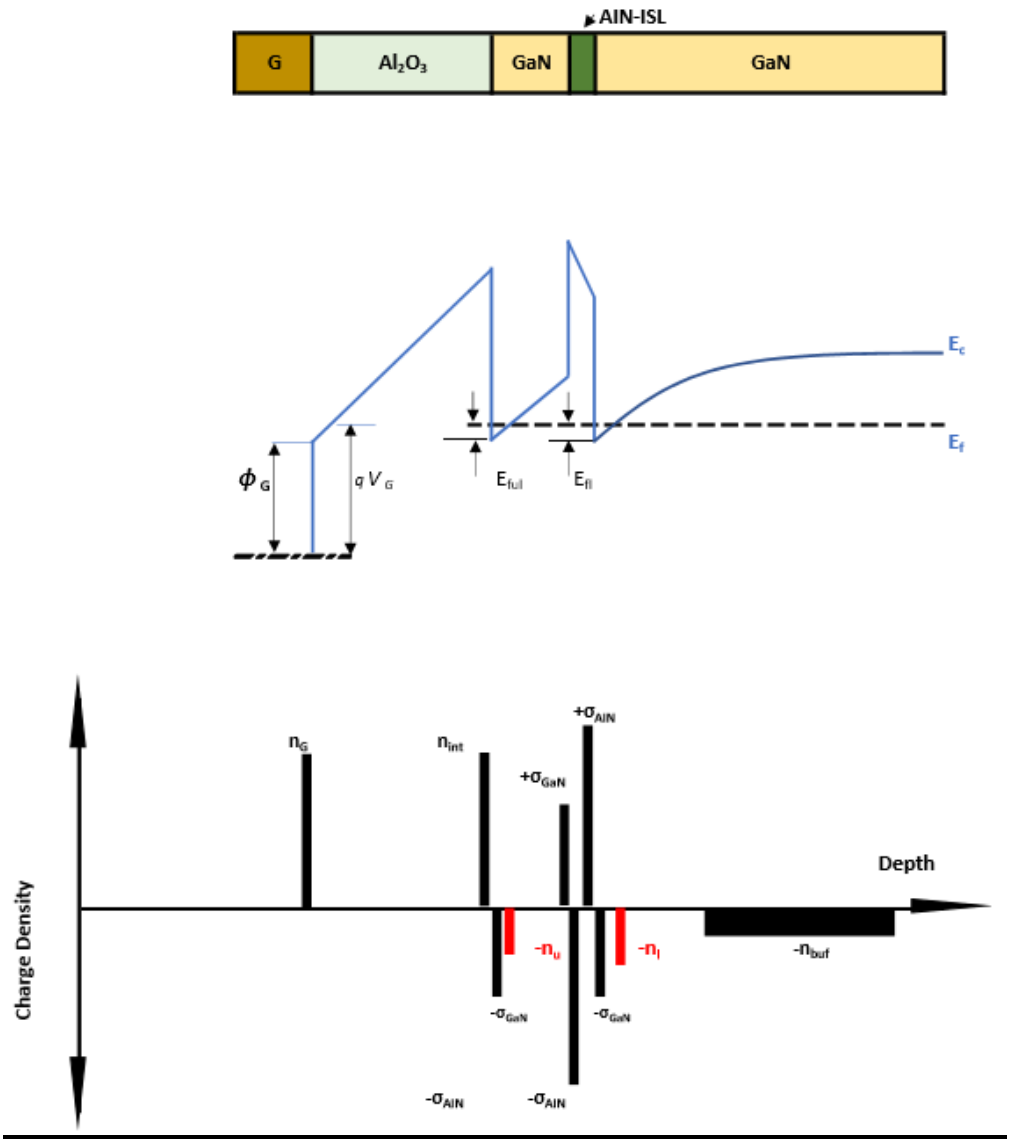

Fig 3.6: Schematic "band diagrams" and "charge distributions" at the recessed gate region of the normally-off DC-MOS-HEMT, when $V_g > V_{th\text{-}u}$, both channels are on

An effective net positive charge (n_{it}), which may include fixed charges, ionisation traps, and charges in the majority of the dielectric, is normally present at the MOS interface. The interface charge with an equivalent effect on the gate control can be used to represent the dielectric bulk charges. In the concerned study, we assume $n_{it} = 1.5\times10^{13}$ cm^{-2}. When V_g is greater than $V_{th\text{-}u}$, both channels are turned on. Now if we apply Gauss's law from the lower channel to the upper channel, we get the same equation as the equation (1)

$$n_l = \left[\frac{\left\{\frac{q^2(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}}t_{AlN-ISL}+E_{fu}-E_{fl}\right\}}{\left\{\left(\frac{q^2}{\epsilon_{GaN}}.t_{ug}\right)+\left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-ISL}\right)\right\}}\right] - n_{buf} \qquad \text{.....(6)}$$

We apply Gauss' Law from the upper channel to the gate electrode to obtain the formula for the "2DEG density" in the upper channel.

$$-E_{fu} + \Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN}-n_l-n_u-n_{buf})}{\varepsilon_{Al2O3}} \cdot t_{Al2O3} - \varphi_G + qV_g = 0.$$

Here,$\Delta EC_{\text{-Al2O3/GaN}}$ is the conduction band offset, which value is 2.57 eV.

$$(n_l + n_u + n_{buf})\left(\frac{q^2}{\varepsilon_{Al2O3}} t_{Al2O3}\right) = -E_{fu} + \Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN})}{\varepsilon_{Al2O3}} t_{Al2O3} - \varphi_G + qV_g$$

Or

$$n_u = \frac{\left[\Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN})}{\varepsilon_{Al2O3}} t_{Al2O3} - E_{fu} - \varphi_G + qV_g\right]}{\frac{q^2}{\varepsilon_{Al2O3}} t_{Al2O3}} - n_l - n_{buf} \quad \text{.....(7)}$$

This is the the"2DEG density" in the upper channel, which is obtained by simplifying the above equation.

3.5.2.Threshold voltage of the Upper Channel:

From equation (7), we can understand that nu drops when gate voltage decreases. If gate voltage is decreased to the Upper channel Threshold Voltage i.e $V_{th\text{-}u}$,upper channel will be turned off. In such condition, n_u=0 and also E_{fu}=0.The "2DEG Density" in the lower channel will be same as equation (6).

$$n_l = \left[\frac{\left\{\frac{q^2(\sigma_{AlN}-\sigma_{GaN})}{\epsilon_{AlN}} t_{AlN-ISL} + E_{fu} - E_{fl}\right\}}{\left\{\left(\frac{q^2}{\epsilon_{GaN}}.t_{ug}\right) + \left(\frac{q^2}{\epsilon_{AlN}}.t_{AlN-ISL}\right)\right\}}\right] - n_{buf} \quad \text{.....(8)}$$

Putting n_u=0 and E_{fu}=0 at equation (7)

$$0 = \frac{\left[\Delta Ec_{-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN})}{\varepsilon_{Al2O3}} t_{Al2O3} - \varphi_G + qV_g\right]}{\frac{q^2}{\varepsilon_{Al2O3}} t_{Al2O3}} - n_l - n_{buf}$$

Or

$$(n_l + n_{buf})\left(\frac{q^2}{\varepsilon_{Al2O3}} t_{Al2O3}\right) = [\Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN})}{\varepsilon_{Al2O3}} t_{Al2O3} - \varphi_G + qV_g]$$

Or,

$$-qV_g = \Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN}-n_l-n_{buf})}{\varepsilon_{Al2O3}} t_{Al2O3} - \varphi_G$$

Or

$$V_{th\text{-}u} = -\left[\Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it}-\sigma_{GaN}-n_l-n_{buf})}{\varepsilon_{Al2O3}} t_{Al2O3} - \varphi_G\right]/q \quad \text{.....(9)}$$

This equation is for upper channel Threshold Voltage.

3.5.3. 2DEG Density When Only the Lower Channel Turned On:

When $V_{th-l} < V_g < V_{th-u}$, only Lower channel turns on.

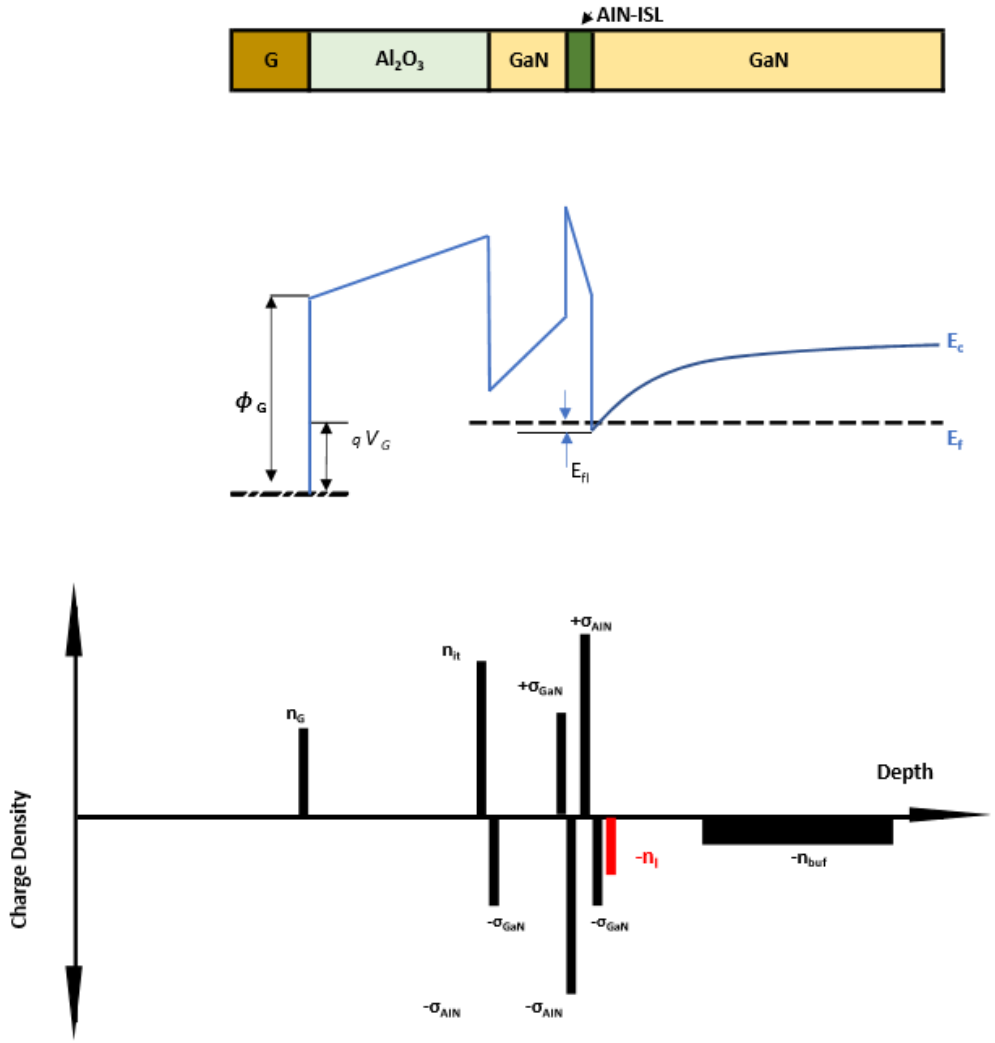

Fig 3.7: Schematic "band diagrams" and "charge distributions" at the "recessed gate region" of the normally-off DC-MOS-HEMT, when $V_{th-l} < V_g < V_{th-u}$, only lower channel turns on

Now if we apply Gauss's Law, from lower channel to the gate electrode,

$$-E_{fl} + \Delta E_{c-AlN/GaN} + \frac{q^2(\sigma_{AlN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AlN}} \cdot t_{AlN-ISL} - \Delta E_{c-AlN/GaN} + \frac{q^2(-n_l - n_{buf})}{\epsilon_{GaN}} \cdot t_{ug} + \Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{Al2O3}} \cdot t_{Al2O3} - \varphi_G + qV_g = 0.$$

Or,

$$\left(n_l + n_{buf}\right)\left[\left(\frac{q^2}{\epsilon_{AlN}} t_{AlN-ISL}\right) + \left(\frac{q^2}{\epsilon_{GaN}} t_{ug}\right) + \left(\frac{q^2}{\epsilon_{Al2O3}} t_{Al2O3}\right)\right] = [-E_{fl} + \frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\epsilon_{AlN}} t_{AlN-ISL} + \Delta E_{c-Al2O3/GaN} + \frac{q^2(n_{it} - \sigma_{GaN})}{\epsilon_{Al2O3}} t_{Al2O3} - \varphi_G + qV_g$$

Or,

$$n_l = \frac{\left[\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\epsilon_{AlN}} t_{AlN-ISL} + \frac{q^2(n_{it} - \sigma_{GaN})}{\epsilon_{Al2O3}} t_{Al2O3} - \Delta E_{c-Al2O3/GaN} - \varphi_G + qV_g - E_{fl}\right]}{[\left(\frac{q^2}{\epsilon_{AlN}} t_{AlN-ISL}\right) + \left(\frac{q^2}{\epsilon_{GaN}} t_{ug}\right) + \left(\frac{q^2}{\epsilon_{Al2O3}} t_{Al2O3}\right)]} - n_{buf} \quad \text{.....(10)}$$

This is the "2DEG Density" in the lower channel.

D. Threshold Voltage of the Lower Channel:

When we calculate Threshold Voltage for Lower channel, we set the value n_l=0 and E_{fl}=0 in the equation (10)

$$0 = \frac{\left[\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\epsilon_{AlN}} t_{AlN-ISL} + \frac{q^2(n_{it} - \sigma_{GaN})}{\epsilon_{Al2O3}} t_{Al2O3} - \Delta E_{c-Al2O3/GaN} - \varphi_G + qV_g\right]}{[\left(\frac{q^2}{\epsilon_{AlN}} t_{AlN-ISL}\right) + \left(\frac{q^2}{\epsilon_{GaN}} t_{ug}\right) + \left(\frac{q^2}{\epsilon_{Al2O3}} t_{Al2O3}\right)]} - n_{buf}$$

or

$$n_{buf}\left[\left(\frac{q^2}{\epsilon_{AlN}} t_{AlN-ISL}\right) + \left(\frac{q^2}{\epsilon_{GaN}} t_{ug}\right) + \left(\frac{q^2}{\epsilon_{Al2O3}} t_{Al2O3}\right)\right] = \left[\frac{q^2(\sigma_{AlN} - \sigma_{GaN})}{\epsilon_{AlN}} t_{AlN-ISL} + \frac{q^2(n_{it} - \sigma_{GaN})}{\epsilon_{Al2O3}} t_{Al2O3} - \Delta E_{c-Al2O3/GaN} - \varphi_G + qV_g\right]$$

Or

$$V_{th-l} = -\frac{\left[\frac{q^2\left(\sigma_{AlN} - \sigma_{GaN} - n_{buf}\right)}{\epsilon_{AlN}} t_{AlN-ISL} + \frac{q^2\left(-n_{buf}\right)}{\epsilon_{GaN}} t_{ug} + \Delta E_{c-Al2O3/GaN} + \frac{q^2\left(n_{it} - \sigma_{GaN} - n_{buf}\right)}{\epsilon_{Al2O3}} t_{Al2O3} - \varphi_G\right]}{q} \quad \text{.....(11)}$$

In the DC-MOS-HEMT, $V_{th\text{-}l}$ is actually the "threshold voltage" of the device itself because the lower channel turns on before the upper channel does (V_{th}).

CHAPTER-4

4.1.RESULTS AND DISCUSSION:

Here we finally obtain the necessary results along with the discussions thereby explaining the situation physically and drawing an agreement with the graphical observation. The plots are obtained after writing necessary programs using Analytical Model.

Here we are observing the effect of AlN-ISL layer, varying the thickness(1.5nm,3nm,4.5nm,6nm) of it.

4.1.1. 2DEG Density Variation with the variation of AlN-ISL Layer and tug:

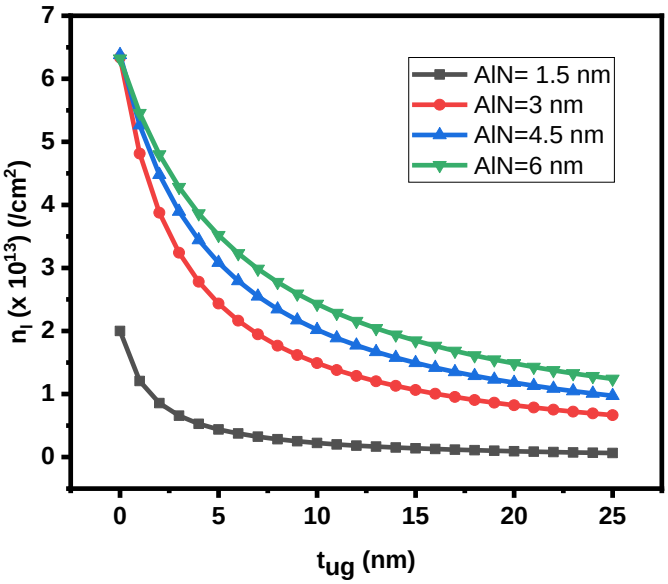

Fig 4.1: Variation of 2DEG Density of "Lower Channel" with reference to t_{ug} for Different thickness of AlN-ISL Layer.

Using the equation (6) ,here we obtained the 2DEG Variation of Lower channel for different thickness of tug and AlN-ISL Layer. It is observed that the density of electron increases with the rise in thickness of A1N-ISL layer. This may happen because of the strong polarisation between "AlN and GaN" layer. Due to the strong polarisation both positive and negative sheet charges are located at its opposite surfaces. Which may affect the 2DEG Density of upper channel Layer also.

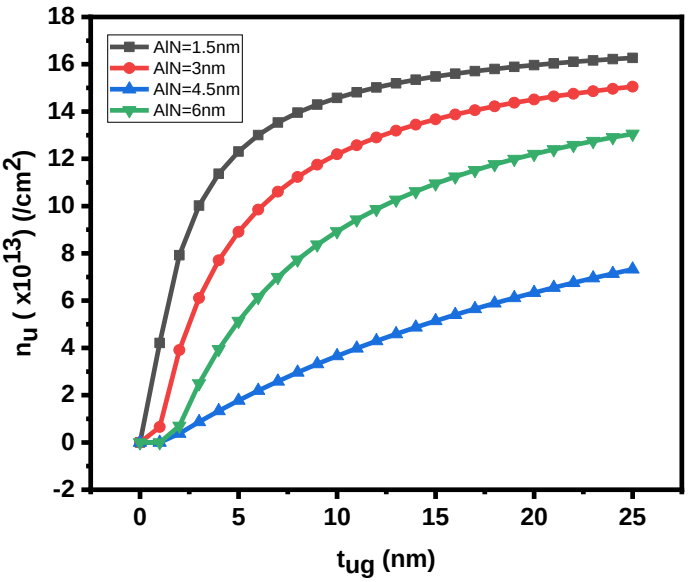

Fig 4.2: Variation of 2DEG Density of "Upper Channel" with reference to t_{ug} for Different thickness of AlN-ISL Layer.

As we can see the above graph (Figure 4.2) is showing the 2DEG Density of upper channel layer with the variation of tug and AlN-ISL Layer. This graph is obtained using the equation (6) and equation (7),taking the V_g=10 V. The Density of electron is getting decreased with increase of thickness of AlN-ISL layer. Because the strong polarisation introduces a charge dipole into the heterostructure. Due to this dipole the located negative charge in the upper surface of the AlN-ISL layer,

reduce the electron density(2DEG Density) in upper channel.

Comparing Figure (4.1) and Figure (4.2) , we can see, when the charge dipole at AlN-ISL layer reducing the 2DEG Density of upper channel layer, and simultaneously it is increasing the 2DEG Density of the lower channel. Which compensate the total electron density. So the net charge is constant.

Again, when we increase the distance between upper channel and AlN-ISL i.e when t_{ug} is enlarged, the upper channel electron density is getting increase and the lower channel electron density is getting decreased. So increasing the distance more electron get allocated at the upper channel.

4.1.2. 2DEG Density in the upper channel with the variation of V_g for different t_{ug} and different AlN Layer thickness:

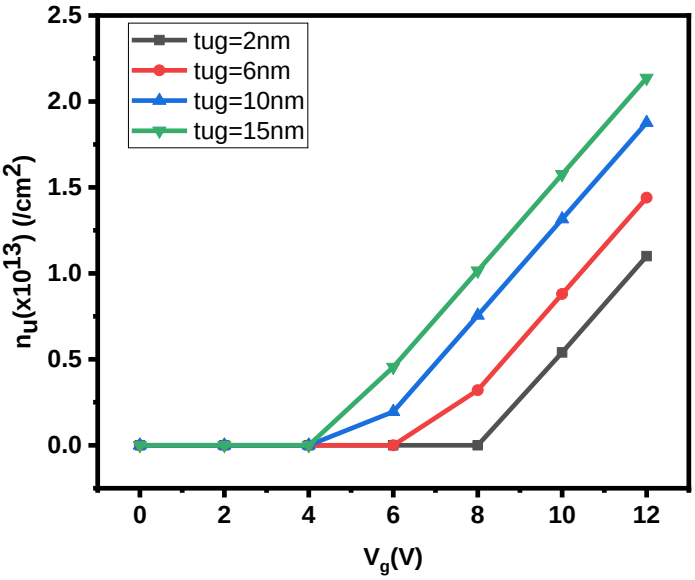

Fig.4.3: The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=1.5 nm

Here, in Figure (4.3) we observe the variation of "2DEG Density" of the "upper channel" with respect to V_g for different thickness of t_{ug}. We can see when t_{ug}=2nm upper channel is off at lower V_g. This is because of the located negative charge of the upper surface of AlN-ISL layer. When t_{ug} is small upper channel will be on at higher V_g, when AlN-ISL layer thickness is 1.5 nm.

Concurrently, if we increase t_{ug}, we can see at comparable lower V_g, upper channel is turned on. For t_{ug} =6nm upper channel became on at V_g near about 7 Volt. But at t_{ug}=2nm gate voltage was more than 8 Volt to make upper channel on.

So if the distance between upper channel and AlN-ISL is increased ,with a small gate voltage we can make upper channel on.

Thus AlN-ISL has a significant impact on 2DEG Density of both upper and Lower Channel.

Now we will observe if we raise the AlN-ISL layer thickness, the impact on 2DEG.

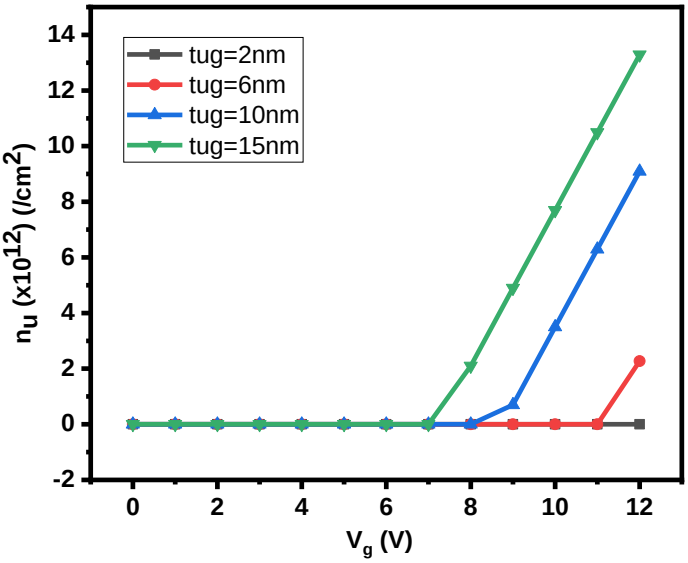

Fig.4.4: The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=3 nm

Similarly we obtain this graph from equation(6) and (7). This graph (Figure4.4) shows upper channel 2DEG Density with respect to gate voltage(V_g) For AlN-ISL=3nm

We can see, if we raise the thickness of AlN layer, density of the "negative charge" in the upper surface of AlN layer will increase. And this will decrease the positive charge density in the "upper channel" . So the Threshold voltage of the upper will shift to the more positive value. More positive gate voltage will require to make upper channel on.

Now if we enlarge the distance of t_{ug} ,Threshold voltage of the upper channel will be decreased.2DEG Density will be more in the upper channel.

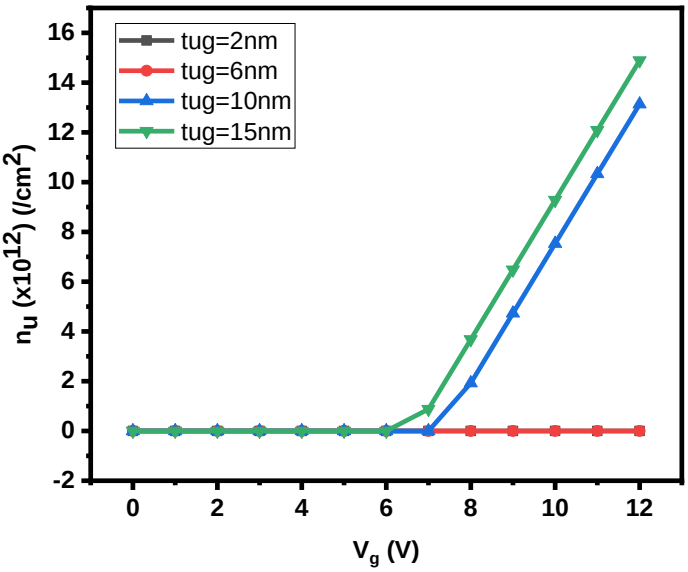

Fig.4.5: The upper channel "2DEG Density" with reference to gate voltage and the Thickness of AlN-ISL Layer=4.5 nm

Figure (4.5) is obtained from equation (6) and (7). This graph is showing when AlN-ISL layer thickness is 4.5 nm, for t_{ug}=2nm and t_{ug}=6 nm, no electrons get accumulated to make 2DEG. So the upper channel 2DEG Density is zero.

When t_{ug}=10 nm i.e AlN-ISL layer is far from the upper channel ,then some electron get accumulated to form upper channel.

When t_{ug}=15nm, more electrons get accumulated and form the upper channel.

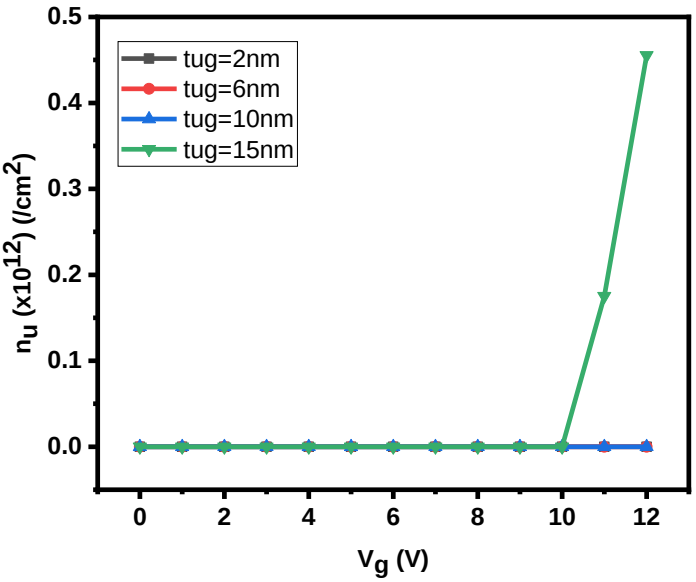

Fig.4.6: The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=6 nm

When AlN-ISL layer thickness is 6nm , the density of the negative charge in the upper surface is that high no positive charge can accumulate to form upper channel. So the threshold voltage is very high for AlN-ISL=6nm.

When AlN-ISL Layer thickness is as high as 6nm and t_{ug} value is small no upper channel formation is there with gate voltage 10 volt.

After making t_{ug}=15 nm, some 2DEG is showing but the value is very small.

4.1.3 Threshold Voltage of Upper and "Lower Channel" with respect to tug:

A. Threshold Voltage of Lower Channel for different Thickness of AlN-ISL:

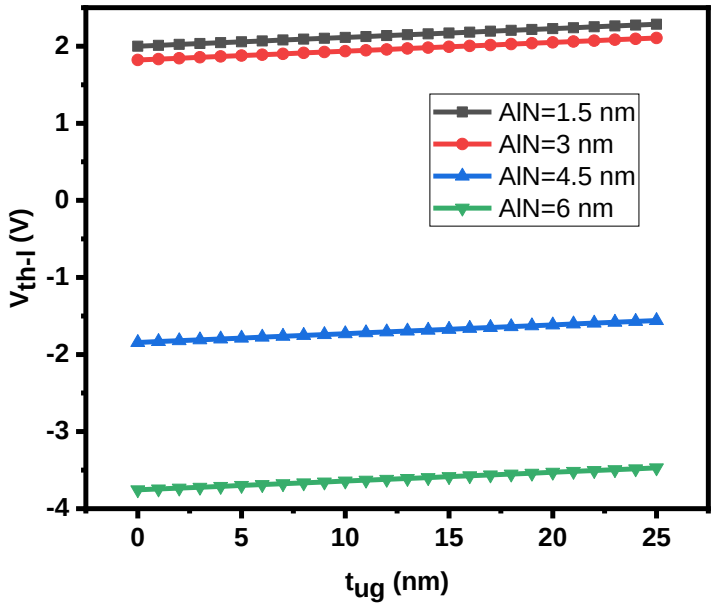

Fig 4.7: Threshold Voltage of Lower channel with the variation of t_{ug} for Different thickness of AlN-ISL

From Figure 4.1, we have already seen that the 2DEG Density got increased with the variation of AlN-ISL layer.The Threshold Voltage for the lower channel we have calculated using the equation (11). From the equation it is observed that threshold voltage is a strong function of AlN-ISL .

When AlN-ISL=1.5nm, the 2DEG Density of the lower channel is ~$2x10^{13}$ cm^{-2} which makes threshold voltage ~2V. But as we have increased the thickness of the AlN-ISL layer the 2DEG Density is increased. As 2DEG Density increased Threshold Voltage got decreased.

For AlN-ISL=3nm, 2DEG Density at t_{ug}=2nm is ~$5x10^{13}$ cm^{-2}. Which makes still threshold voltage a positive value. But further increase of AlN-ISL layer thickness make threshold voltage a negative value. Due to the strong polarisation between AlN-ISL Layer and GaN layer , a large number of electron accumulates at the lower channel and makes lower channel 2DEG Density very high. For this reason Threshold Voltage shifts towards negative Value.

B.Threshold Voltage of upper Channel for different Thickness of AlN-ISL:

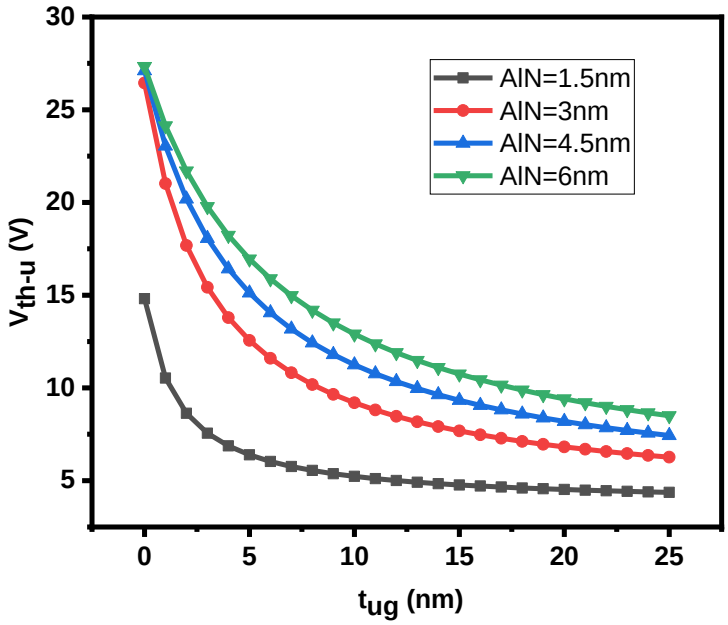

Fig 4.8: Threshold Voltage of Upper channel with the variation of tug for Different thickness of AlN-ISL

The expression for Threshold voltage of upper channel has been derived. From equation (9), it is seen that that the "threshold voltage" derived is also a strong function of AlN-ISL layer. And also from Figure (4.3),(4.4),(4.5),(4.6) we can see that threshold voltage of the upper channel is strong function of t_{ug} also.

When AlN-ISL layer thickness is 1.5 nm and t_{ug}=2nm , the "threshold voltage" of the "upper channel" is a positive value. Because of the positive charge of upper surface of the AlN-ISL makes 2DEG Density of upper channel very low. It needs high gate voltage to make upper channel on. But if we shift AlN-ISL downwards i.e for large value of t_{ug} electron density in the upper channel increased , which makes threshold voltage comparatively low. Figure (4.8) also proves that.

When AlN-ISL layer thickness is more than 1.5 nm and t_{ug} is small more positive charge will accumulate on the upper surface of the AlN-ISL, which makes upper channel of for lower value of the gate voltage.

When AlN-ISL Layer thickness is as high as 6nm and t_{ug} value is small no upper channel formation is therewith gate voltage 10 volt. So the "Threshold Voltage" for upper channel is very high with the 6nm thickness of AlN-ISL layer.

CHAPTER-5

5.1. CONCLUSION:

This thesis shows the 2DEG variations with the "AlN Insertion Layer" thickness for different thickness of upper channel layer at gate region. When gate voltage is less than lower channel threshold voltage, two channels are pinched off, so 2DEG density of lower and upper channel is equal to zero. When gate voltage is less than upper channel threshold voltage but more than lower channel threshold voltage, 2DEG density of upper channel is zero but lower channel exists.

We have found that smaller value of thickness of upper channel layer at gate region will give the abundance of electron in lower channel. Now if the thickness of the AlN-ISL layer is raised too, the electron accumulation will be more, and simultaneously the electron density at the upper channel will decrease. So the upper channel threshold voltage will increase.

As threshold voltage of the upper channel is the strong function of thickness of the upper channel at gate region, if the value of thickness of the upper channel at gate region is raised, the threshold voltage for the upper channel will be decreased.

At the same time threshold voltage of lower channel is almost independent of t_{ug} but it is a strong function of $t_{AlN\text{-}ISL}$. Larger thickness of AlN-ISL will contribute to a massive number of electrons at lower channel so the threshold voltage of the lower channel shifts towards negative value.

We have found that as the lower channel is turned on first followed by the upper channel, lower channel threshold voltage is the "threshold voltage of DC-MOS HEMT".

Appendix

- **2DEG densities in the access region of the DC-MOS-HEMT:**

```
a=4.29*10^-13;
b=1.824*10^-14;
c=3.86*10^-26;
d=3.04*10^-26;
tua=[0:1:25]
nl=[(a-tua.*b)./(c+tua.*d)./10^12]
e=2.432*10^-14
f=1.96*10^-14
c1=4.86*10^-27
d1=3.04*10^-27
tua=[0:1:25]
nu=[(tua.*e-f)./(c1+tua.*d1)./10^12]
for i=1:6
   if nu(i)<0
      nu(i)=0;

   end
end
nl
plot(tua,nl);
hold on
plot(tua,nu);
```

- **Variation of 2DEG Density of "Lower Channel" with reference to t_{ug} for Different thickness of AlN-ISL Layer:**

```
tug=[0:1:25]
a=9.72*10^-13;
b=1.824*10^-14;
c=4.86*10^-26;
d=3.04*10^-26;
nl=[((a-tug.*b)./(c+tug.*d))./10^13];
nl1=[((6.16*10^-12)-tug.*(1.824*10^-14))./(tug.*(3.04*10^-26)+(9.72*10^-26))./10^13]
nl2=[((9.2526*10^-12)-tug.*(1.824*10^-14))./(tug.*(3.04*10^-26)+(1.45*10^-25))./10^13]
nl3=[((1.22834*10^-11)-tug.*(1.824*10^-14))./(tug.*(3.04*10^-26)+(1.944*10^-25))./10^13]
plot(tug,nl)
hold on
plot(tug,nl1)
hold on
plot(tug,nl2)
hold on
plot(tug,nl3)
```

- **Variation of 2DEG Density of "Upper Channel" with reference to t_{ug} for Different thickness of AlN-ISL Layer:**

```
tug=[0:1:25]
a1=5.3424*10^-12;
b1=2.02*10^-12;
c1=4.86*10^-26;
d1=3.04*10^-26;
nu=[((tug.*a1-b1)./(c1+tug.*d1))./10^13];
for i=1:6
   if nu(i)<0
      nu(i)=0;

   end
end
nu
nu1=[((tug.*5.342*10^-12)-(4.51*10^-12))./((tug.*3.04*10^-26)+(9.72*10^-26))./10^13]
for i=1:6
   if nu1(i)<0
      nu1(i)=0;

   end
end
nu1
nu2=[((tug.*5.3464*10^-12)-(6.787*10^-12))./((tug.*3.04*10^-26)+(9.72*10^-25))./10^13]
for i=1:6
   if nu2(i)<0
      nu2(i)=0;

   end
end
nu
nu3=[((tug.*5.34*10^-12)-(8.9*10^-12))./((tug.*3.04*10^-26)+(1.944*10^-25))./10^13]
for i=1:6
   if nu3(i)<0
      nu3(i)=0;

   end
end
nu3
plot(tug,nu)
hold on
plot(tug,nu1)
hold on
plot(tug,nu2)
hold on
plot(tug,nu3)
```

- **The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=1.5 nm:**

```
a1=2.80*10^12;
b1=2.26*10^13;
vg=[0:2:12];
nu1=[(vg.*a1-b1)./10^13];
for i=1:7
   if nu1(i)<0
      nu1(i)=0;
   end

end
nu1
a2=2.80*10^12
b2=1.92*10^13
nu2=[(vg.*a2-b2)./10^13]
for i=1:7
   if nu2(i)<0
      nu2(i)=0;
   end

end
nu2
a3=2.802*10^12
b3=1.486*10^13
nu3=[(vg.*a3-b3)./10^13]
for i=1:7
   if nu3(i)<0
      nu3(i)=0;
   end

end
nu3
a4=2.802*10^12;
b4=1.226*10^13;
nu4=[(vg.*a4-b4)./10^13];
for i=1:7
   if nu4(i)<0
      nu4(i)=0;
   end
end
nu4
plot(vg,nu1)
hold on
plot(vg,nu2)
hold on
plot(vg,nu3)
hold on
plot(vg,nu4)
```

- **The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=3 nm:**

```
vg=[0:1:12];
q=1.6*10^-19;
l=length(vg);
nu1=[((vg.*q-5.597*10^-18)./(5.719*10^-32))./10^12]
for i=1:l
   if nu1(i)<0
      nu1(i)=0;

   end
end
nu1
nu2=[((vg.*q-1.79*10^-18)./(5.719*10^-32))./10^12]
for i=1:l
   if nu2(i)<0
      nu2(i)=0;

   end
end
nu2
nu3=[((vg.*q-1.40*10^-18)./(5.719*10^-32))./10^12]
for i=1:l
   if nu3(i)<0
      nu3(i)=0;

   end
end
nu3
nu4=[((vg.*q-1.16*10^-18)./(5.719*10^-32))./10^12]
for i=1:l
   if nu4(i)<0
      nu4(i)=0;

   end
end
nu4
plot(vg,nu1)
hold on
plot(vg,nu2)
hold on
plot(vg,nu3)
hold on
plot(vg,nu4)
```

- **The upper channel "2DEG Density" with reference to gate voltage and the Thickness of AlN-ISL Layer=4.5 nm:**

```
vg=[0:1:12]
q=1.6*10^-19
l=length(vg)
nu1=[((vg.*q-3.116*10^-18)./(5.719*10^-32))./10^12]
for i=1:l
   if nu1(i)<0
      nu1(i)=0;

   end
end
nu1
nu2=[((vg.*q-2.22*10^-18)./(5.71*10^-32))./10^12]
for i=1:l
   if nu2(i)<0
      nu2(i)=0;

   end
end
nu2
nu3=[((vg.*q-1.17*10^-18)./(5.71*10^-32))./10^12]
for i=1:l
   if nu3(i)<0
      nu3(i)=0;

   end
end
nu3
nu4=[((vg.*q-1.07*10^-18)./(5.71*10^-32))./10^12]
for i=1:l
   if nu4(i)<0
      nu4(i)=0;

   end
end
nu4
plot(vg,nu1)
hold on
plot(vg,nu2)
hold on
plot(vg,nu3)
hold on
plot(vg,nu4)
```

- **The upper channel 2DEG Density with respect to gate voltage and the Thickness of AlN-ISL Layer=6 nm:**

```
vg=[0:1:12]
q=1.6*10^-19
l=length(vg)
nu1=[((vg.*q-3.34*10^-18)./(5.71*10^-32))./10^13]
for i=1:l
   if nu1(i)<0
      nu1(i)=0;

   end
end
nu1
nu2=[((vg.*q-2.44*10^-18)./(5.71*10^-32))./10^13]
for i=1:l
   if nu2(i)<0
      nu2(i)=0;

   end
end
nu2
nu3=[((vg.*q-1.99*10^-18)./(5.71*10^-32))./10^13]
for i=1:l
   if nu3(i)<0
      nu3(i)=0;

   end
end
nu3
nu4=[((vg.*q-1.66*10^-18)./(5.71*10^-32))./10^13]
for i=1:l
   if nu4(i)<0
      nu4(i)=0;

   end
end
nu4
plot(vg,nu1)
hold on
plot(vg,nu2)
hold on
plot(vg,nu3)
hold on
plot(vg,nu4)
```

- **Threshold Voltage of Lower channel with the variation of t_{ug} for Different thickness of AlN-ISL:**

```
tug=[0:1:25]
vth_l1=[-(-2-tug.*0.0114125)]
vth_l2=[-(-1.82125-tug.*0.0114125)]
vth_l3=[-(1.84375-tug.*0.0114125)]
vth_l4=[-(3.75625-tug.*0.0114125)]
plot(tug,vth_l1)
hold on
plot(tug,vth_l2)
hold on
plot(tug,vth_l3)
hold on
plot(tug,vth_l4)
```

- **Threshold Voltage of Upper channel with the variation of tug for Different thickness of AlN-ISL:**

```
tug=[0:1:25]
a=7.198*10^-25
b=1.124*10^-25
c=4.86*10^-26
d=3.04*10^-26
vth_u=[(a+tug.*b)./(c+tug.*d)]
vth_u1=[((tug.*1.12*10^-25)+(2.57*10^-24))./((tug.*3.04*10^-26)+(9.72*10^-26))]
vth_u2=[((tug.*1.12*10^-25)+(3.93*10^-24))./((tug.*3.04*10^-26)+(1.45*10^-25))]
vth_u3=[((tug.*1.12*10^-25)+(5.3125*10^-24))./((tug.*3.04*10^-26)+(1.944*10^-25))]
plot(tug,vth_u)
hold on
plot(tug,vth_u1)
hold on
plot(tug,vth_u2)
hold on
plot(tug,vth_u3)
hold off
```

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