INVESTIGATION OF SiC TRENCH GATE UMOSFET TO REDUCE ITS ON-RESISTANCE

Thesis Submitted to the Department of Electronics and Telecommunication Engineering in partial fulfilment of the requirements for the degree of

MASTER IN TECHNOLOGY IN VLSI AND MICRO ELECTRONICS ENGINEERING

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Certificate of Recommendation

This is to certify that **Tania Bera** has satisfactorily completed the thesis entitled **"INVESTIGATION OF SiC TRENCH GATE UMOSFET TO REDUCE ITS ON-RESISTANCE" under** the guidance of Dr. **Chandrima Mondal**, Department of Electronics and Telecommunication Engineering, Jadavpur University. We recommend that her dissertation is fully adequate in scopeand quality for the partial fulfilment of the requirement for the degree of MASTER **IN TECHNOLOGY IN VLSI AND MICRO ELECTRONICS ENGINEERING,** in the Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata-700032.

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The foregoing thesis entitled **"INVESTIGATION OF SiC TRENCH GATE UMOSFET TO REDUCE ITS ON-RESISTANCE"** is hereby approved as a creditable study of **MASTER IN TECHNOLOGY IN VLSI AND MICRO ELECTRONICS ENGINEERING** in Department of Electronics and Telecommunication Engineering and presented in a manner satisfactory to warrant its acceptance as a prerequisite to the degree for which it has been submitted. It is understood that by this approval the undersigned do not necessarily endorse or approve any statement made, opinion expressed or conclusion drawn therein but approve this thesis only for the purpose for which it is submitted.

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ABSTRACT

The SiC U-shaped trench-gate metal-oxide semiconductor field-effect transistors or UMOSFETs are generally known as a SiC MOSFET with low ON-resistance because of the absence of high channel density and JFET resistances. At high drain voltages, during the device operation the gate oxide of UMOSFET suffers from a high electric field. To overcome the problem, in the structure a p^+ shielding region is added at the bottom of the trench. The p^+shielding region guards the gate oxide. But when p^+ shielding region is added, it increases the total ON-resistance as it is introducing a JFET region composed of the drift region, p-body region, and p+ shielding region. In this thesis, an upgraded SiC UMOSFET structure with an added n-type region in the drift region is discussed to reduce ON-resistance of the device. A n-type region is added in the drift layer for that reason depletion region is decreased as a result, ON-resistance of the modified-UMOS is reduced. Here we have compared the ON-resistance of modified UMOSFET with varying the trench depth and implementing the same with simulations using Sentaurus TCAD.

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CHAPTER 1: INTRODUCTION

In recent years the scientists showing their attention in power semiconductor [1] devices for different kind of electronic products. Power ICs are mainly used in electronic products, like mobile phones, laptops, digital cameras etc. Power MOS have become the smart choice for the switching devices as it has low switching power loss.

Power diode were first power semiconductor device, which was introduced in 1952 by R. N. HALL. The thyristors were introduced in 1957. They can carry high current and also able to resist high reverse breakdown voltage. It has a disadvantage that once it is turned on, we cannot turn off it by external control, we have to disconnect power from the device, to turned it off. For switching circuits this is a major disadvantage.

Bipolar transistors were introduced in 1948, but the first device which can handle large power were introduced in the 1960s [1]. we can turn it on or off by controlling the base terminal thus the BJT overcomes the limitations (the turn off issue) of the thyristors.

Power MOSFET was introduced in the 1970s with the developments of the MOSFET technology. These devices work at high frequency. In 1969 HITACHI invented 1st vertical MOSFET named as VMOS or V-groove MOSFET [2]. In the same year double diffused MOSFET or D MOSFET [2] was invented in ETL LAB, with self-aligned gate.

Insulated Gate Bipolar Transistor (IGBT) [1] became popular in the 1990s. IGBT can handle power like BJT, and also have the advantages of the isolated gate drive of the power MOSFET. It has since nearly fully replaced the BJT in power applications.

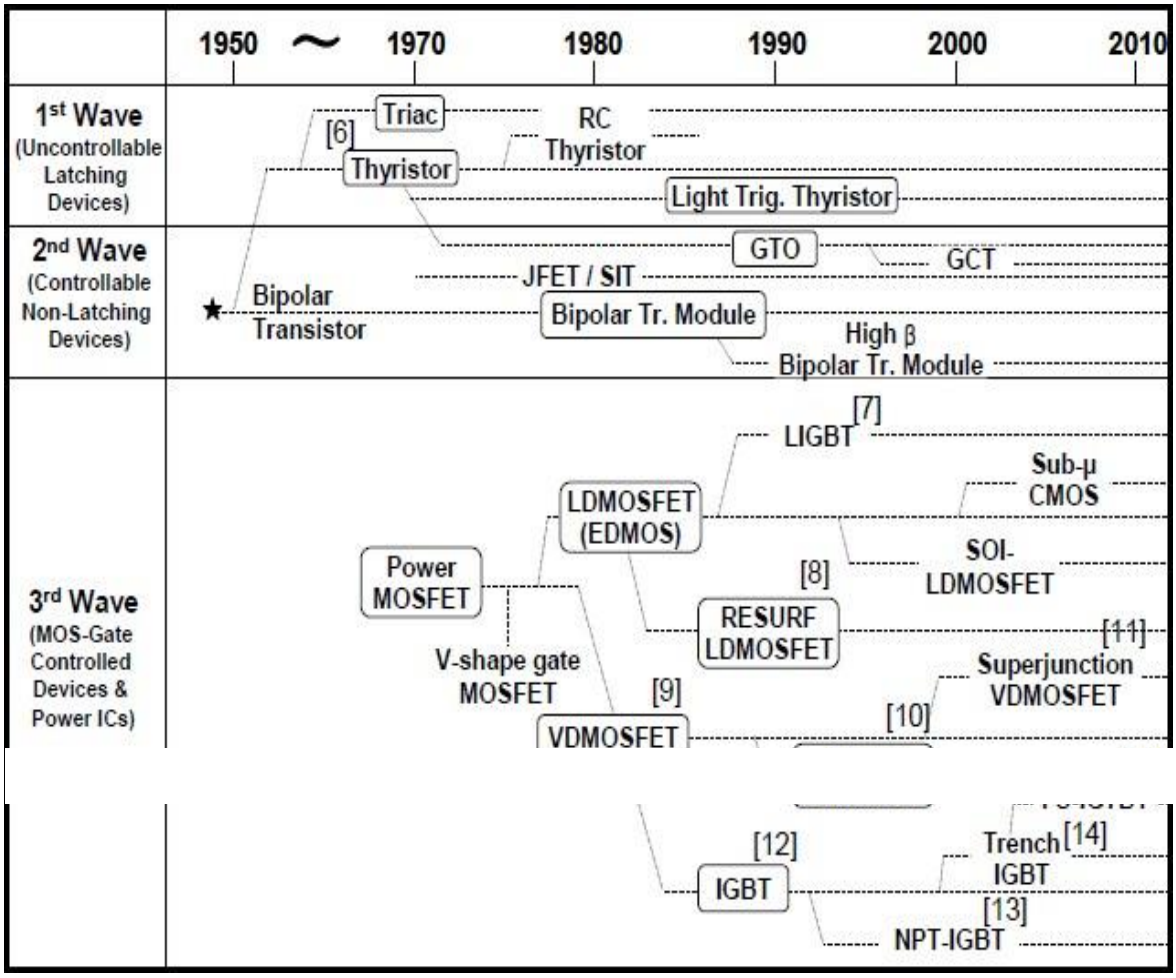

Fig:1.1 Growth of power semiconductor devices [2]

1.1 MERITS OF POWER MOSFETS

Power MOSFETs are important device in handling high current and high voltage applications. Power MOSFETs are seen in the 1970s, before that power bipolar transistors were the only devices available for high-speed power applications. BJT's production cost is low but due to their low current gain at typical current operating levels, it became less desirable.

1. The input resistance of power MOSFETs is high and they are voltage-controlled devices. So, in the MOSFET driving circuit for gate is simpler.
2. In comparison with bipolar transistors, the MOSFET has a very fast switching speed (typically up to 100 kHz) this is because of the fact that the absence of the minority carrier injection.

3. Power MOSFET does not have second breakdown.
4. Power MOSFETs are the easiest devices to parallel.
5. Due to positive temperature coefficient the MOSFETs have a good thermal stability.
6. We can easily turn it on or off.
7. The power MOSFET requires extremely small input power, due to very high input resistance.
8. The on-state resistance $R_{DS(ON)}$ is very small.
9. Power MOSFETs have very low noise figures than the power BJTs.
10. Power MOSFETs breakdown voltages is high due to the drift layer, as compared to small signal MOSFET.

1.2 Disadvantages

- The power dissipation of on-state is high.
- The blocking capacity of the MOSFET is asymmetric so the power MOSFET can block high forward voltage in the place of high reverse voltage. So, we have to add a diode to protect the MOSFET.
- Power MOS need special care while handling else they can get damaged due to static electricity.

1.3 Applications

The POWER MOSFET is the most used power semiconductor device. In 2010, as the report, it is seen that they capture 53% of the power device market, it captures the market better than the IGBT (27%), and BJT (9%), almost 60 billion power MOSFETs are dispatched yearly as of 2018. These include the trench POWER MOSFET, trench MOS are sold over 100 billion up to February 2017 and super junction MOSFET sold 5 billion units as of 2019.

- UPS
- RELAY DRIVER
- SMPS
- High-frequency inverters
- Used within power amplifiers
- In motor controlling

- Display driver

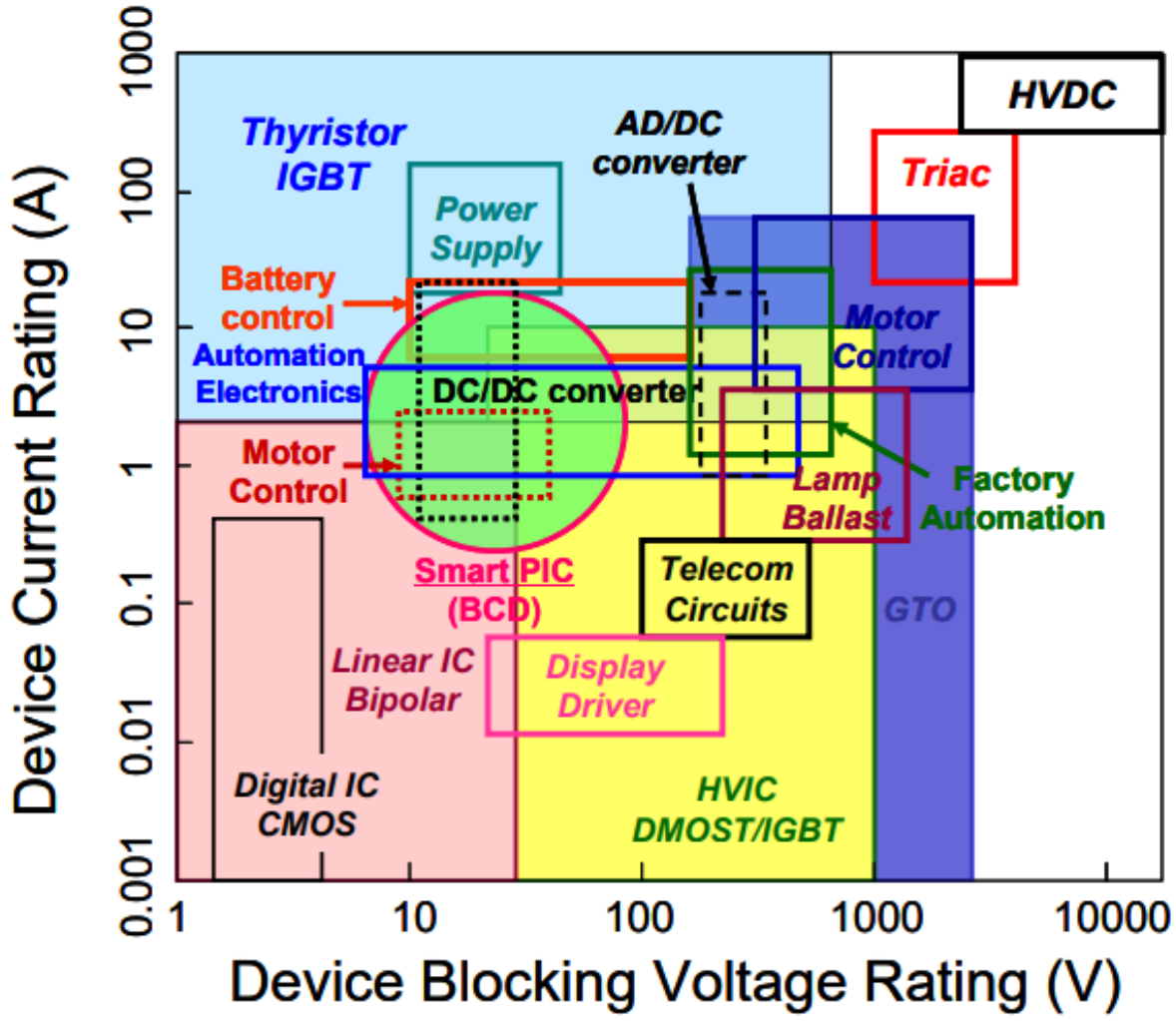

Fig:1.2 Power device applications and technologies, according to their voltages and current ratings.[2]

1.4 Basic Principle of MOS Device

The metal-oxide semiconductor field-effect transistor MOSFET [3] is the most popular field-effect transistor, which is used in both analog and digital circuits. It controls the electricity which can flow through the source and drain terminals based on the voltage applied to the gate terminal.

There are two types of MOSFET such as-

- **Depletion Mode**
- **Enhancement Mode**

1.4.1 Depletion Mode

When gate voltage is 0, the channel shows its maximum conductance and when the voltage on the gate is negative or positive, then reduces the channel conductivity.

1.4.2 Enhancement Mode

When V_{gs}=0 the device does not conduct. With increasing gate voltage, the device has conductivity also getting better.

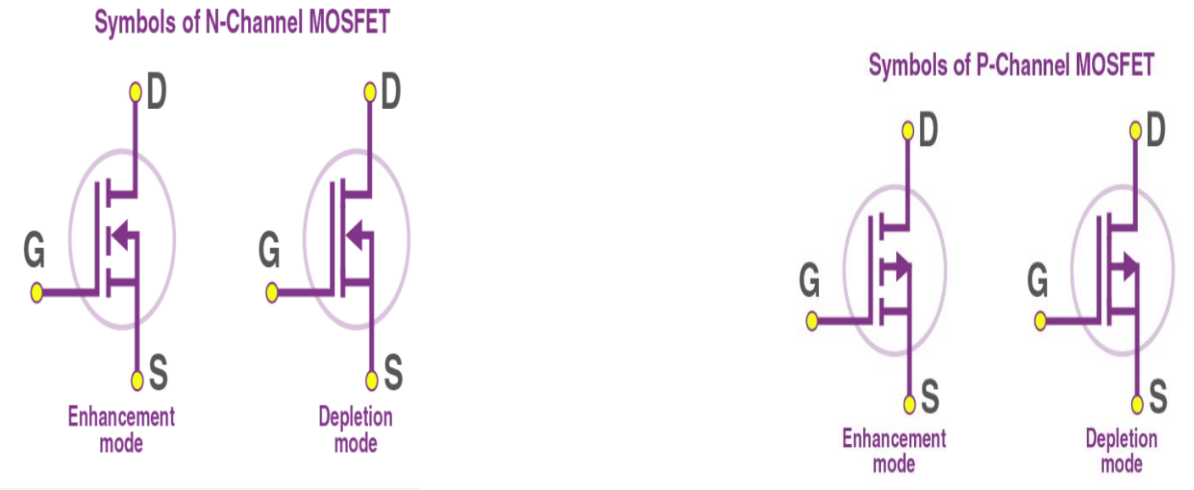

Fig:1.3 and 1.4 Symbols of MOSFETS [3]

1.4.3 P-Channel MOSFET

In P channel MOSFET, channel region between drain and source is p-type. It has four terminal gate(G), drain(D), source(S), body(B). the source and drain are heavily doped using p-type semiconductor and body or substrate is n-type.

1.4.4 N- Channel MOSFET

In N channel MOSFET, channel region between drain and source is n-type. It has four terminal gate(G), drain(D), source(S), body(B). the source and drain are heavily doped using n-type semiconductor and body or substrate is p-type.

1.5 TYPES OF POWER MOSFETS

There are two types of power MOSFETs are available:

(1) lateral and

(2) vertical power MOSFET.

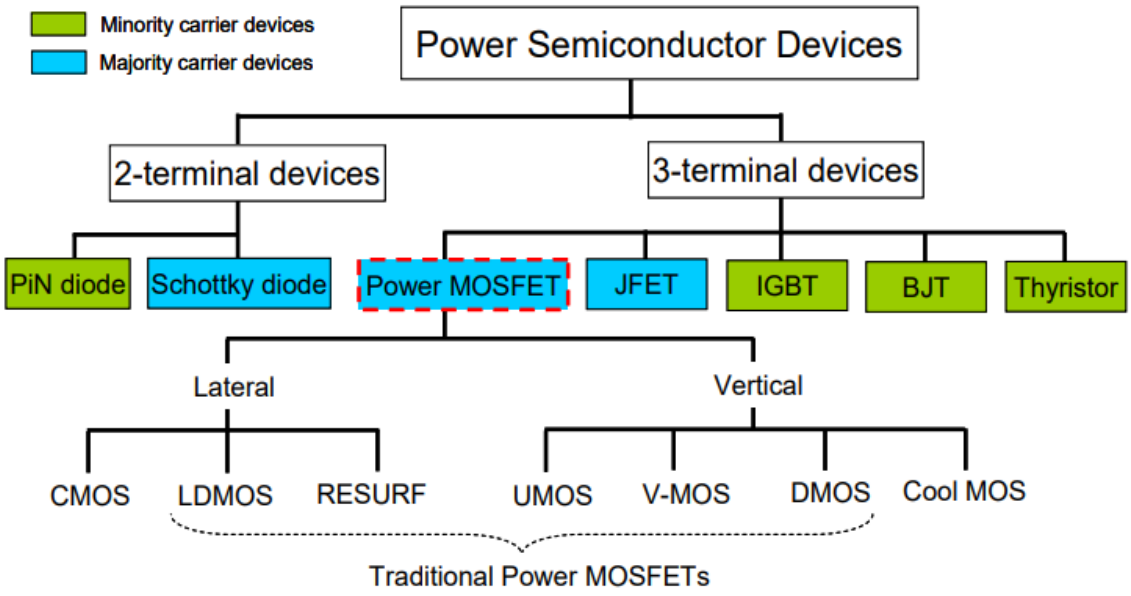

Fig: 1.5 different types of power semiconductor device [2]

1.6 TRADITIONAL VERTICAL MOSFETS

1.6.1 V-MOSFET

A VMOS [2] transistor is a one type of MOSFET. We can call VMOS as “V GROOV MOSFET’ or “VERTICAL METAL OXIDE SEMICONDUCTOR. The VMOS has a v shaped gate which allows the device to carry a high quantity of current from the source terminal to the drain terminal of the device. A wider channel is created for the shape of the depletion region, for this reason more current flows through it. When the device operates in blocking mode, in the N^+/p^+ junction the extreme electric field is seen. As the lower part of the groove has a sharp corner, it causes increase of electric field in the edge of the channel in the depletion region, due to high electric field the trench of the gate is damaged. Due to this reason, in present days the V-groove structure is not used in commercial devices.

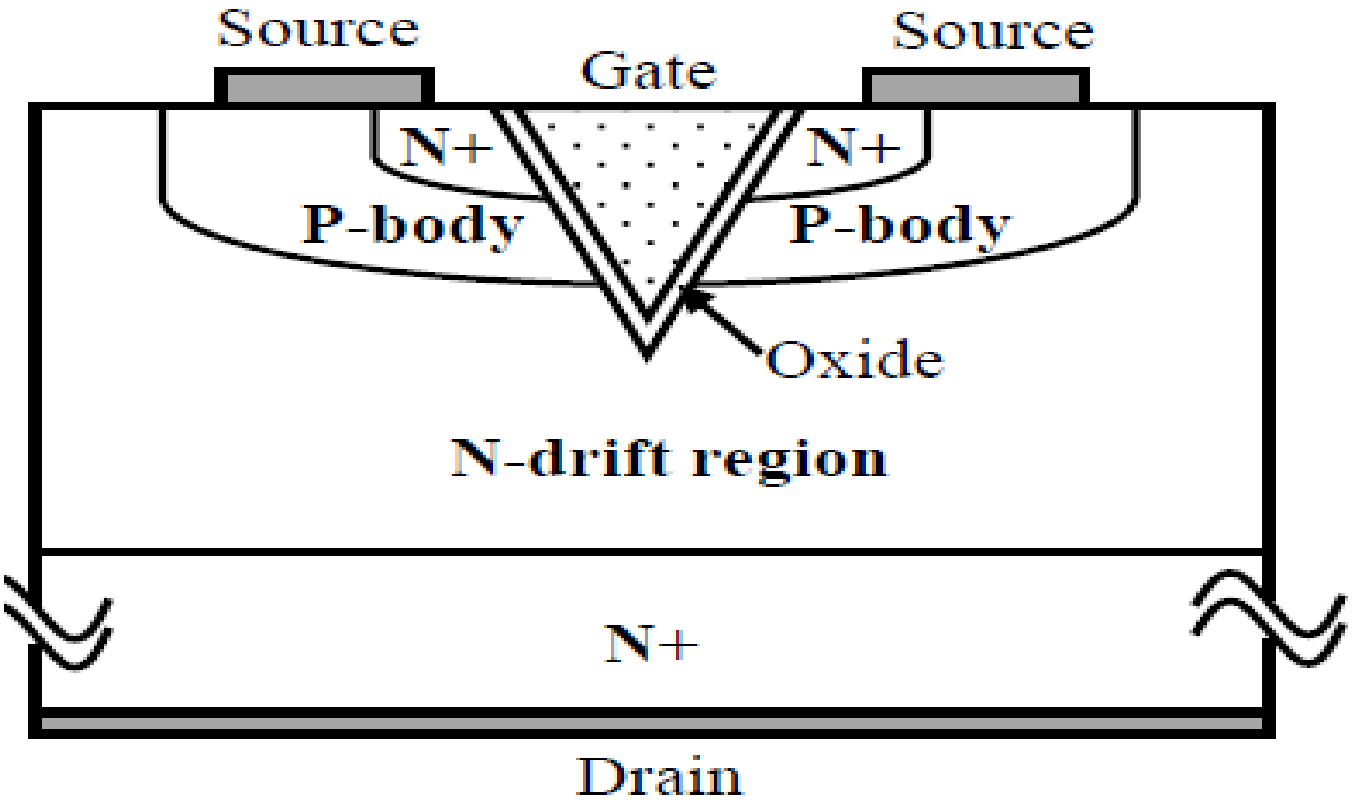

Fig: 1.6 Structure of V-MOSFET.[2]

VMOSFET Applications

- VMOS are used in switching power amplifiers.
- VMOS are used in Hi-fi audio power amplifiers.
- In broadband high-frequency amplifiers, VMOS are used.

1.6.2 DMOSFET

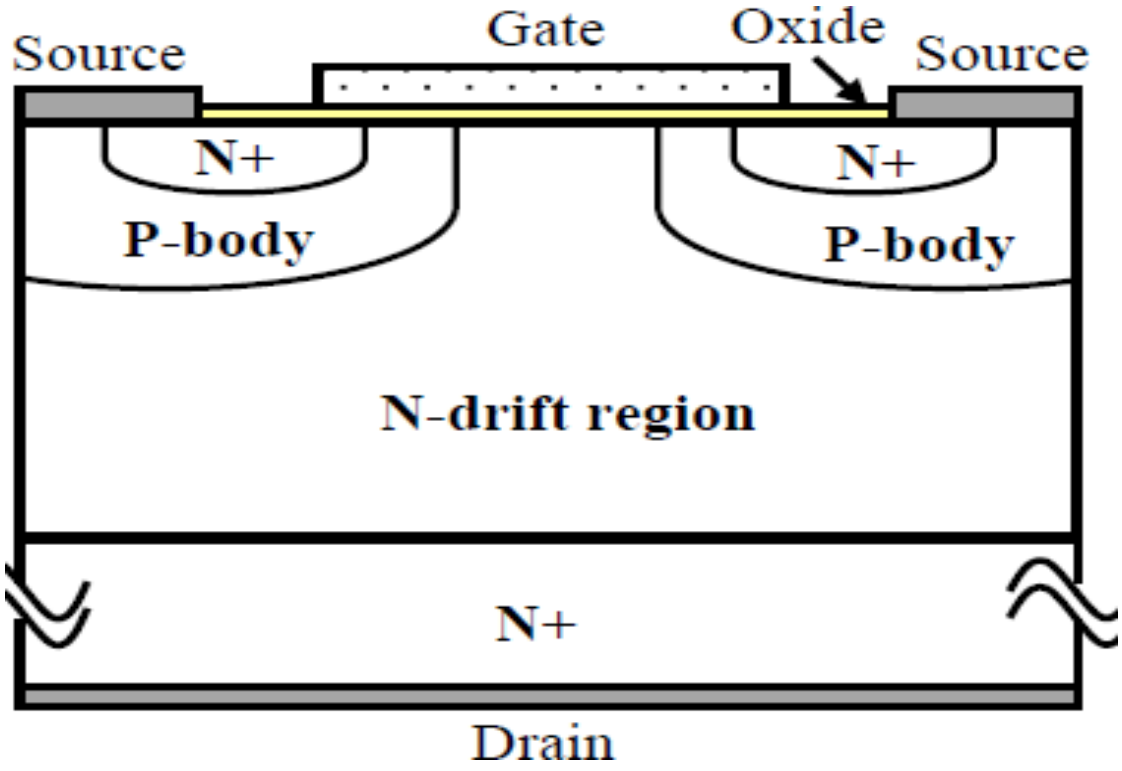

Fig: 1.7 Structure of DMOSFET [2]

DMOSFET [2] is called as double diffused MOSFET. The diffusion refers to the production process: the P-well is gotten by a diffusion process (i.e., a dual diffusion process is to create the P-body and N+ regions, hereafter the name double-diffused). DMOS are the replacement of the V-MOSFET to overcome the issue of high electric field in the tip of the V-groove. Above fig 1.7 shows the vertical structure of DMOS.

When V_g is bigger than threshold voltage and V_{ds} is positive, the current which is flowing in the DMOSFET, is going first horizontally across channel then goes towards the drain, horizontally. Further straight and

smaller current pathway can be reached when channel is positioned vertically. This thing takes important part to make the structure of the UMOSFET.

1.6.3 UMOSFET

In this kind of MOSFET the shape of the gate region like a U, so due to U-shaped gate region it is called as UMOSFET. Fig.1.8 is the configuration of UMOSFET. There are no JFET effect in this kind of MOSFET. The UMOSFET has higher doping concentration in channel region which is reason for low ON-resistance and also the oxide tip is not sharp (as in the V-MOSFET). Because by isotropic etching, the corners of the gate oxide can be curved. Due to the high electrical field, the gate oxide is damaged, to prevent this, p-body is planned to be, deeper.

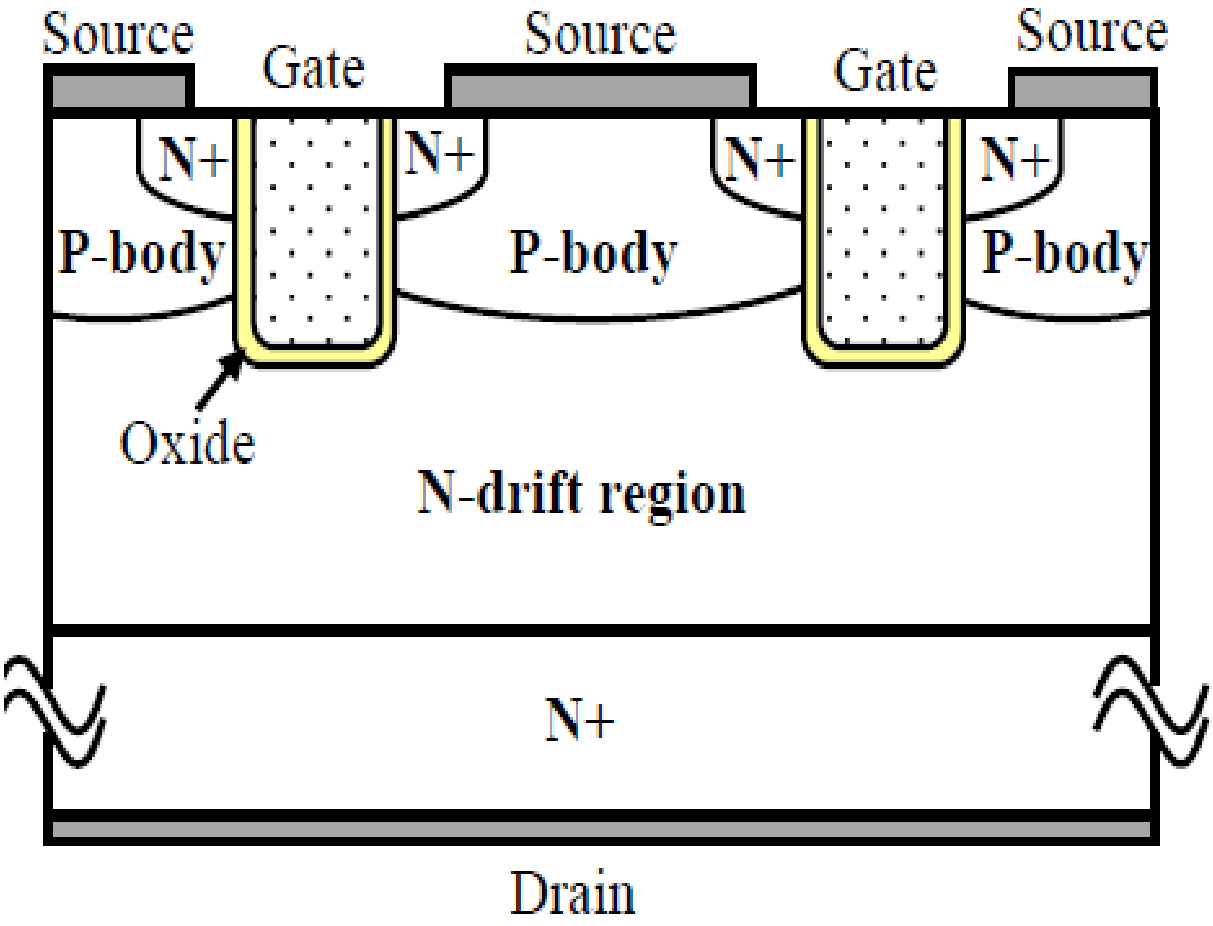

Fig: 1.8 Structure of UMOSFET [2]

UMOSFETs are appropriate for high-power applications as of the lack of the JFET region, it has low ON-resistance. The performance limitation of UMOSFETs is for high electric field at the gate oxide which create blocking voltage, where the trench extents the p-base region and exposed the gate oxide. To control this problem, a p^+ shielded region is added at bottom part in the trench. The p^+ shielded region efficiently guards gate oxide and recovers the breakdown voltage. The JFET resistance created by the p^+ shielded and the p-body regions meaningfully rises the ON-resistance. There are, many paths to decrease the JFET resistance effect. Like, by introducing an n-type current spreading layer [10-15] between the p-body is planned. Introducing an n-type region covering the p^+-SiC shielded region is projected. But in spite of several technical issues, the UMOS structure still proposed advantages over the DIMOS structure.

1.7 Wide Bandgap Semiconductors and POWER MOSFETS

Electricity generation is responsible for forty percentage of prime energy feeding in the United States. and in next few days it is predictable that the percentage of energy consumption will be higher. Progress of progressive power electronic devices with excellent productivity, consistency, functionality will deliver the world with a better benefit in placement of progressive power technologies. Furthermore, combination of advanced converters proposed considerable power saving options, by fundamentally more well-organized strategies, and by enabling higher levels of implementation for advanced applications.

Technical Opportunity

To achieving high power efficiency, it needs power semiconductor switches which have low power loss. Power silicon-based switch technology contains IGBTs, MOSFET.

Power semiconductor devices which are made of silicon have some significant restrictions. They are-

Switching Frequency:

Silicon based POWER MOSFETs require big die areas to retain conduction losses low. For this reason, at high switching frequencies, high gate capacitance produces losses and a huge

peak in current is seen. Silicon based IGBTs have small die in comparison MOSFETs because of conductivity modulation as well as for minority carriers also. As IGBT have high life time minority carriers so it decreases the switching frequency range.

Poor High-Temperature Performance:

Silicon has low bandgap so that becomes reason to high intrinsic carrier concentrations in POWER MOSFETs, for this reason at high temperatures huge leakage current is seen.

High Losses:

Silicon has low bandgap as well as low critical electric field (30 V/μm) for this reason it has considerable critical thickness. For large thickness the devices showed up huge conduction losses and as well as high resistance also.

As a result, opportunities for advanced productivity have developed with the progress of WBG [4] power semiconductor devices, for the fundamental differences in material properties between Si and **Gallium Nitride and Silicon Carbide, Gallium Oxide (Ga2O3) and Diamond** [5,6,7,8,9]. Higher electric fields in these wide band gap materials {≥ 2 MV/cm} allow narrower voltage-blocking layers with high doping concentration. For this reason, decrease of On-resistance are seen in comparison of an equivalent Si device. Low conduction losses and the high breakdown electric field mean that wide band gap materials can reach the same amount of blocking voltage as well as the on-resistance with a lesser form factor. This decreased capacitance permits higher frequency operation. Wide band gap materials have lower intrinsic carrier concentration which allows robust high-temperature & decrease leakage currents performance. WBG semiconductors have reduced cooling requirements, and small form factor power converters.

The use of SiC semiconductors in the design of power electronic devices and applications is quickly increasing. This is mainly for SiC having the qualities like high thermal conductivity, and chemical stability, high electron saturation velocity, high physical stability, The SiC MOSFETs are important candidate for high switching applications for the superior physical properties of SiC

Table:1.1 Properties of Silicon Carbide (4H-SiC), Gallium Nitride (GaN), $Ga_2\ O_3$, Silicon (Si), and Diamond. [6,7]

Propriety	**4H-SiC**	$Ga_2\ O_3$	**Si**	**GaN**	**Diamond**
Electron Mobility ($10^3\ cm^2$/V. s)	**0.9**	**0.3**	**1.3**	**1.5**	**2.00**
Breakdown Field (10^6 V/cm)	**3.0**	**8.0**	**0.3**	**3.5**	**13.0**
Thermal Conductivity (W/cm.k)	**3.7**	**0.1**	**1.5**	**1.3**	**22.9**
Saturation Drift Velocity (10^7cm/s)	**2.0**	**2.0**	**1.0**	**2.5**	**1.50**
Band Gap Energy (eV)	**3.2**	**4.7**	**1.1**	**3.4**	**5.50**

Table: 1.2 properties of Si,, 6H SiC, and 4H SiC , 3C SiC at 300 K [8,9]

Property	**3C SiC**	**Si**	**6H SiC**	**4H SiC**
Thermal conductivity, θ_κ(W/cm. K)	**5**	**1.5**	**4.9**	**4.9**
Energy gap, E_g(eV)	**2.39**	**1.12**	**3.03**	**3.26**
Electron drift velocity,v_{sat} (x10^7 cm/s)	**2.5**	**1**	**2**	**2**
Electron mobility, μ_n (cm^2 /Vs)	**750**	**1400**	**370^1**	**800^1**
Hole mobility, μ_p (cm^2 /V. s)	**40**	**600**	**90**	**115**
Dielectric constant, ε	**9.7**	**11.8**	**9.7**	**9.7**
Critical Field, E_c (MV/cm)	**1.5**	**0.3**	**3.2**	**3**

1: perpendicular to c-axis

OBJECTIVE OF THE THEISIS

In this thesis, UMOSFET structure made of SiC with an additional n-type region at the bottom of the trench is studied. A n-type region is added in the drift layer for that reason depletion region is decreased as a result ON-resistance of the modified-UMOS is reduced. Here we have compared the ON-resistance of modified UMOSFET with varying the trench depth. In the results we will see that the ON-resistance of the device is decreasing gradually, with increasing the trench depth,

Next in chapter 2 literature survey is presented. In Chapter 3 the device structure and the simulation has been described. Chapter 4 involves the results and discussion. In Chapter 5, Conclusion is presented.

REFERENCES

[1] B.J Baliga, “Power Semiconductor Devices”,2nd edition,2008, ISBN 0-534-94098-6.

[2] Abraham Yoo,” Design, Implementation, Modeling, and Optimization of Next Generation Low-Voltage Power MOSFETs “, Department of Materials Science and Engineering University of Toronto,2010

[3] CMOS DIGITAL INTEGRATED CIRCUITS Analysis and Design by SUNG-MO (STEVE) KANG, University of Illinois at Urbana- Champaign, YUSUF LEBLEBIGI Worcester Polytechnic Institute Swiss Federal Institute of Technology-Lausanne, 5th edition,2005

[4] Isik C. Kizilyalli, Eric P. Carlson, Daniel W. Cunningham, Joseph S. Manser, Yanzhi “WIde Band-Gap Semiconductor Based Power Electronics for Energy Efficiency”, “Ann” Xu, Alan Y. Liu March 13, 2018 United States Department of Energy Washington, DC 20585

[5] L. F. S. Alves, P. Lefranc, P. Jeannin, and B. Sarrazin., “Review on SiC-MOSFET devices and associated gate drivers”, In Feb2018 IEEE International Conference on Industrial Technology (ICIT), pages 824–829

[6] L. F. S. Alves, R. C. M. Gomes, P. Lefranc, R. De A. Pegado, P. Jeannin, B. A. Luciano, and F. V. Rocha,”Sic power devices in power electronics: An overview”,In 2017 Brazilian Power Electronics Conference (COBEP), pages 1–8, Nov 2017.

[7] Luciano FS Alves, Gutemberg G dos Santos Jr, and Mateus C Lucena. ‘Transistores hemt gan:” Uma nova expectativa na eletrônica de potência. Jornal do Pet Elétrica (Brazilian magazine). issn: 2316-5863., 2017.

[8] J. Zhang,” Power electronics in future electrical power grI_ds”. In 2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pages 1–3, July 2013.

[9] A. K. Agarwal,” An overview of sic power devices”, In Nov 2010 International Conference on Power, Control and Embedded Systems, pages 1–4,

[10] K. Ueno and T. Oikawa, "Counter-doped MOSFETs of 4H-SiC," in *IEEE Electron Device Letters*, vol. 20, no. 12, pp. 624-626, Dec. 1999, doi: 10.1109/55.806105.

[11] S. Sridevan and B. Jayant Baliga, "Lateral n-channel inversion mode 4H-SiC MOSFETs," in IEEE Electron Device Letters, vol. 19, no. 7, pp. 228-230, July 1998, doi: 10.1109/55.701425.

[12] J. Kim and K. Kim, "Single-Event Burnout Hardening 4H-SiC UMOSFET Structure," in IEEE Transactions on Device and Materials Reliability, vol. 22, no. 2, pp. 164-168, June 2022, doi: 10.1109/TDMR.2022.3151704.

[13] Y. Wang, J. -c. Zhou, M. Lin, X. -j. Li, J. -Q. Yang and F. Cao, "A Comparative Study of Single-Event-Burnout for 4H-SiC UMOSFET," in IEEE Journal of the Electron Devices Society, vol. 10, pp. 373-378, 2022, doi: 10.1109/JEDS.2022.3158810.

[14] D. Bharti and A. Islam, "Optimization of SiC UMOSFET Structure for Improvement of Breakdown Voltage and ON-Resistance," in IEEE Transactions on Electron Devices, vol. 65, no. 2, pp. 615-621, Feb. 2018, doi: 10.1109/TED.2017.2779482.

[15] Jue Wang and B. W. Williams, "Evaluation of high-voltage 4H-SiC switching devices," in IEEE Transactions on Electron Devices, vol. 46, no. 3, pp. 589-597, March 1999, doi: 10.1109/16.748883.

CHAPTER 2: LITERATURE SURVEY

1.In this paper [1], authors have proposed an improved effectiveness of U-shaped trench-gate MOSFET or we can call it UMOSFET structure which is made of SiC. The projected device structure takes benefit of a added p^+polySi/SiC region which helps the device to decrease ON-resistance. The heterojunction diode created by the p^+-polySi and the n-drift regions makes improvements in body diode effect, and also decreases the reverse recovery charge. Authors also demonstrate that projected device structure offers a 56.5% development in the FOM (figure of merit), and decrease in ON-resistance and reverse recovery charge.

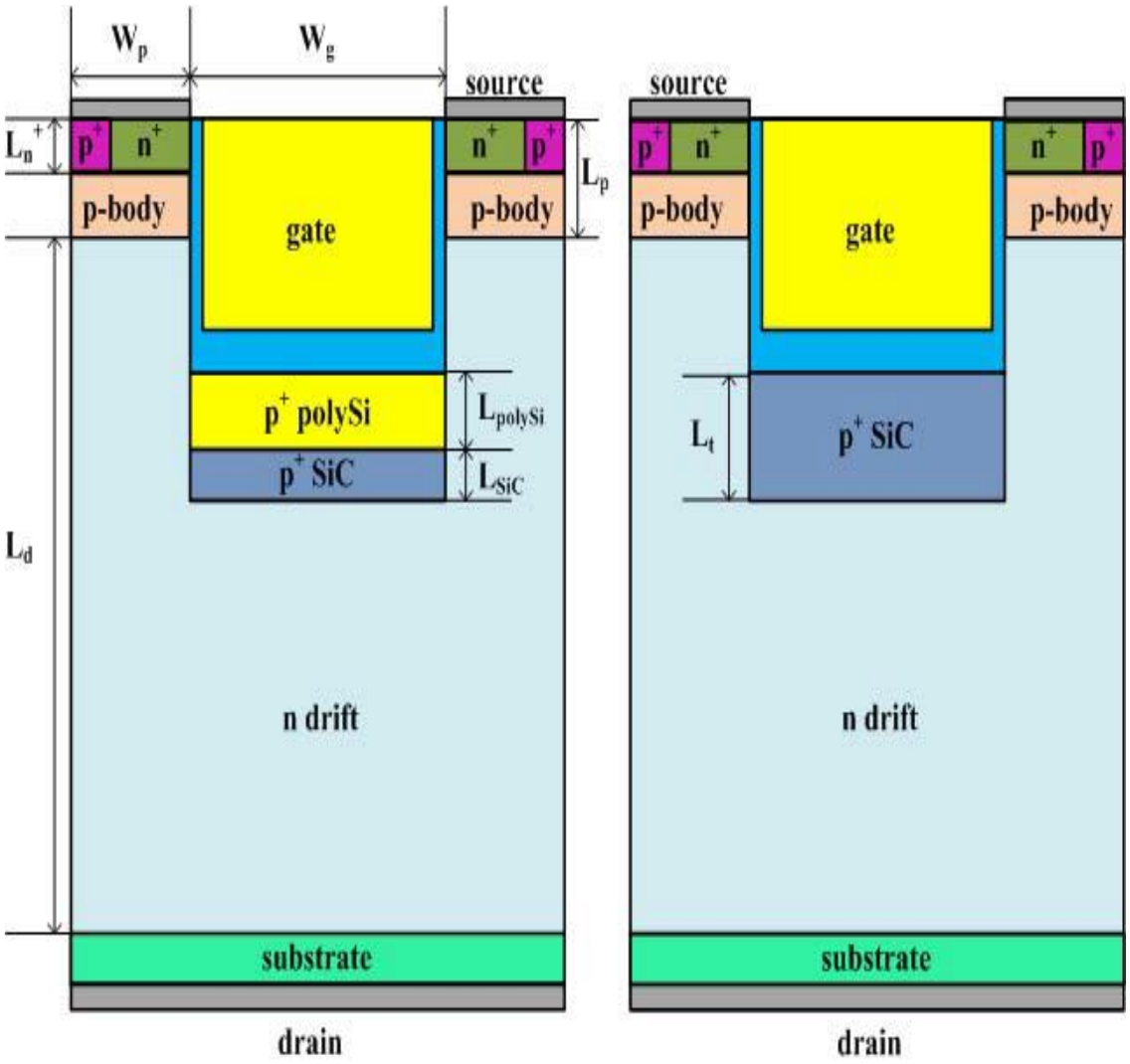

Fig: 2.1 The proposed structure [1]

2.In this paper [2] authors have work on 4H-SiC Trench p-n junction Gate MOSFET with p^+ shield to reduce ON-Resistance and as well as to reduce switching loss. In this work, authors have designed 4H-SiC UMOSFET. The structure of the MOSFET included a n-type region at the drift region, is proposed which reduces the ON-resistance while maintaining the breakdown voltage. Here, the gate structure is made of p- n junction which decrease the switching loss. In order to simulate the device, authors have used Sentaurus TCAD. SiC based UMOSFETs generally lack JFET resistance and exhibits low channel density thereby possessing lower values of ON-resistance. However, a high electric field is attached with the gate dielectric while operating the device at high drain bias. This dilemma can be well resolved by offering a adjustment to the present structure and adding a p^+ shielding region at the lower part of the trench. This area acts as a protection for the gate dielectric on one side while enhancing the ON-resistance due to the inclusion of a JFET resistance comprising of p^+ shielding region, drift region and p-body region, which adds to the benefit of the device. In this work, authors have upgraded the 4H-SiC UMOSFET structure by incorporating an additional n-type region at the drift region and a p-n junction in the trench with the primary aim of reducing the ON-resistance and the dynamic power dissipation.

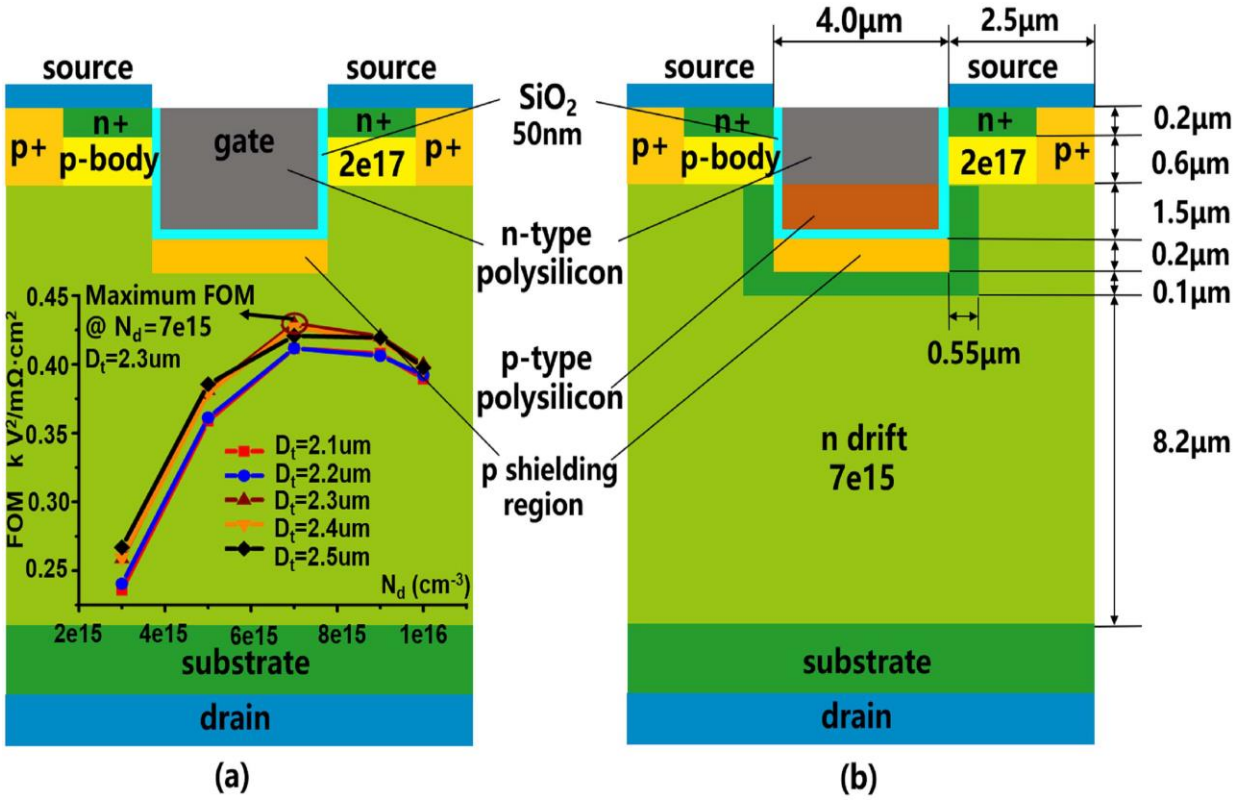

Fig: 2.2 Schematic diagram of the proposed device.[2]

3. In this paper [3] authors have designed and fabricated of UMOSFETs with specific on-resistances of 105.1m$\Omega.cm^2$,and the blocking voltage is 5.05kV and the current density is 100 A/cm^2. To guard the gate oxide from the device's high electric fields, these kinds of devices incorporate a long self-aligned p bottom implant. A shadow implant cover was created to protect the device's sidewalls from somewhat undesirable p-bottom implant. Thease MOSFETs are the 1st to contain a post-oxidation anneal in nitric oxide to development of the inversion layer of electron mobility. A solo zone JTE which peak blocking voltage (7.5kV) was executed in the proposed device.

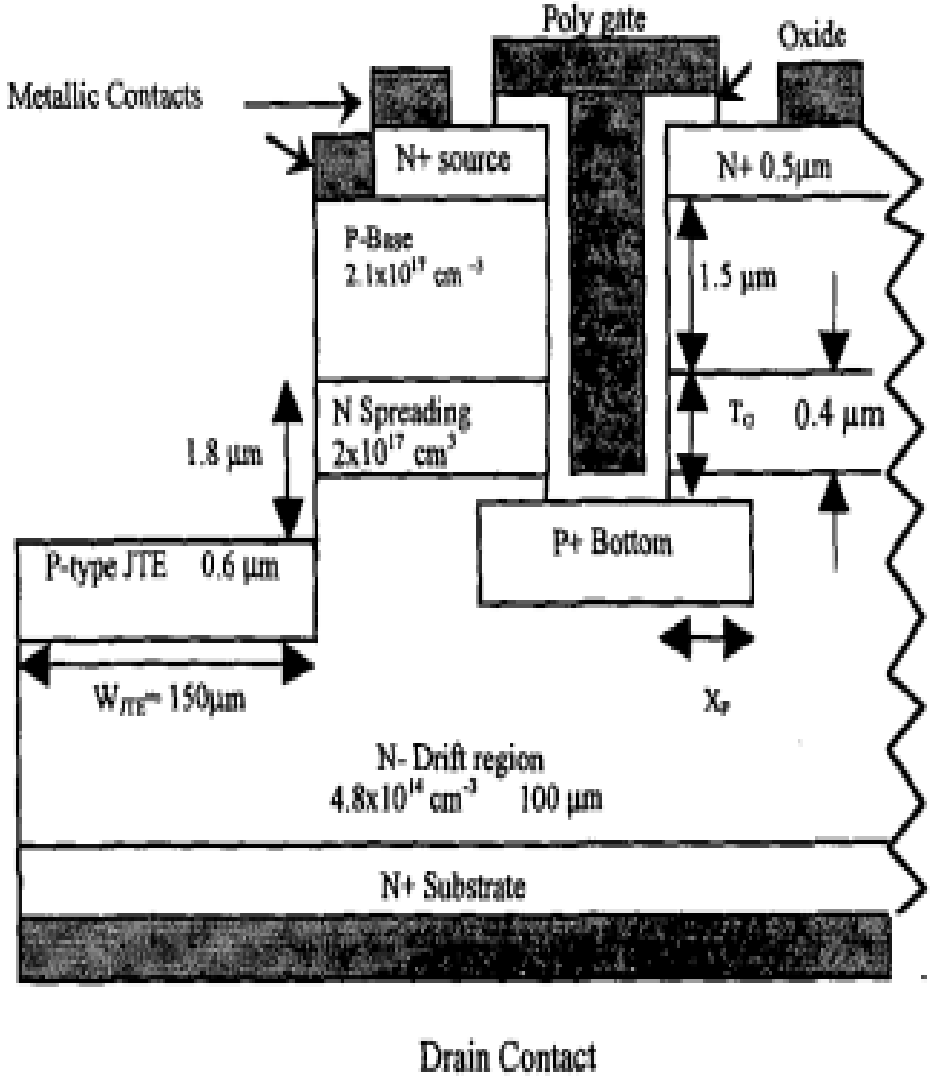

Figure:2.3 Schematic diagram of the proposed UMOSFET. [3]

4.In this paper [4] authors have discussed about Vertical trench-gate metal–oxide–semiconductor field-effect transistors in 4H-SiC having together junction termination extension & trench oxide protection are stated for the 1st time. Structures are fabricated without and with counter-doped channels. In doped-channel FETs, blocking voltages is 3360 V and specific ON-resistances is 199 m$\Omega.cm^2$ and for FETs without doped channels blocking voltage is 3055V and ON-resistance121 m$\Omega.cm^2$. This kind of blocking voltage is the maximum stated till date for the case of UMOSFETs in SiC.

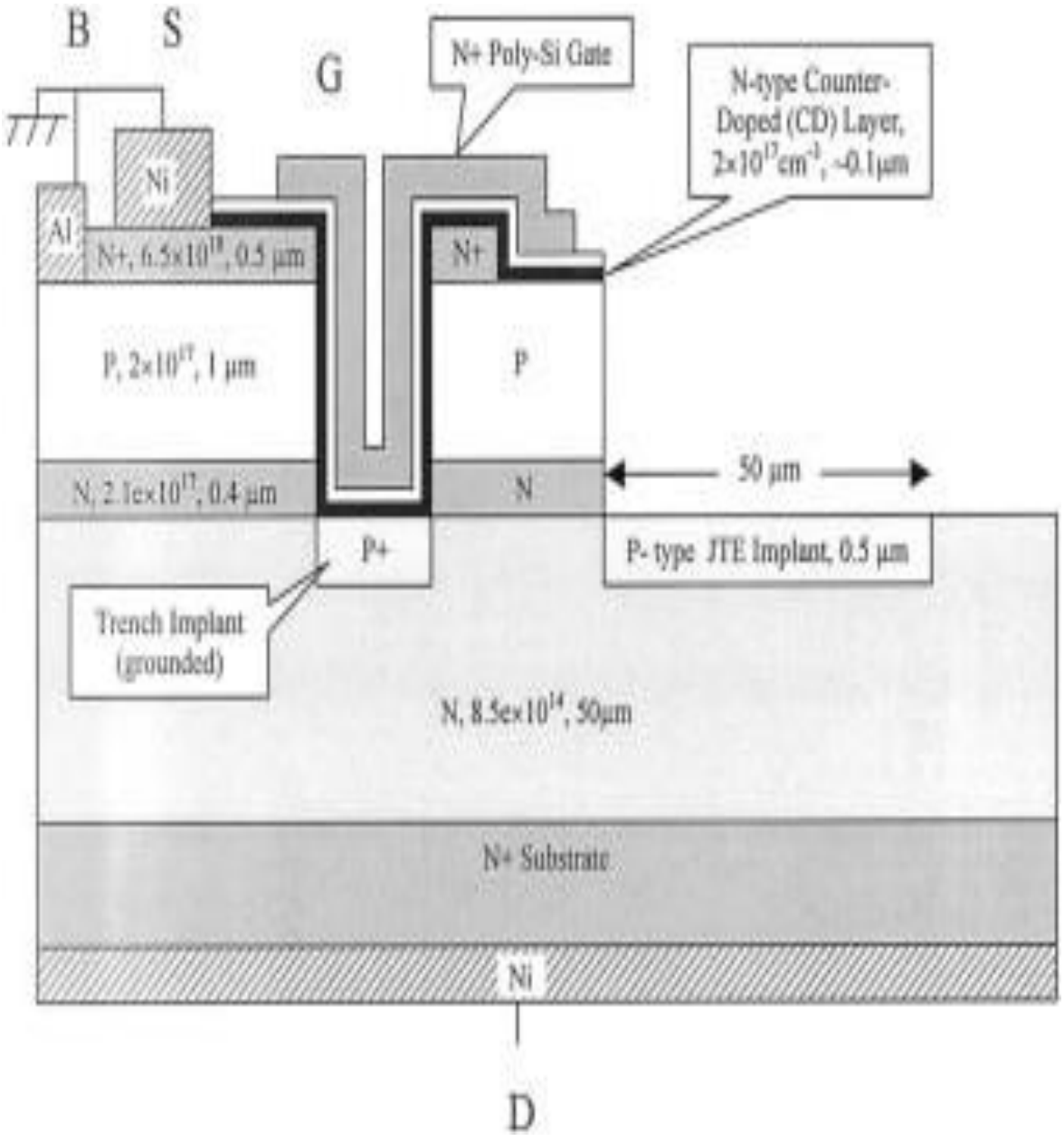

Fig: 2.4 Cross section of the doped-channel UMOSFET [4]

REFERENCES

[1] X. Zhou, R. Yue, J. Zhang, G. Dai, J. Li, and Y. Wang, “4H-SiC trench MOSFET with floating/grounded junction barrier-controlled gate structure,” IEEE Trans. Electron Devices, vol. 64, no. 11, pp. 4568–4574, Nov. 2017. doi: 10.1109/TED.2017.2755721

[2] Kai Tian , Anders Hallén, Jinwei Qi , Shenhui Ma , Xinxing Fei, Anping Zhang , and Weihua Liu, “An Improved 4H-SiC Trench-Gate MOSFET With Low ON-Resistance and Switching Loss”, in *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2307-2313, May 2019, doi: 10.1109/TED.2019.2905636.

[3] I. A. Khan, J. A. Cooper, M. A. Capano, T. Isaacs-Smith and J. R. Williams, "High-voltage UMOSFETs in 4H SiC," Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics, 2002, pp. 157-160, doi: 10.1109/ISPSD.2002.1016195.

[4] Y. Li, J. A. J. Cooper and M. A. Capano, "High-voltage (3 kV) UMOSFETs in 4H-SiC," in IEEE Transactions on Electron Devices, vol. 49, no. 6, pp. 972-975, June 2002, doi: 10.1109/TED.2002.1003714.

CHAPTER 3: DEVICE STRUCTURE AND SIMULATION

SiC is a standard choice in case of high temperature and high-power applications because of its high critical field and wide bandgap qualities [1][3]. SiC MOSFET is a good candidate for advanced power switching devices for its physical properties [1], [2], [3]. Conventional SiC U-shaped trench gate MOSFETs have high switching speed as it has the low ON-resistance as there is no parasitic JFET [1][4]. At high drain voltages, during the device operation, gate oxide is suffering from a high electric field. This problem arises because of high electric field in drift region, the trench spans the p-body region for this reason the gate oxide is exposed at the bottom of the trench [1], [2] [6-13]. To overcome the problem, In the structure a p^+shielding region is added at the bottom of the trench. The p^+shielding region guards the gate oxide. But when p^+shielding region is added, it increases the total ON-resistance as it introduces a JFET region composed of the drift region, p-body region, and p^+shielding region. To reduce the total ON-resistance, a n-type region is added, covering the p shielding region at the bottom of the trench gate.

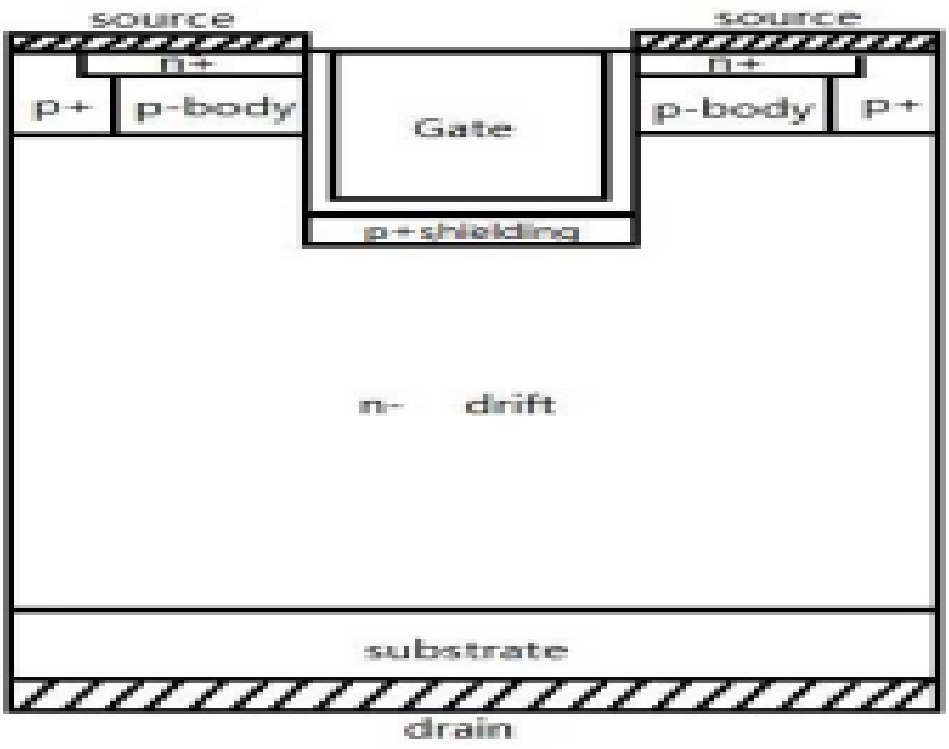

Fig:3.1 Conventional p^+shielding UMOSFET [4]

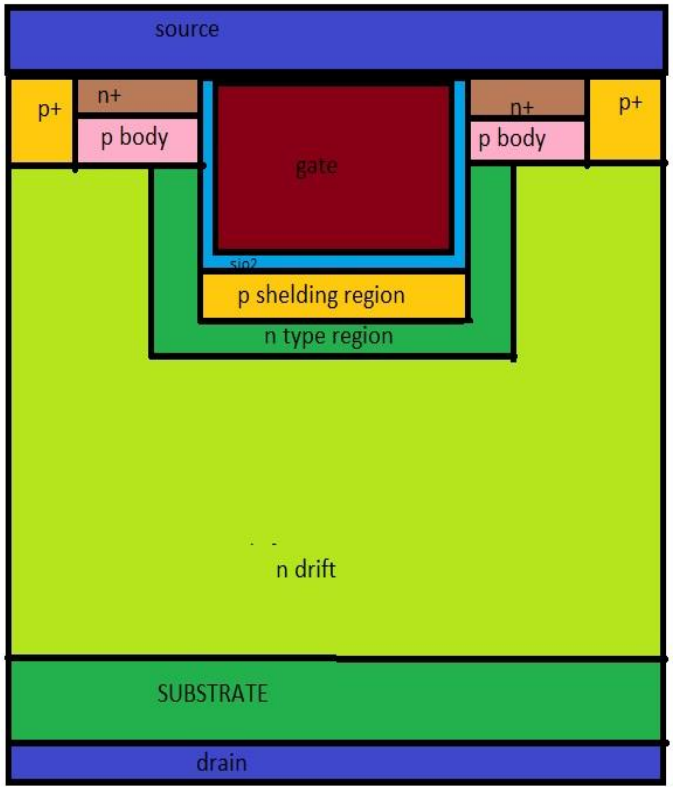

Fig:3.2 Cross-sectional views of the improved UMOS

Fig:3.1 Shows of the conventional UMOS. Fig:3.2 shows the improved-UMOS. In the structure, silicon carbide is used for the substrate region, n-drift region, n^+ regions and n type region, p body region, and p^+regions. In gate region n type polysilicon is used. In gate oxide SiO2 is used. Source and drain contact are made of metal. Structure parameters are shown in table no: 3.1. The gate oxide (for the bottom and both sidewalls) is 50 nm thick. Gate region thickness is 2.25um. The p^+shielding region thickness is 0.2 µm. N drift region width is 10um. p^+regions thickness is 0.8 µm. n^+regions thickness is 0.2 µm. P body region thickness is 0.6 µm. Substrate region thickness is 0.5 µm. Source contact thickness is 1.2 µm. Drain contact thickness is 1.5 µm. The gate region is doped with phosphorus and its doping concentration is 7×10^{20} $cm^{-3.}$ The n type region is doped with phosphorus and its doping concentration is 5×10^{16} $cm^{-3.}$ The n drift region is doped with phosphorus and its doping concentration is 7×10^{15} $cm^{-3.}$ The.n^+ regions are doped with phosphorus and its doping concentration is· 2×10^{20} $cm^{-3.}$ The substrate region is doped with phosphorus and its doping concentration is· 7×10^{20} $cm^{-3.}$ The p^+ shielding region is doped with boron and its doping concentration is 2×10^{18} $cm^{-3.}$ The p^+regions are doped with boron and its doping concentration is 2×10^{20} $cm^{-3.}$ The p body

regions are doped with boron and its doping concentration is 2×10^{17} $cm^{-3.}$ In the structure of improved UMOS, the n-type region has higher doping concentration than that of the n-type drift region and for this reason it reduces the depletion region which is introduced by p^{+}shielding region. A reduced depletion region offers a wider space for the electrons and decreases the JFET resistance. It improves the ON-resistance further. The added n-type region decreases the vertical depletion region which is formed by the p^{+} shielding region, letting the electrons to spread out earlier in the horizontal direction. In this thesis paper, I am varying the trench depth. I have verified the characteristics of the improved p^{+}shielding UMOSFET with an added n-type region with simulations using Sentaurus TCAD. The electron/hole equations of continuity and the Poisson equation are solved, with Avalanche recombination. doping-dependent mobility, high-field saturation mobility, band narrowing. By Sentaurus Structure Editor at I have drawn the improved UMOSFET structure which is seen in the fig no 3.2. In the structure I have taken 3 regions for meshing.one is overall region second one is for gate interface region and third one is for channel region. The meshing structure and doping concentration are seen in fig:3.3 and 3.4 and 3.5. In this thesis paper, I have compared the characteristics of improved UMOSFET with the conventional structure.

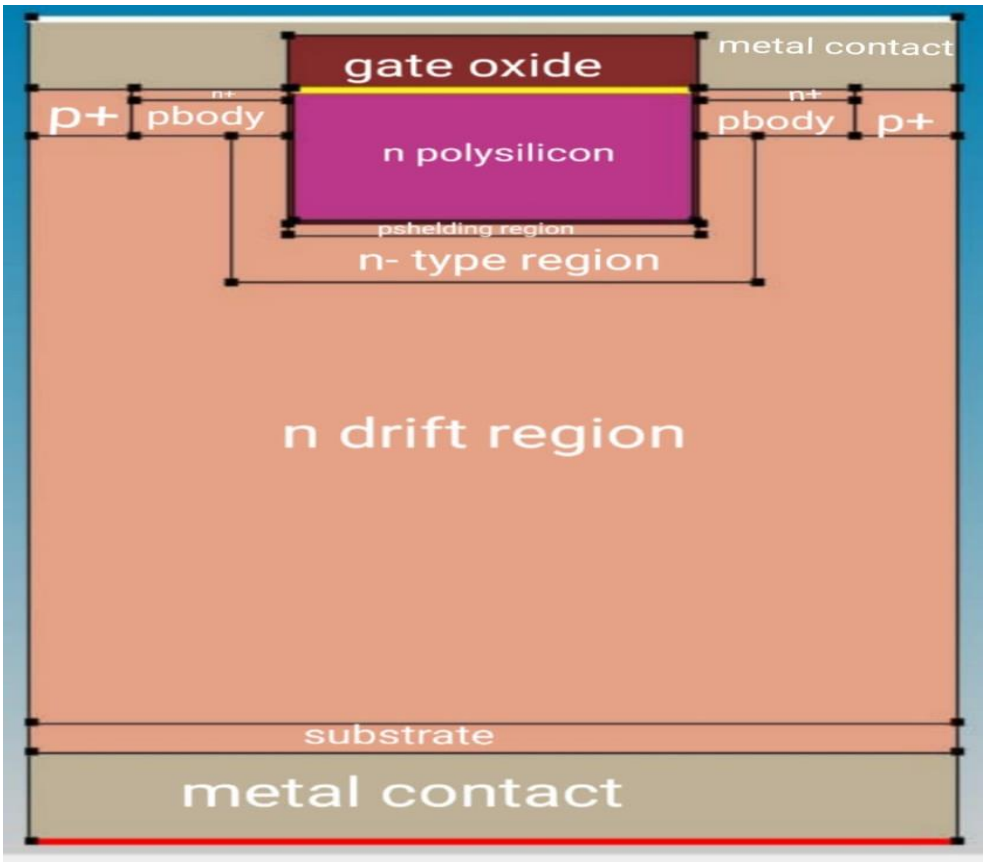

Fig:3.3 Structure of UMOS in SDE

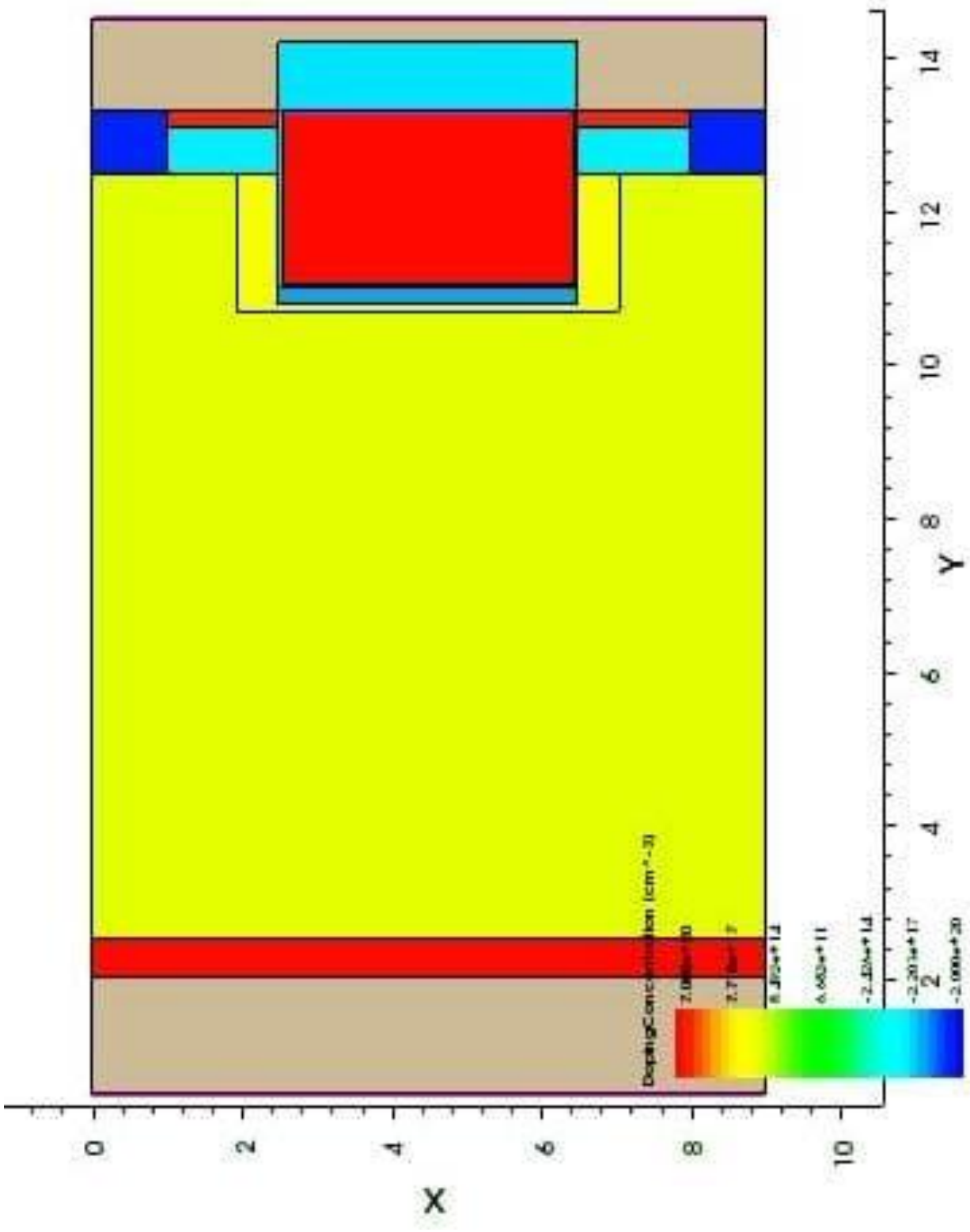

Fig:3.4 Schematic diagram with doping concentration.

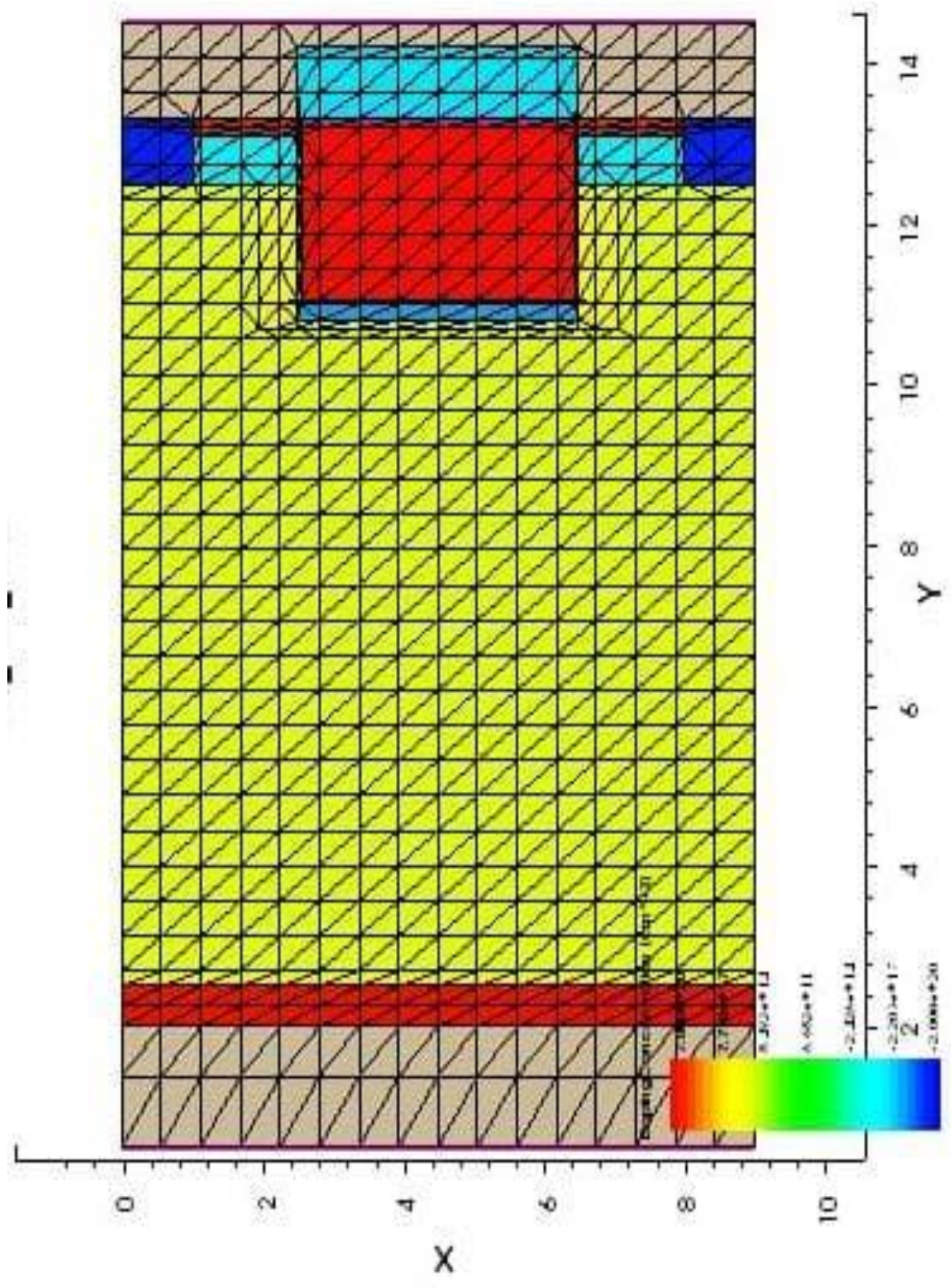

Fig :3.5 Schematic diagram with meshing

In Sentourus TCAD structure part is done in sde. For device physics we have to use Sentaurus Device section. In this section there is one part called physics section.in physics part we have to put different kind of models to run the structure. Here in my thesis paper, I have used different kind of models and they are doping-dependent, high-field saturation, Enormal, eAvalanche, hAvalanche, EffectiveIntrinsicDensity (Bandgap Narrowing (Slotboom)

Table 3.1 Models name and their working [5]

MODEL NAME	MODEL WORKING
Doping Dependence	To calculate mobility, it is used.
High-field saturation	Highfield Saturation can be specified eHighFieldSaturation for electrons and it is a function of the effective field experienced by the carrier in its direction of motion.
Enormal	It is used for mobility calculation
eAvalanche and hAvalanche	The eAvalanche and hAvalanche specify driving forces or separate models for the hole and electron ionization coefficients
EffectiveIntrinsicDensity, Bandgap Narrowing, Slotboom	These are bandgap narrowing model.

TABLE: 3.2 DEVICE PARAMETERS FOR THE SIMULATIONS

REGION NAME	MATERIAL	THICKNESS (μm)	DOPING CONCENTRAION (cm^{-3})	DOPING MATERIAL
GATE	N TYPE POLY SILICON	2.25	7×10^{20}	PHOSPHORUS
SiO_2 LAYER	SiO2	0.05	-	-
p^+ SHELDING REGION	SILICON CARBAIDE	0.2	$2x10^{18}$	BORON
N TYPE REGION	SILICON CARBAIDE	variable	5×10^{16}	PHOSPHORUS
N DRIFT	SILICON CARBAIDE	10	7×10^{15}	PHOSPHORUS
p^+ REGIONS	SILICON CARBAIDE	0.8	2×10^{20}	BORON
n^+ REGIONS	SILICON CARBAIDE	0.2	$2x10^{20}$	PHOSPHORUS
PBODY REGIONS	SILICON CARBAIDE	0.6	2×10^{17}	BORON
SUBSTRATE REGION	SILICON CARBAIDE	0.5	7×10^{20}	PHOSPHORUS
SOURCE CONTACT	METAL	1.2	-	-
DRAIN CONTACT	METAL	1.5	-	-

Reference

[1] Y. Li, J. A. Cooper, Jr., and M. A. Capano, “High-voltage (3 kV) UMOSFETs in 4H-SiC,” IEEE Trans. Electron Devices, vol. 49, no. 6, pp. 972–975, Jun. 2002

[2]] B. J. Baliga,” Silicon Carbide Power Devices.” Singapore: World Scientific, 2005.

[3] N. Ericson et al., “A 4H silicon carbI_de gate buffer for integrated power systems,” IEEE Trans. Power Electron., vol. 29, no. 2, pp. 539–542, Feb. 2014

[4] I. A. Khan, J. A. Cooper, Jr., M. A. Capano, T. Isaacs-Smith, and J. R. Williams, “High-voltage UMOSFETs in 4H SiC,” in Proc. 14th ISPSD, Jun. 2002, pp. 157–160.

[5] Sentaurus™ Device User GuI_de Version J-2014.09, September 2014

[6] Y. Wang, Y. Ma, Y. Hao, Y. Hu, G. Wang, and F. Cao, “Simulation study of 4H-SiC UMOSFET structure with p+−polySi/SiC shielded region,” IEEE Trans. Electron Devices, vol. 64, no. 9, pp. 3719–3724, Sep. 2017. doi: 10.1109/TED.2017.2723502

[7] Kai Tian, Anders Hallén, Jinwei Qi , Shenhui Ma , Xinxing Fei, Anping Zhang , and Weihua Liu, “An Improved 4H-SiC Trench-Gate MOSFET With Low ON-Resistance and Switching Loss”, in *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2307-2313, May 2019, doi: 10.1109/TED.2019.2905636.

[8] K. Ueno and T. Oikawa, "Counter-doped MOSFETs of 4H-SiC," in *IEEE Electron Device Letters*, vol. 20, no. 12, pp. 624-626, Dec. 1999, doi: 10.1109/55.806105.

[9] S. Sridevan and B. Jayant Baliga, "Lateral n-channel inversion mode 4H-SiC MOSFETs," in IEEE Electron Device Letters, vol. 19, no. 7, pp. 228-230, July 1998, doi: 10.1109/55.701425.

[10] J. Kim and K. Kim, "Single-Event Burnout Hardening 4H-SiC UMOSFET Structure," in IEEE Transactions on Device and Materials Reliability, vol. 22, no. 2, pp. 164-168, June 2022, doi: 10.1109/TDMR.2022.3151704.

[11] Y. Wang, J. -c. Zhou, M. Lin, X. -j. Li, J. -Q. Yang and F. Cao, "A Comparative Study of Single-Event-Burnout for 4H-SiC UMOSFET," in IEEE Journal of the Electron Devices Society, vol. 10, pp. 373-378, 2022, doi: 10.1109/JEDS.2022.3158810.

[12] D. Bharti and A. Islam, "Optimization of SiC UMOSFET Structure for Improvement of Breakdown Voltage and ON-Resistance," in IEEE Transactions on Electron Devices, vol. 65, no. 2, pp. 615-621, Feb. 2018, doi: 10.1109/TED.2017.2779482.

[13] Jue Wang and B. W. Williams, "Evaluation of high-voltage 4H-SiC switching devices," in IEEE Transactions on Electron Devices, vol. 46, no. 3, pp. 589-597, March 1999, doi: 10.1109/16.748883.

CHAPTER 4: THE OUTCOMES AND DISCUSSION

Here we finally obtain the necessary results along with the discussions thereby explaining the situation physically and drawing an agreement with the graphical observation. The plots are obtained after writing necessary programs in Sentourus TCAD.

4.1 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH OF MODIFIED UMOSFET

When we apply a small positive voltage V_{ds} between drain and source [5]of the device, the voltage V_{ds} is the reason for which the current is flowing through the induced n channel. Free electrons carry the current by moving from source terminal to drain terminal. The current flows in the opposite of negative charge so the current in the channel, I_d will be from drain terminal to source terminal. The density of electrons in the channel depends on the magnitude of V_{gs} (gate voltage). The magnitude of I_d depends on density of electrons. For V_{gs} =V_t (threshold voltage, the channel is just made and the current conducted is still insignificantly low. When gate voltage surpasses threshold voltage, large amounts of electrons are attracted into the channel. We see that when we increase in the channel depth the charge carriers in the channel also increases. As a result, conductance is increased in the channel and resistance is decreased. The channel conductance is proportional to the (V_{gs} - V_t), where (V_{gs} - V_t) is the additional gate voltage which is called overdrive or effective voltage. Which follows that the current I_d, will be proportional to the (V_{gs} - V_t) V_{ds}. So, when V_{ds} is small the device operates as linear resistor, and V_{gs} is controlling its value. The resistance is unlimited for V_{gs} <=V_t and its value will be decreases as V_{gs} exceeds V_t.

Operation as V_{ds} is Increased

For the next case consider the V_{ds} is increased when V_{gs} is constant and at a value that is greater than V_t. Across the channel from source terminal to drain terminal, the voltage increases from zero to V_{ds} Thus, the voltage among points along channel and gate is reduced from V_{gs} to (V_{gs} -V_{ds}) at the source end to the drain end. On this voltage, depth of the channel is dependent, so the channel is no longer of even depth; the channel will be thinnest at drain terminal end and

deepest at source end. When V_{ds} is increased, the channel turns into narrower and its resistance rises. Thus, the I_d -V_{ds}curve bends and it is not increasing linearly. When $V_{ds}$is increased to the value that decreases the voltage between gate and channel at the end of drain terminal to V_t (threshold voltage), then we can say that

V_{gd}=V_t

or (V_{gs} -V_{ds}) = V_t

or V_{ds}= (V_{gs} -V_t)

at this condition at the drain end, channel depth reduces nearly zero, at this point the channel is called pinched off. When we Increase V_{ds}further more than this value, it has very tiny consequence on the channel outline, and also the current through the channel remains constant at that value got for V_{ds}= V_{gs} -V_t. Thus, the MOSFET is arrived in the saturation region of operation and the drain current saturates at this value, and. The voltage V_{ds} at which saturation occurs is denoted V_{dsat}

V_{dsat}= V_{gs} -V_t

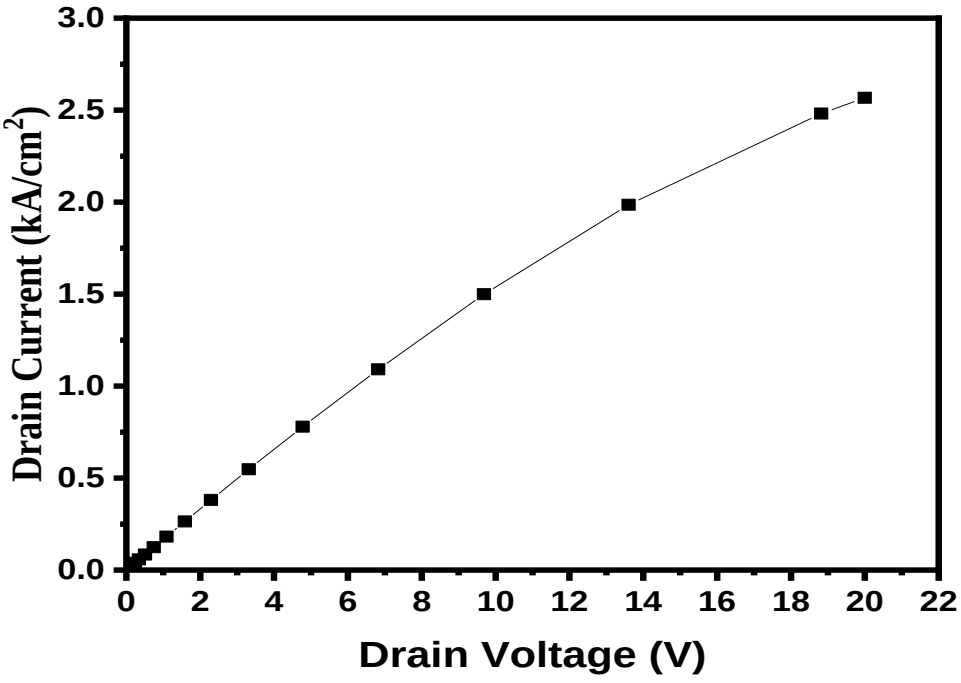

Fig:4.1 Graph of Drain current vs Drain voltage of modified UMOS

Same mechanism is happening for the above graph of I_d vs V_d.

Here I have fixed the gate voltage (V_g) at 10 V and vary the drain voltage up to 20V. As V_t is 6.5v[from fig19] so gate voltage is greater than threshold voltage. As a result, when we apply drain voltage, the drain current will flow through the device. As we increase the drain voltage the drain current will also increasing. From the graph I have got the drain current (I_d) is 2.567kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = (V_1-V_2)/ (I_1-I_2)

= (1.58-1.08) V/ (0.264-0.1.82) kA/cm^2

=6.0mΩ.cm^2

4.2 DRAIN CURRENT VS GATE VOLTAGE GRAPH OF MODIFIED UMOSFET

When we apply a positive gate to source voltage (V_{gs}) between gate and source terminal of the device at a fixed drain to source voltage (V_{ds}) The voltage V_{ds} is the reason for which a current is flowing through the induced n channel. For V_{gs} = V_t (threshold voltage) [5], the channel is just induced and the current conducted is still insignificantly small. As gate voltage exceeds threshold voltage, more electrons are attracted into the channel. With increasing V_{gs} current I_d also started increasing. When we increasing V_{gs} at a time electrical field along with the channel reaches a critical value the velocity of carriers inclines to saturate due to phonon scattering and the mobility also degrades, for this reason, when we increase the V_{gs} more, current (I_d) saturates at this value and will not increase further. Same mechanism is happening for the bellow graph of I_d vs V_g. Here I have fixed the drain voltage at 10 V and vary the gate voltage up to 20V.From the graph I have got the drain current (I_d) is 1.457kA/cm^2, and threshold voltage is 6.52304 V Here we can see that threshold voltage is 6.5V. When the gate voltage exceeds the value of threshold voltage means after 6.5 V the drain current started increasing. With increasing V_{gs} current I_d also started increasing. But after some time when V_{gs} is almost 10V the current got saturated because of velocity saturation the mobility degrades.

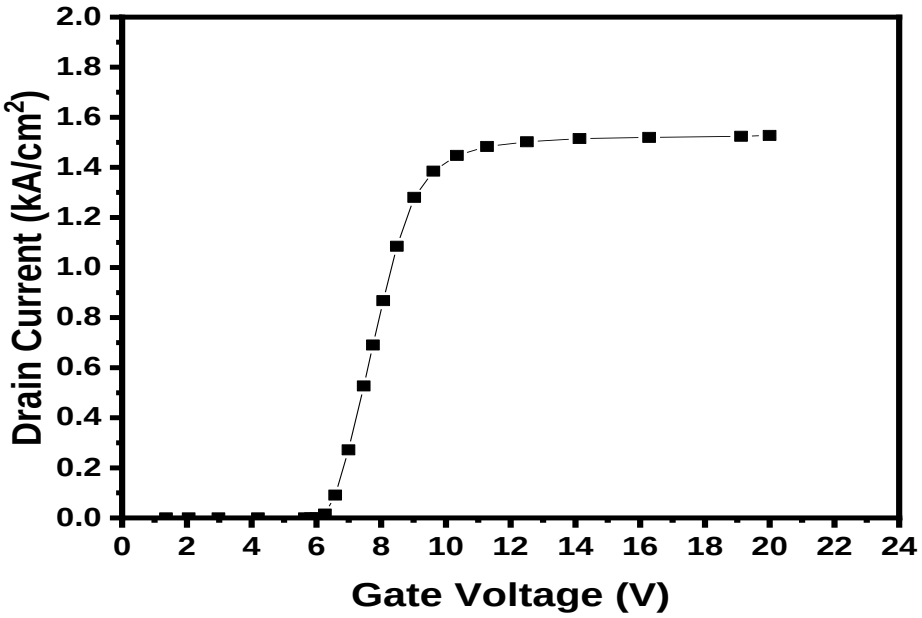

Fig:4.2 Graph of Drain current vs Gate to source voltage of modified UMOS

4.3 COMPARISION OF DRAIN CURRENT VS DRAIN VOLTAGE GRAPH IN BETWEEN CONVENTIONAL UMOSFET AND IMPROVED UMOSFET STRUCTURE

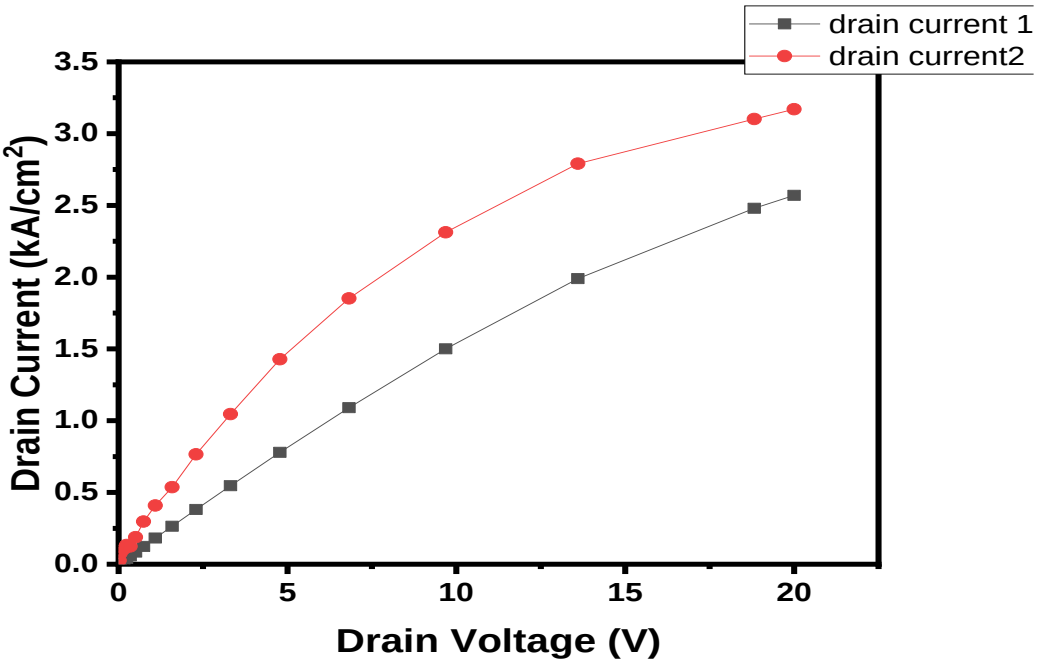

Fig:4.3 Comparison of Drain current vs Drain voltage graph of conventional UMOS (drain current2) and modified UMOS (drain current 1).

For modified UMOS Here I have fixed the gate voltage (V_g) at 10 V and vary the drain voltage up to 20V.From the graph I have got the drain current (I_d) is 2.65kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = (V_1-V_2)/ (I_1-I_2)

= (1.58-1.08) V/ (0.264-0.182) kA/cm^2

=6.0 mΩ.cm^2

For conventional UMOS [1,2], fixed the gate voltage (Vg) is 10 V and the drain voltage varied up to 20V.From the graph, the drain current (I_d) is 3.11kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = (V_1-V_2)/ (I_1-I_2)

= (1.58-1.08) V / (0.536-0.409) kA/cm^2

=3.94mΩ.cm^2

4.4 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH FOR IMPROVED UMOSFET STRUCTURE WITH VARYING TRENCH DEPTH

4.4.1 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH FOR IMPROVED UMOSFET STRUCTURE WHEN TRENCH DEPTH IS 0.1µm.

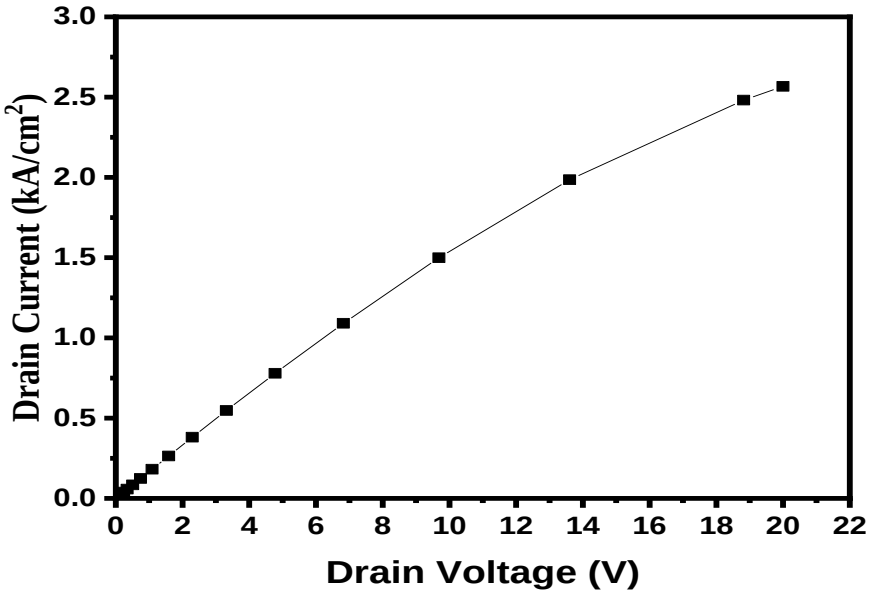

Fig:4.4 Graph of Drain current vs Drain voltage of modified UMOS when trench depth is 0.1µm.

Here gate voltage is fixed at 10V. Drain voltage is varied from 0 to 20V. The trench depth is 0.1µm, from the graph I have got the drain current (I_d) is 2.567kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = (V_1-V_2)/ (I_1-I_2)

= (1.58-1.08) V/ (0.264-0.1.82) kA/cm^2

=6.0mΩ.cm^2

4.4.2 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH FOR IMPROVED UMOSFET STRUCTURE WHEN TRENCH DEPTH IS 0.3µm.

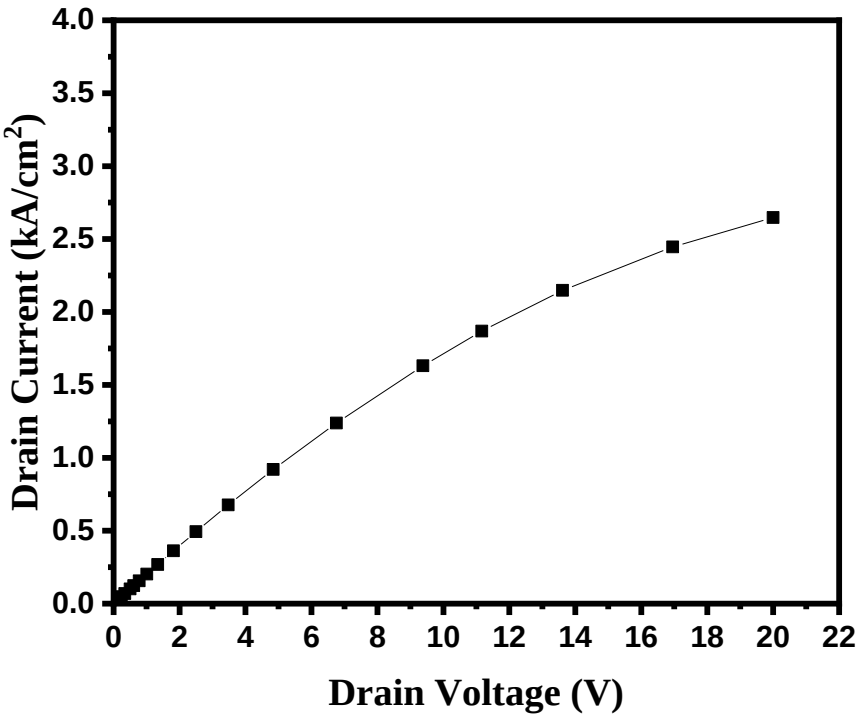

Fig:4.5 Graph of Drain current vs Drain voltage of modified UMOS when trench depth is 0.3µm.

Here gate voltage is fixed at 10V. Drain voltage is varied from 0 to 20V. The trench depth is 0.3µm, from the graph I have got the drain current (I_d) is 2.648kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = $(V_1\text{-}V_2)/ (I_1\text{-}I_2)$

= (1.33-1.00) V/ (0.268-0.202) kA/cm^2

=5.00mΩ.cm^2

4.4.3 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH FOR IMPROVED UMOSFET STRUCTURE WHEN TRENCH DEPTH IS 0.5µm.

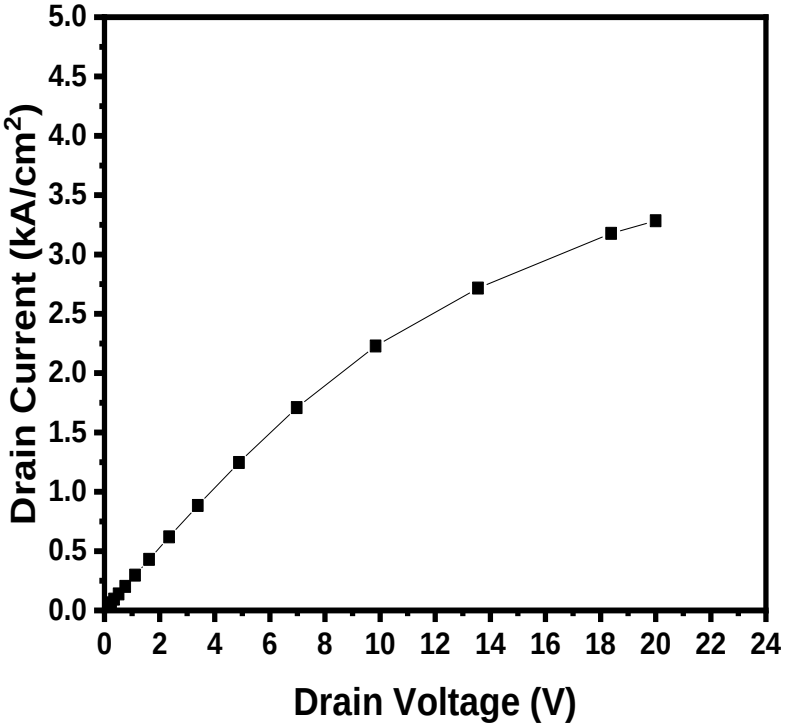

Fig:4.6 Graph of Drain current vs Drain voltage of modified UMOS when trench depth is 0.5µm.

Here gate voltage is fixed at 10V. Drain voltage is varied from 0 to 20V. The trench depth is 0.5µm. From the graph I have got the drain current (I_d) is 3.284kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = $(V_1\text{-}V_2)/ (I_1\text{-}I_2)$

= (1.61-1.11) V/ (0.431-0.297) kA/cm^2

=3.73mΩ.cm^2

4.4.4 DRAIN CURRENT VS DRAIN VOLTAGE GRAPH FOR IMPROVED UMOSFET STRUCTURE WHEN TRENCH DEPTH IS 0.8µm.

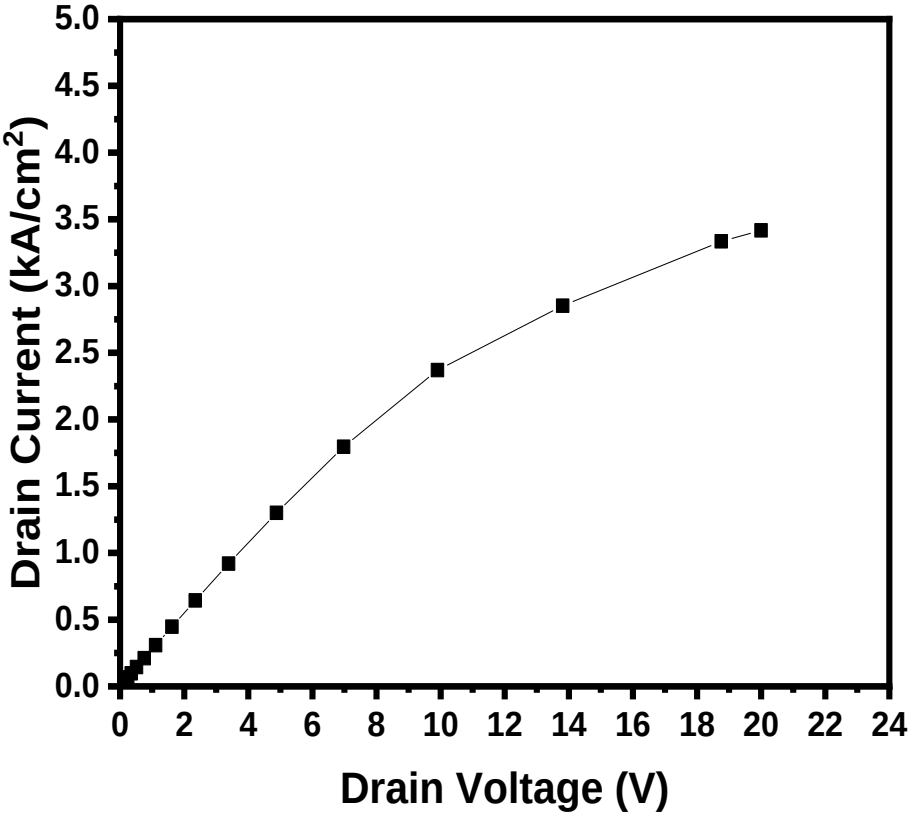

Fig:4.7 Graph of Drain current vs Drain voltage of modified UMOS when trench depth is 0.8µm.

Here gate voltage is fixed at 10V. Drain voltage is varied from 0 to 20V. The trench depth is 0.8µm. From the graph I have got the drain current (I_d) is 3.417kA/cm^2. After the calculation slope of the graph

I have got the ON- resistance (Ron) = (V_1-V_2)/ (I_1-I_2)

= (1.61-1.11) V/ (0.447-0.308) kA/cm^2

=3.59mΩ.cm^2

4.4.5 GRAPH OF VARIATION OF TRENCH DEPTH WITH ON-RESISTANCE

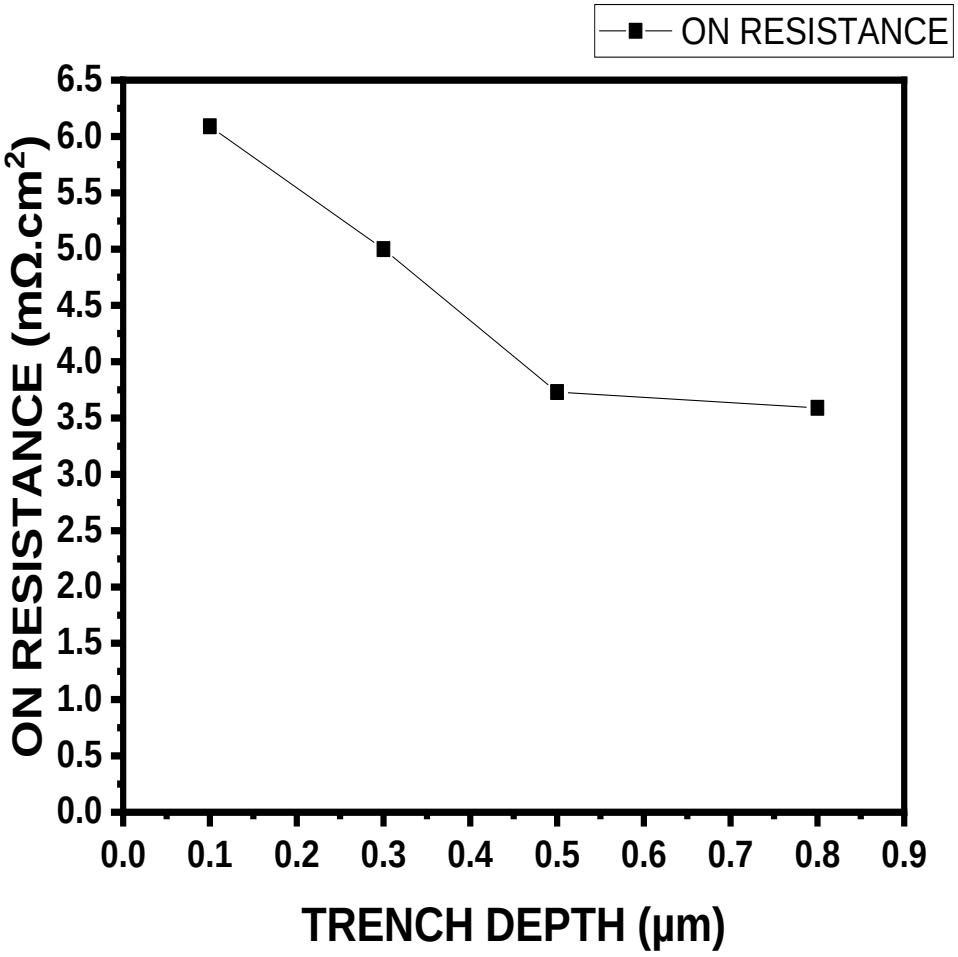

Fig: 4.8 Graph of varying trench depth vs ON-resistance

Here we can see that with different trench depth ON-resistance is changing. With the increasing value of trench depth, the ON-resistance values are decreasing. The values are shown in the table no 4.1. In the structure of improved UMOS, the n-type region has higher doping concentration [1-4] than that of the n-type drift region and for this reason it reduces the depletion region which is introduced by p^+shielding region. A reduced depletion region offers a wider space for the electrons and decreases the JFET resistance [1,2]. It improves the ON-resistance further.

TABLE NO: 4.1 Comparison of ON-resistance in different trench depth

TRENCH DEPTH (µm)	ON- RESISTANCE(mΩ.cm^2)
0.1	**6.09**
0.3	**5**
0.5	**3.73**
0.8	**3.59**

From the above graphs and results we can see that the conventional UMOSFET's ON-resistance is 3.94mΩ.cm^2.When we include n type region in the device the ON-resistance of the modified device is changing rapidly. Now when we increase the trench depth, the ON-resistance is decreasing. Like when depth is 0.1µm the ON- resistance is 6.0 mΩ.cm^2 but when we increase the trench depth like 0.3 µm,0.5 µm, and 0.8 µm, the ON- resistance also decreasing like 5 mΩ.cm^2,3.73 mΩ.cm^2,3.59 mΩ.cm^2.When we compare with conventional UMOSFET's ON-resistance with the modified UMOSFET's ON-resistance we can see that the ON-resistance of modified UMOS is lower than the conventional one with increasing trench depth.

CHAPTER 5: CONCLUSION AND FUTURE WORK

In this thesis development and working principle of UMOSFET are studied. The comparison study of I-V characteristics and ON-resistance of Conventional UMOSFET and Modified UMOSFET have been done here. In this thesis, SiC UMOSFET structure with an added n-type region at the bottom of the trench is studied. A n-type region is added in the drift layer for that reason depletion region is decreased as a result ON-resistance of the modified-UMOS is reduced. Here we have compared the ON-resistance of modified UMOSFET with varying the trench depth. With increasing the trench depth, the ON-resistance is decreasing gradually. Presenting a work opens more scope more future work. This is true in this case as well. Future work may include a new physical design or new material to improve the working of UMOSFET.

Reference

[1] X. Zhou, R. Yue, J. Zhang, G. Dai, J. Li, and Y. Wang, “4H-SiC trench MOSFET with floating/grounded junction barrier-controlled gate structure,” IEEE Trans. Electron Devices, vol. 64, no. 11, pp. 4568–4574, Nov. 2017. doi: 10.1109/TED.2017.2755721

[2] Kai Tian , Anders Hallén, Jinwei Qi , Shenhui Ma , Xinxing Fei, Anping Zhang , and Weihua Liu, “An Improved 4H-SiC Trench-Gate MOSFET With Low ON-Resistance and Switching Loss”, in *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2307-2313, May 2019, doi: 10.1109/TED.2019.2905636.

[3] I. A. Khan, J. A. Cooper, M. A. Capano, T. Isaacs-Smith and J. R. Williams, "High-voltage UMOSFETs in 4H SiC," Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics, 2002, pp. 157-160, doi: 10.1109/ISPSD.2002.1016195.

[4] Y. Li, J. A. J. Cooper and M. A. Capano, "High-voltage (3 kV) UMOSFETs in 4H-SiC," in IEEE Transactions on Electron Devices, vol. 49, no. 6, pp. 972-975, June 2002, doi: 10.1109/TED.2002.1003714.

[5] CMOS DIGITAL INTEGRATED CIRCUITS Analysis and Design by SUNG-MO (STEVE) KANG, University of Illinois at Urbana- Champaign, YUSUF LEBLEBIGI Worcester Polytechnic Institute Swiss Federal Institute of Technology-Lausanne, 5th edition,2005