Parametric Study of MOSFET

A comprehensive project report has been submitted in partial fulfilment of the requirements for the degree of

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in

VLSI Design and Microelectronics Technology

Thesis Submitted

by

DEBASIS MONDAL

Roll No: 001910703016

Examination Roll No.: M6VLS22015

Registration No.: 150143 of 2019-2020

Under The Esteemed Guidance

of

Prof. Manotosh Biswas

Department of Electronics & Tele-Communication Engineering

Jadavpur University, Kolkata-700032

West Bengal, India

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JADAVPUR UNIVERSITY

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_____.

Prof. Manotosh Biswas
Supervisor
Department of electronics and Telecommunication Engineering
Jadavpur University, Kolkata-700032

_____.

Prof. Manotosh Biswas
Head of the Department
Department of electronics and Telecommunication Engineering
Jadavpur University, Kolkata-700032
700032

_____.

Prof. Chandan Majumder
Dean
Faculty Council of Engineering and Technology(FET)
Jadavpur University, Kolkata-

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NAME: **DEBASIS MONDAL**

EXAMINATION ROLL NUMBER: **M6VLS22015**

DEPARTMENT: **ELECTRONICS AND TELE-COMMUNICATION ENGINERING (ETCE)**

THESIS TITLE: **PARAMETRIC STUDY OF MOSFET**

_____.
(Debasis Mondal)

Date: _____.

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NAME: **DEBASIS MONDAL**

EXAMINATION ROLL NUMBER: **M6VLS22015**

DEPARTMENT: **ELECTRONICS AND TELE-COMMUNICATION ENGINERING (ETCE)**

THESIS TITLE: **PARAMETRIC STUDY OF MOSFET**

NOMENCLATURE

V_{gs}- Gate to Source voltage

V_{ds}- Drain to Source voltage

V_{th}- Threshold voltage at room temperature

V_{fb}- Flat band voltage

J_{tn}- Direct gate tunneling in n-channel MOSFET current density

J_{sdn}- Source Drain Extension tunneling current density

J_{tpoly}-Leakage current density due to poly gate

J_{fn}- Fowler Nordheim Tunneling

E_{ox}- Dielectric constant of gate oxide

E_{ot}- Equivalent Oxide Thickness

C_{ox} - Oxide capacitance

μ - Mobility

L: Grid length (distance source-drain)

Z: Grid width

d: Oxide thickness

I_D: Drain current in linear region operation

I_{Dsat}: Drain current in saturation region operation

V_D: Drain voltage

V_{Dsat}: Drain voltage saturation

V_G : Grid voltage

V_T : Threshold voltage

e: Electron charge

W: Limit the space charge zone

N_a: Concentration of dopants in the channel

E : Electric field

E_c: Critical electric field (measured experimentally parameter Ec is about 5 × 104 v/cm)

T : The temperature of the network

T_0: The room temperature (300k)

K : Factor varying between (2.2 and 2.7)

I_R = body leakage current

I_{TH} = current due to threshold voltage change

I_{RDS}= current due to drain and source contact resistance

V_{OTH} = threshold voltage at elevated temperature

R_{DS} = drain and source contact resistance at room temperature

R_{ODS} = drain and source contact resistance at elevated temperature

W = MOSFET channel width

L = MOSFET channel length

A = cross-sectional area

q = electron charge ln electron mobility

Cox = oxide capacitance

a = proportionality constant

b = multiplying factor

GREEK LETTERS

ε_{Si} : Silicon permittivity (ε_{Si} = 1.05 10-12F/cm)

ε_{ox} : Oxide permittivity (ε_{ox} = 3.4531 10-13F/cm pours la silice)

Φ_F: Fermi potential

μ_o: The electron mobility under low field

θ : Measured experimentally parameter (θ[V-1] = 1.5/d)

γ : An empirical coefficient in the range from 2 to 3 (mV/k)

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ABSTRACT

Telecommunications, data processing, physics and electronics, take a very important place in the events of research of the various laboratories. In the field of the ultra-high frequencies, the field-effect transistor MOSFET caused many studies and research to exploit its interesting and promising characteristics as well as possible. The objective of this contribution is devoted to study the static properties I-V of MOSFET. The study enables us to calculate the drain current as function of bias in both linear and saturated modes; this effect is evaluated using a numerical simulation program, one could notice that the MOS transistor characteristics are very sensitive to the temperature. The load of inversion via the threshold voltage and the mobility of the carriers are the two principal impacted parameters, it was noted that the increase in the temperature induces a drop of the threshold voltage like that of mobility, and an immediate consequence of this reduction is the diminution in the drain current. One can thus conclude that the temperature influences the performances of the device; more it is low, better is the reliability of the device under operation.

It is well known that the device performance and characteristics are influence by change in operating temperature. Proper description of temperature effects in a device is essential for a circuit level MOSFET model to predict circuit behaviour over a wide range of temperature. To perform high temperature application, proper understanding of temperature reliant on parameter in MOSFET is critical. In a MOSFET model, there are many temperature dependent parameters such as bandgap, carrier mobility, threshold voltage, subthreshold leakage current, drain to source ON resistance, contact region resistance, saturation velocity etc. All of this parameters need to be modelled correctly. This paper deals with analysis of temperature effect on some of the MOSFET parameters like bandgap, carrier mobility, saturation velocity and contact region resistance. The analysis of all the effect are done by using mathematical simulation. The overall impact of these parameters on the characteristics of the MOSFET have been analysed.

Keywords: MOSFET, MATLAB/Simulink, COMSOL Multiphysics

CHAPTER 1

INTRODUCTION

Today, the thermal reliability is the critical issue faced by the semiconductor industry. So an essential role in performance and efficiency of the device is the temperature. Heat dissipation will occur within the device, when an IC is operational. This is called self-heating of the device, and this self-heating of the ICs device is burn in to a series of issue that affects the reliability of the device. It produces to large current, greater junction temperature and as a result in thermal runaway and ultimately rendering the device useless. A high end device should be productive efficiently and exhibits good performance for a high range of temperature. In order to optimize the performance of the device, the parameter that comes in the case of MOSFET scenario are bandgap optimization, subthreshold leakage issue, carrier mobility and saturation velocity, the resistance at contact and interface like source and drain. This work is focused on analysing the variation of each of these parameters with the variation in temperature. This effect of temperature on the device parameters, only if analysed and modelled, its effect on device staging can be known and consequently the better performing trustable device can be originated.

Big problem with BJT (bipolar junction transistor) was static power immoderation that is. power is reduced even if the circuit is not switching. BJT used on void tubes. BJT was a current controlled device, a silicon piece with three domain emitters, base, collector and after this MOSFET introduced which was a current controlled device. Basic MOS transistors used metal as the gate material, silicon di oxide as insulator and semiconductor as substrate, which titled the device as MOS i.e., Metal Oxide Semiconductor Transistor, whereas FET (field effect transistor) is named because of the fact that with an electric field crossing the gate that gate oxide therefor switches on and off by the transistor. MOS transistor is 4 terminal device that is. drain, gate, source, body. MOS transistors can be characterized in two structures n-MOS &p-MOS, both of them are complimentary in nature. Generally, poly-silicon consisting of heavy doping material of either n or p type can be used as gate material, silicon is used as insulator whereas source and drain are made by implanting donor contamination on both the sides. Allowing that two regions are biased at different potentials then the region at lower potential is source and the region at higher potential will act as drain. MOS transistors are no more ‘insulated gate’ devices, these insulated gates were used in IGFET or MOSFET. IGFET and MOSFET are voltage-controlled devices whose gate isolated from the body by a metal oxide layer. This layer makes the input resistance extremely high. Simultaneously gate is electrically isolated from the main current carrying channel avail between drain and source there is no flow of current in gate.

The MOS transistor is by far, the device the most encountered in the current production of semiconductor components, several acronyms are used in the literature to describe the metal oxide semiconductor (MOS) transistor: MOS field effect transistor (MOSFET), insulated gate field effect transistor (IGFET) and metal oxide semiconductor transistor (MOST). Silicon technologies field-effect MOSFET transistors are very mature and offer components with very honourable performances because of the intrinsic physical properties at relatively low

cost. This remains a major asset in the current context making it possible to fulfil the requirements of communication systems in terms of power.

The transistors are usually modulated by using the model of the same diagram. But this kind of models can only give one limited outline on the physical behaviour of the component, that is why the physical models based on analytical description intervene, in terms of transport properties, geometrical and technological parameters of the transistor.

When designing and implementing a circuit, the measurement of a MOSFET'S I-V characteristics become important. With a realistic SPICE model of the device, we can predict the risks of damage prior to application. Manufacturers provide datasheets of these devices with detail. However, the given data in datasheets is mostly on the extreme values rather than the average values. This is especially necessary when a MOSFET is desired to operate at 0-5 V gate voltage provided by microprocessors. For this reason, we need to measure the current voltage characteristics of these devices in detail.

MOSFET device parameters, such as threshold voltage (V_{th}), current on/off ratio ($I_{on/off}$) and sub-threshold swing, are usually inferred from the output and transfer characteristics. The drain current (I_{ds}) is plotted versus the drain voltage (V_{ds}) for various gate voltages (V_{gs})and is called the transfer characteristic. The drain current (I_{ds}) is plotted versus the V_{gs} for various V_{ds} and is called transfer characteristic.

Device characteristics are result by change in operating temperature. Proper description of temperature effects in a device is important for a circuit level MOSFET model to expect circuit behaviour over an inclusive range of temperature. To perform in high temperature application, proper understanding of temperature dependent parameter in MOSFET is critical. In a MOSFET model, there are many temperatures reliant on parameters such as bandgap, carrier mobility, threshold voltage, subthreshold leakage current, drain to source ON resistance, contact area resistance, saturation velocity like this. All of these restrictions need to be modelled correctly. This paper contracts with investigation of temperature result on some of the MOSFET parameters like bandgap, carrier mobility, saturation velocity and contact region resistance. The analysis of all the effect are done by using mathematical simulation. The complete effect of these parameters on the characteristics of the MOSFET have been examined. The general performance of electron mobility when plotted versus the effective field is physically studied. Due to charged cores in the silicon bulk, the oxide, and the interface, Coulomb scattering is revealed to be in charge for the deviation of mobility curves. Silicon major impurities have a double effect:

(a) Coulomb scattering due to the charge of these impurities themselves and
(b) reduction of screening caused by the loss of inversion charge when the depletion charge is increased.

The electric-field region in which mobility curves behave generally regardless of bulk-impurity concentration, substrate bias, or interface charge has been resolute for state-of-the-art MOSFET'S. Lastly, this study shows that electron mobility must be a function of the inversion and the depletion charges rather than a simple function of the electric field.

1.1 MOSFET

***M**etal **O**xide **S**ilicon **F**ield **E**ffect **T**ransistor* is shortened as MOSFET. It is just a unipolar transistor and used as an electronic switch and to amplify electronic signals. The device has three terminals containing of a source, gate and drain. Apart from these terminals there is a substrate generally called the body which is always linked to the source terminal for practical applications.

In recent years, its discovery has led to the leading usage of these devices in digital IC due to its structure. The Silicon di-oxide (SiO2) layer acts as an insulator and delivers electrical isolation among the gate and an active channel between the source and the drain which provides high input impedance which is almost endless thus capturing all the input signal.

The MOSFET fundamentals are discussed in detail in many types of reference books. The discussed here will focus on the relevant aspects for this work, which include scaling, and the minimization of parasitic source/drain resistance. In this Chapter the MOSFET fundamentals and main scaling issues of MOSFET'S are allow for in the next Section. To continue scaling, fully depleted (FD) MOSFETs are discussed Parasitic source/drain resistance is a big issue in FD MOSFETs, and SB MOSFETs are allowed for as a solution to this issue.

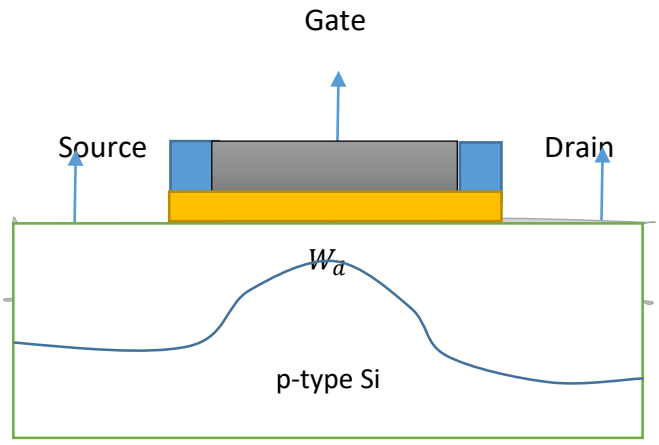


Figure: 1.1 : Short channel n-type MOSFET

This figure shows that Short channel n-type MOSFET, with applied drain bias, showing how the depletion regions in the source and drain affect the depletion region under the gate.

1.1.a. *MOSFET LAYOUT AND CROSS SECTION*

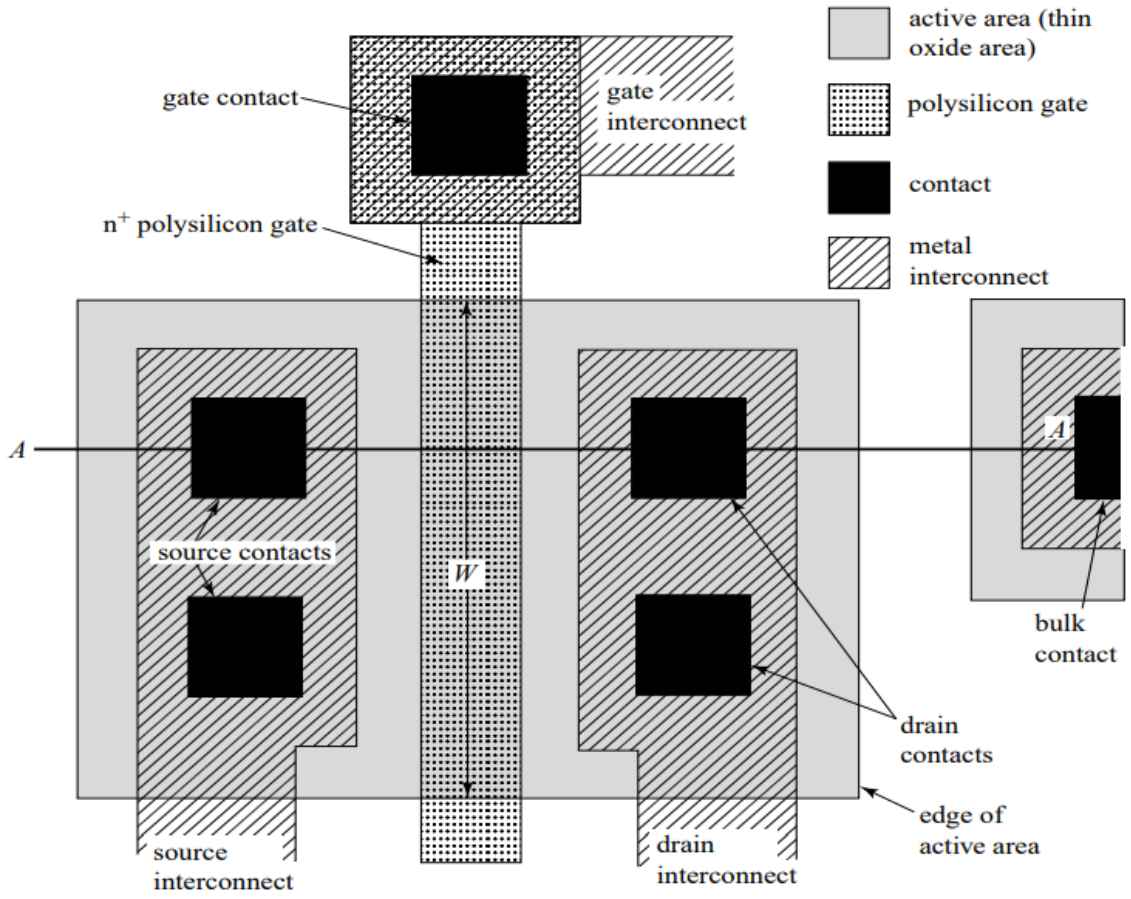


Figure: 1.2. This figure shows that the MOSFET layout

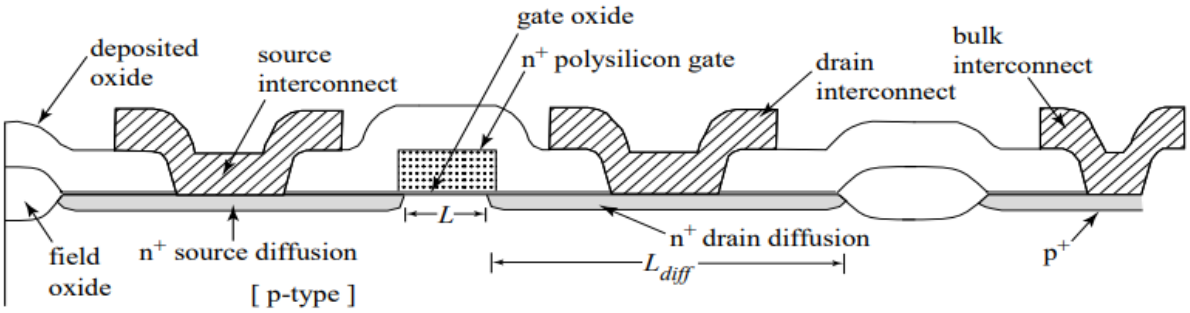


Figure: 1.3. This figure shows that the MOSFET cross sectional view.

1.1.B. CIRCUIT SYMBOL

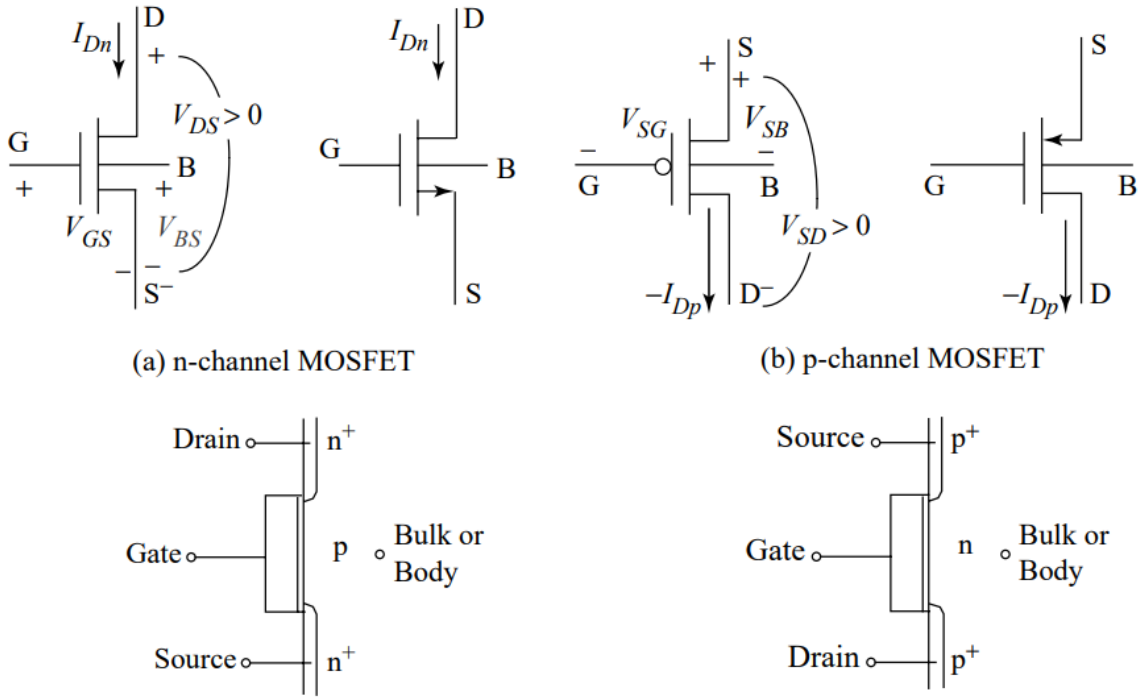


Fig: 1.4. (a). Symbol of the n-channel MOSFET, (b). symbol of the p-channel MOSFET

1.1.1 MOSFET FUNDAMENTALS AND SCALING

For the purposes of CMOS technology, the transistor should act a switch, with large current in the on state (I_{on}) And low current in the off state (I_{off}). Considering an nMOS device with the gate bias is equal to the circuit operation bias (V_g), The output curve ($I_d - V_d$) Is shown in fig 1.2. The curve has two parts, the linier and saturation regions. The characteristics in the linier region are given by ($I_s = 0$)

$$I_d = \frac{W}{L}\mu Cox\left((V_g - V_t)V_d - \frac{m^2 v^2 d}{2}\right) \quad \text{.....(1)}$$

where is the oxide capacitance per area (unit [F·Cm^{-2}]), and m=1+C_d/C_{ox} (C_d=$\mathcal{E}_{si}/W_{di}$) Is the body-effect coefficient. At extremely low V_d the device runs as a resistor, the gate bias attracts electrons to the interface, forming a conductive inversion layer at the interface. The factor arises since the inversion layer at the drain is smaller than at the source, since -Vs > -V_d. When V_d = (-V_t)/m the device reaches saturation, and the drain current is given by

$$I_{dsat} = \frac{W}{2Lm}\mu Cox(V_g - V_t)^2 \quad \text{.....(2)}$$

The current equations assume low field mobility, that is when the electric field in the transport direction is low. For devices with gate length less than a few hundred nm, the field

along the channel ($\mathcal{E}$) Is large, and the low field mobility approximation is no longer valid. At a certain lateral field, the carrier velocity saturates, and the drain current

$$I_{dsat} = WC_{ox}v_{sat}(V_g - V_t - \mathcal{E}_{sat}L) \quad \text{.....(3)}$$

Therefore, at short L the drain becomes less sensitive to decrease in L., in extremely scaled transistors, where the gate length is smaller than the mean free path between scattering events, the current is limited by its ballistic current:

$$I_{ball} = Q < v^+ \geq WC_{ox}(V_g - V_t) < v^+ > \quad \text{.....(4)}$$

where is the mean velocity of carriers going from source to drain. Monte Carlo simulations show scattering is relevant even in small transistors, but the ballistic current is nevertheless a useful upper limit to current transport in nanoscale devices. If the drain of the MOSFET has applied bias V_{dd} and the gate bias is increased from 0 to V_{dd} the MOSFET first passes through the subthreshold region and at the threshold voltage V_t it passes to the saturation region. The subthreshold current may be written as

$$I_d = I_o e^{\frac{q(V_g - V_t)}{mkt}} \quad \text{.....(5)}$$

Where I_0 is the current at V_g=V_t.

Optimum MOSFET performance requires balance between minimizing I_{off} and maximizing Ion. A decrease in Vt causes logarithmic increase in I_{off} and linier increase in Ion. Device optimization may also decrease m, thus achieving a steeper subthreshold slope. Also, much work has been done to increase the channel mobility. A large performance enhancement is achieved by device scaling

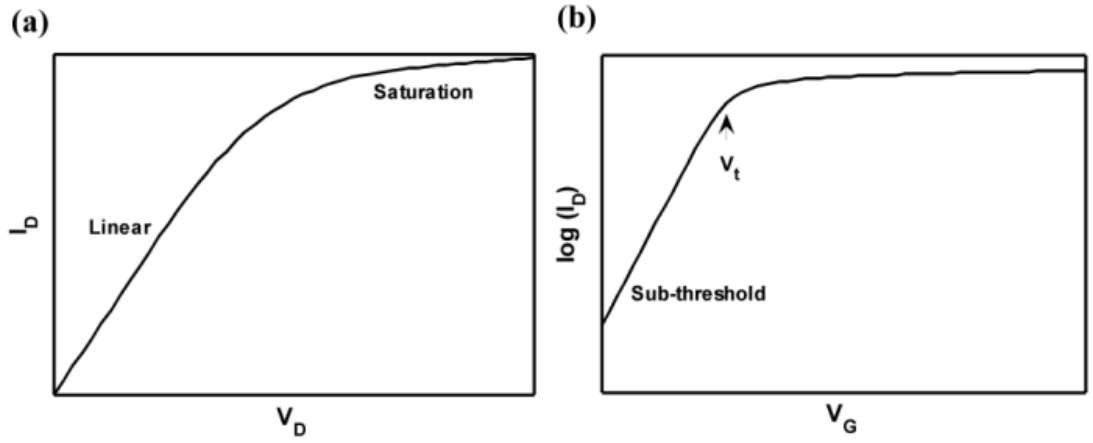


Figure: ***1.5: (a) I_d -V_d and (b) $I_d - V_g$ curves for a n-type MOSFET.***

$$\psi_s(x) \approx \psi_l - \psi_l e^{\frac{x}{\Lambda}} + (V_d - \psi_l)e^{\frac{x-l}{\Lambda}} \quad \text{.....(6)}$$

where the characteristic length Λ is the length the source and drain electric fields penetrate the channel

$$\Lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ax}}} W_{eff} t_{ax} \quad \text{.....(7)}$$

were W_{eff} is the effective depletion width. In long channel case W_{eff}=W_d but considering the S/D region affects the depletion width in a short channel MOSFET, the W_{eff} is larger than Wd in short channel devices.

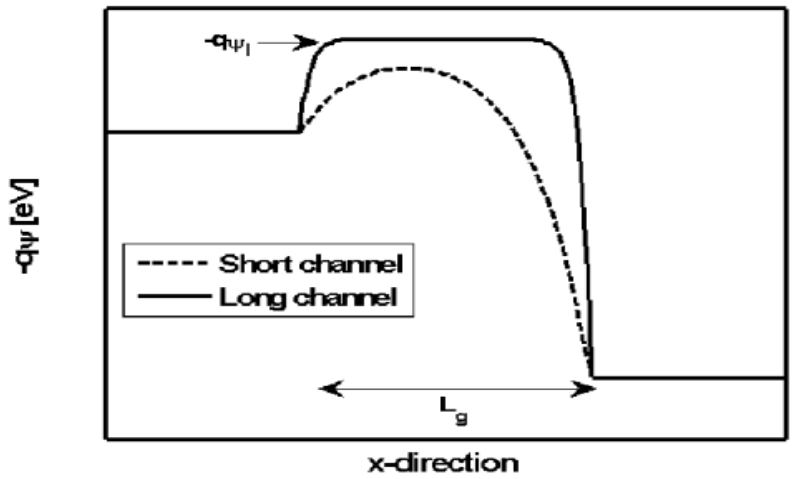


Figure:1.6. Energy band structure

This figure indicates the *Energy band structure with biased close to threshold voltage, for a short and long channel MOSFET. Field penetration from source and drain causes Vt lowering, which is further enhanced as drain bias is increased.* It illustrates some essential characteristics of scaling. If L ≫ Λ the device will exhibit long channel behavior. When L is decreased, eventually the threshold voltage becomes dependent on L since the source and drain will decrease the barrier. For scaling one needs L/Λ = 5-10 depending on the application. When L is smaller than 5-10·Λ a V_t roll-off effect is observed which follows the relationship

$$V_{t-long} - V_t = \Delta V_t \propto e^{-\frac{L}{2\Lambda}} \quad \text{.....(8)}$$

Some V_t roll-off may be acceptable, but there is a serious variability issue when L is small, since a slight change in the gate length will cause momentous changes in threshold voltage and, therefore. assumes low V_d, in the short channel case as V_d is increased the drain field further pulls down the barrier. This drain induced barrier lowering (DIBL) can be included in the threshold voltage,

$$\Delta V_t = 2\sqrt{V_{bi}}(V_d + V_{bi}).e^{-\frac{L}{2\Lambda}} \quad \text{.....(9)}$$

The built-in voltage is the threshold voltage between the gate and S/D regions. To scale L, Λ must be scaled also, thus,$W_{eff}$and t_{ox}/ε_{ox} should be decreased. Scaling of tox has been the subject of extensive research. In short, the tox scaling is fundamentally limited by tunneling leakage currents through the oxide. This has caused the industry to increase ϵox by implementation of high-k oxides and metal gates. The W_{eff} scaling is performed by

decreasing the depletion width Wd and by introducing shallow for junction depths X_j . However, decreasing Wd requires higher bulk doping, causing reduced mobility, and increasing, hot electron degradation and avalanche breakdown. To bypass this problem, so called halo implants have been used to implant a higher concentration of dopants close to the source/drain regions. As X_j is decreased, the doping concentration in the S/D regions has to be increased, to keep the parasitic source/drain resistance within limits. However, as scaling continues the concentration reaches a solid solubility limit which sets a minimum to the Si resistivity. Alternate doping techniques such as plasma doping, gas phase doping, and cluster implantation combined with ultra-rapid annealing methods like pulsed laser annealing, may allow for further reduction of the junction depth. Despite these techniques to continue scaling, the scaling of gate length in bulk MOSFETS is reaching fundamental limitations. The increase of mobility by strain engineering has contributed to further performance enhancement, since the increased-ON currents have allowed for downscaling of device width further decreasing the device footprint. These issues with scaling have led to the introduction of fully depleted (FD) structures, which will be discussed next.

1.1.2 Fully depleted MOSFETs

Fully depleted (FD) MOSFETs have been studied extensively in recent years to enable continued scaling. For this purpose, the MOSFET is usually fabricated on a thin Silicon-On Insulator (SOI) film with low doping so that the whole film is depleted. Several versions of these devices have been proposed depending on how many sides a gate is placed at namely: ultra-thin-body (UTB), double-gate (DG), tri-gate, and gate-all-around. The characteristic length Λ of these devices is decreased with an increasing number of gates. A device with n gates has Λ n=Λ/√n. For the UTB device, smaller Vt roll-off effect has been demonstrated, when compared to bulk technology. However, the drain field still has a strong capacitive coupling through the buried oxide (BOX) to the channel, and the scaling length (Λ) theory is wrong. Simulation study has shown in the ratio between t_{si} and L should be L/t_{si}> 5 to keep the SCE within limits. However, when t_{si} < 3 nm the electron Si mobility is severely reduced, due to increased surface optical phonon scattering and t_{si} thickness fluctuations. The UTB technology may be used for near term technology generations, but eventually t_{si}< 3 nm would be needed to sustain scaling. An improvement to the UTB structure is the use of a thin BOX and a bottom grounded plane. The SCE is improved when the drain field terminates in the bottom ground plane. The use of thin body has been criticized since it leads to larger transverse fields and therefore reduced mobility. A significant improvement to the UTB device is the double-gate MOSFET. This is because the bottom gate screens the drain field, which allow for relaxed t_{si} requirements. A first order approximation from simulation results have given L > 2t_{si} is required to maintain reasonable DIBL and SS. Using the planar fabrication process, there is significant difficulties in placing the second gate underneath the channel. Instead, the Fin FET has been proposed, where a thin vertical body is etched on a SOI

substrate, and the etched sidewalls are used as the channel. Further extensions of the Fin FET approach are tri-gate MOSFETs, which adds a gate on top of the fin (L > 1.5t_{si}. Scaling may lead to a nanowire gate-all around (GAA) device which will allow for L >t_{si}. The GAA device is difficult to fabricate, since at some point in the process the Si nanowire must be suspended to place the gate under the transistor. A practical compromise is the Ω FET in which the oxide under the gate is etched partially, so that the gate covers most of the Si nanowire.

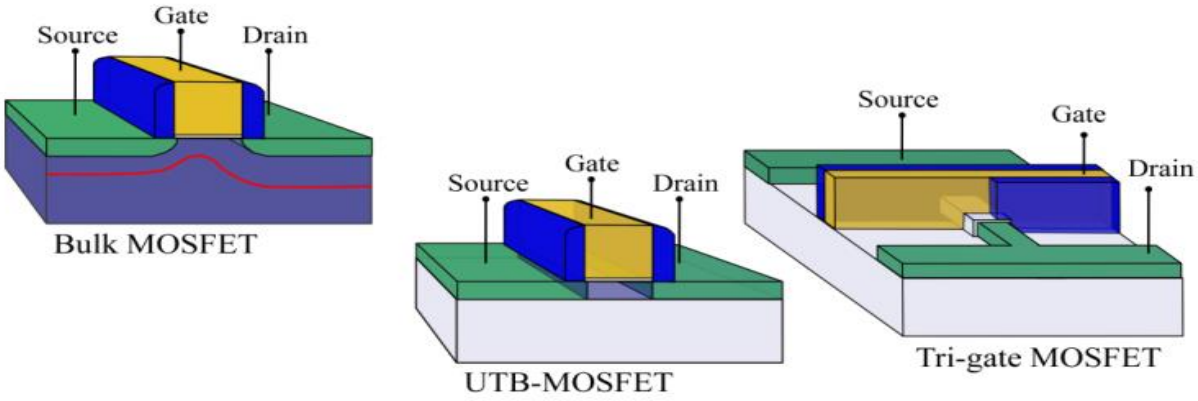


Fig:1.7 MOSFET Schematics: (a) bulk, (b) ultra-thin-body, (c) tri-gate

An important concern for the implementation of thin body FD structures is the control of parasitic series source/drain resistance RSD. Just like scaling of X_j in the bulk MOSFET, the scaling of t_{si} requires an increase in S/D doping concentration. In Si-nanowires (Si-NW) deactivation of dopants can also be a fundamental problem, which would further increase RSD. In a 50% deactivation was reported for a nanowire with a 15 nm diameter. The deactivation was explained by an increase in ionization energy of dopants due to confinement in the Si-NW. Also, self-aligned solicitation is challenging for thin body devices. To solve these issues, the elevated S/D approach is commonly used, where selective epitaxial growth of highly doped Si in the S/D region is used to increase the thickness of the S/D regions. The resistance components are shown in where the RSD is composed of the extension from the epi to the channel R_{ext}, the spreading resistance under the contact (R_{sp}), and the contact resistance (R_{sb}). The thickness of the sidewall spacer needs to be optimized to obtain a balance between minimizing R_{ext} and the fringing capacitance [67]. The focus of this work has been on the reduction of R_{SD} by an alternative approach where the metal is placed at the channel edges, forming a Schottky barrier MOSFET. This structure is introduced in the next Section.

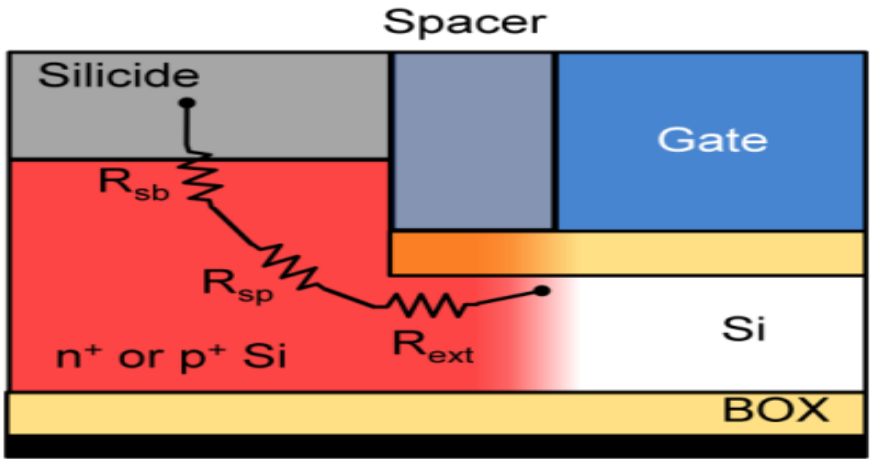


Figure: 1.8. Parasitic resistance components of a FD MOSFET with raised S/D

1.1.3 Schottky barrier MOSFET

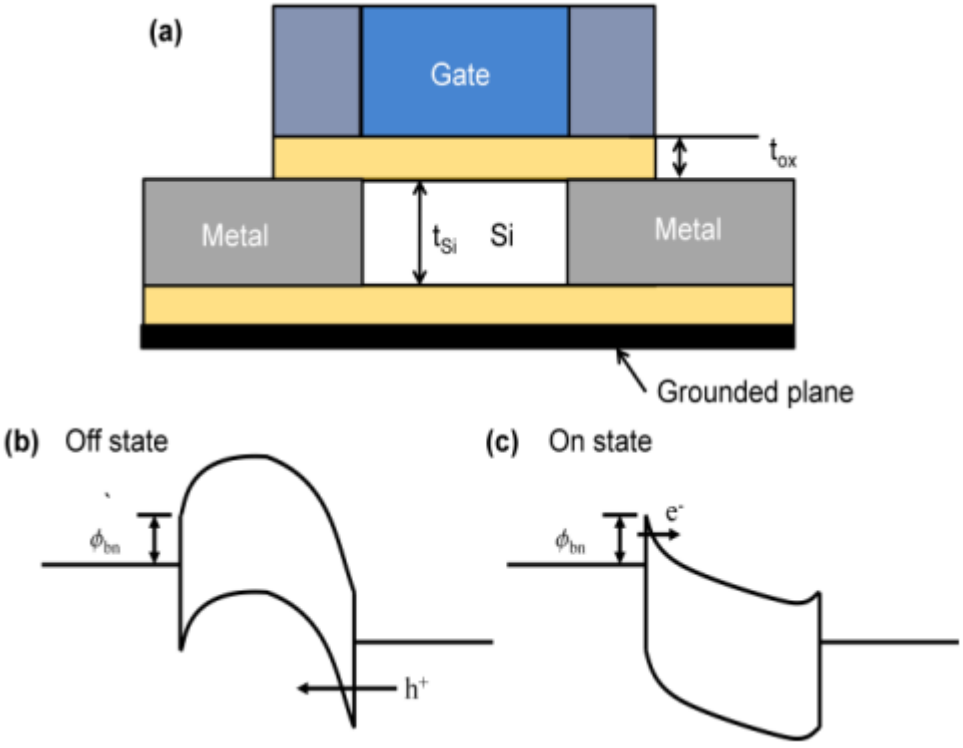


Figure: 1.9. (a) Schematic of the Schottky barrier MOSFET and band diagram for n-MOS device in (b) off state ($V_g = 0$) and (c) on state ($V_g = V_{dd}$).

A schematic and band diagram of the SB- MOSFET is. The device shown is a UTB MOSFET with a thin BOX and grounded bottom plane. The thin BOX would decrease short channel effects but is shown just to be consistent with the analytical model discussed in the next

Section. Devices with doped extensions will be discussed in Section Fundamentals of SB-MOSFETs

n-type SB- MOSFET in the off-state. In the ON regime of the SB- MOSFET (V_d = V_{dd}) The reverse biased Schottky junction at the source end is the largest contributor to the parasitic R_{SD} in the SB- MOSFET. In Schottky diodes the tunneling through the barrier is affected by the doping concentration and bias across the diode. However, in the SB- MOSFET the electric field from the gate controls the potential profile in the channel, and therefore the tunneling. To analyze the basic behavior of SB- MOSFET in the ON regime a modified version of a simple model proposed will be used that has the essential elements needed for the discussion but is not accurate enough for a quantitative study. The current transport through a reverse biased Schottky contact at the source is:

$$I_{sb} = I_{b0} e^{-\frac{q\phi_b'}{kT}} \quad \text{.....(10)}$$

where I_{b0} is given by

$$I_{b0} = W A_{2D} T^{\frac{3}{2}} \quad \text{.....(11)}$$

$$I_{2D} = \frac{q\sqrt{2m_{Rich}(k_B\pi)^{\frac{3}{2}}}}{h^2} \quad \text{.....(12)}$$

where is the 2D effective Richardson constant. the 2D is used here current transport is direct between the metal and the 2D channel. In this simple model only one sub band is accounted for. effective barrier height that considers barrier lowering by tunnelling ($\Delta\phi_t$) And image force barrier lowering ($\Delta\phi_{ifbl}$):

$$\phi_b' = \phi_b - \Delta\phi_t - \Delta\phi_{ifbl} \quad \text{.....(13)}$$

$$\Delta\phi_t = \frac{1}{q}\left(\frac{3qh\ln(2)}{4\sqrt{2m}}\right)^{\frac{2}{3}} \mathcal{E}^{\frac{2}{3}} \quad \text{.....(14)}$$

$$\Delta\phi_{ifbl} = \left(\frac{q}{4\pi\mathcal{E}_{si}}\right)^{\frac{1}{2}} \mathcal{E}^{\frac{1}{2}} \quad \text{.....(15)}$$

The equation uses the WKB approximation and assumes a triangular barrier. Therefore, the results obtained by this simple model are only approximate. Using this simple model, the transport across a Schottky barrier can be obtained if the SBH and the electric field at the interface are known. Assumes non-degenerate transport, however, in nanoscale transistors, the transport is degenerate. To estimate the electric field at the source is used as a starting point. Taking the derivative, the electric field close to the source is: The potential between source and channel is estimated by setting, where is the gate bias at which there is flat band condition at the source. Next, taking the field at the Schottky contact (x = 0) we have:

$$|\mathcal{E}| = \frac{\eta(V_g - V_{fb})}{\Lambda} \quad \text{.....(16)}$$

where η has been added as a geometric factor that is affected by the underlap/overlap between the gate and the metal S/D contact, and the variation in along the height of the Schottky contact. If the resistance of the SB contact is much larger than that of the intrinsic MOSFET, the current characteristics are dominated by the contact and the current of the SB-MOSFET is given by. According to the ITRS the parasitic series resistance should not degrade Ion by more than 33%. Therefore, for the SB- MOSFET technology to be viable, the contact resistance must be decreased sufficiently to fulfil that criterion. The current of an ideal ballistic MOSFET is given by and is several mA/µm. To analyse if SB- MOSFET technology is viable it is possible to analyse which ϕ_b and are needed so that current drive is not limited by the Schottky contact or I_{sb}>

I_{sb}-V_g for the source Schottky contact of a SB- MOSFET with tox = 1 nm, t_{si}= 8 nm, ϵox=3.9, and η = 1. When V_g< V_{fb} an ideal 60 mV/dec slope is assumed. In a SB- MOSFET where current is dominated by the source Schottky contact, the device exhibits a classical thermionic subthreshold slope until a flat band condition is reached between the channel and source (= V_{fb}). At > V_{fb} the increasing enhances the electric field at the source contact and increases tunnelling, therefore, subthreshold slope is obtained with a slope much larger than the ideal 60 mV/dec. Taking the plot shows that ϕ_b ≈ 0.2 eV has similar current as the ballistic current limit, which indicates that is the maximum allow for barrier height for implementation in CMOS technology.

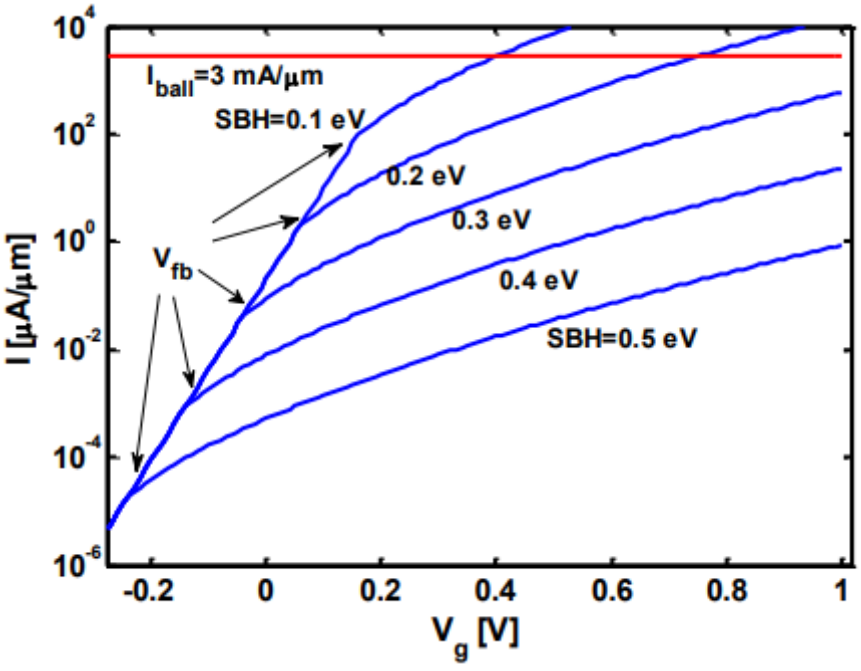


Figure:1.10. I_{sb}-Vg representing the source Schottky contact of a SB- MOSFET with tox=1 nm and tSi=8 nm.

This figure shown that the estimated ballistic current of an ideal MOSFET of the source *Schottky contact of a SB- MOSFET with tox=1 nm and tSi=8 nm*. In a SB- MOSFET with ϕ_b = 0.3 eV and t_{si}= 8 nm is shown, with tox = 0.5 nm, 1 nm, and 4 nm. As t_{si} is decreased the electric

field at the contact increases and the current drive is enhanced. Therefore, as MOSFET technology is scaled down, the increased electric field at the source enhances the performance of SB- MOSFET. The device would reach the ballistic limit with extremely thin equivalent oxide thickness (EOT) of 0.5 nm where the field at the contact was $\mathcal{E}$ = 4.5 MV/cm. This field is on the same order of magnitude as the breakdown field of oxides. For instance, the breakdown field of SiO_2 is approximately 10 MV/cm and 4 MV/cm for HfO_2. Therefore, there is a limit to how much the gate

induced field can enhance tunnelling in SB- MOSFET. Careful simulations have shown = 0.1-0.15 eV been the maximum allow for implementation in CMOS technology.

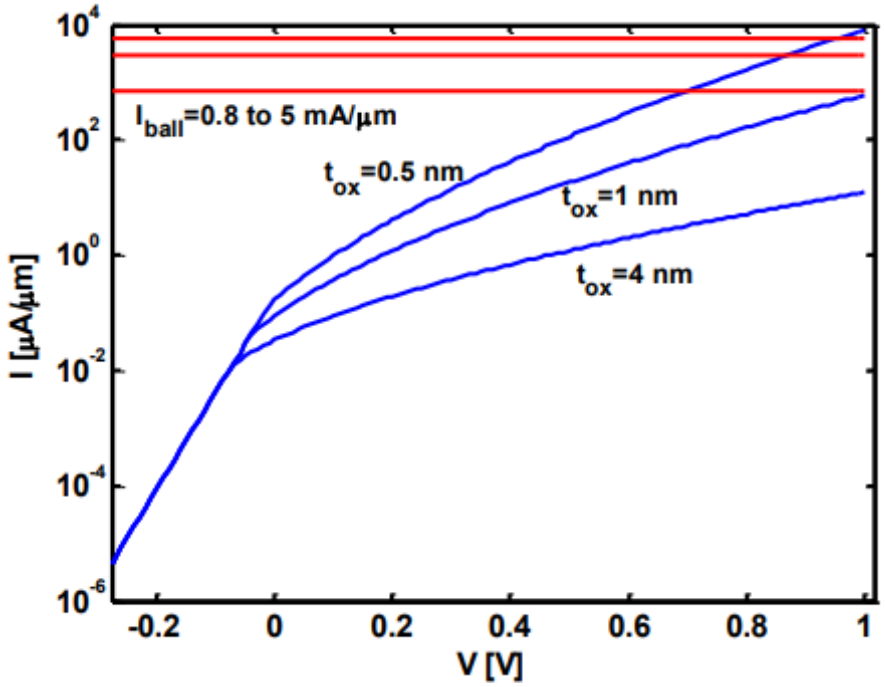


Figure: 1.11. I_{sb}-V_g representing the source Schottky contact of a SB- MOSFET with Φ_b = 0.3 eV and t_{si}= 8 nm.

This figure shown that the estimated ballistic current of an ideal MOSFET, which increase with decreasing t_{ox}.

1.1.4 SB-MOSFETs with doped extensions

To minimize the effective barrier height, a shallow for layer of dopants can be placed in front of the SB contact. The dopants enhance the electric field at the interface and therefore the current. To clarify the discussion, it is useful to define two ranges of devices with doped extensions, the fully depleted contact, and partially depleted contact. That is, the SB contact has depletion length:

$$W_s \approx \sqrt{\frac{2\varepsilon_{si}}{qN_{ext}}\left(\psi_{bi-V-\frac{kT}{q}}\right)} \quad \text{.....(17)}$$

Where Next is the doping concentration of the extension. If the doped extension has a length (Lext), when L_{ext}< W the extension doping is fully depleted and when L> W_s it is partially depleted. The reason it is important to distinguish between the two cases is that in the fully depleted case, the electric field at the Schottky contact is affected by the field from the gate. However, in the partially depleted case the effect of the field from the gate is decreased since the gate field is screened by the mobile carriers in the non-depleted portion of the extension.

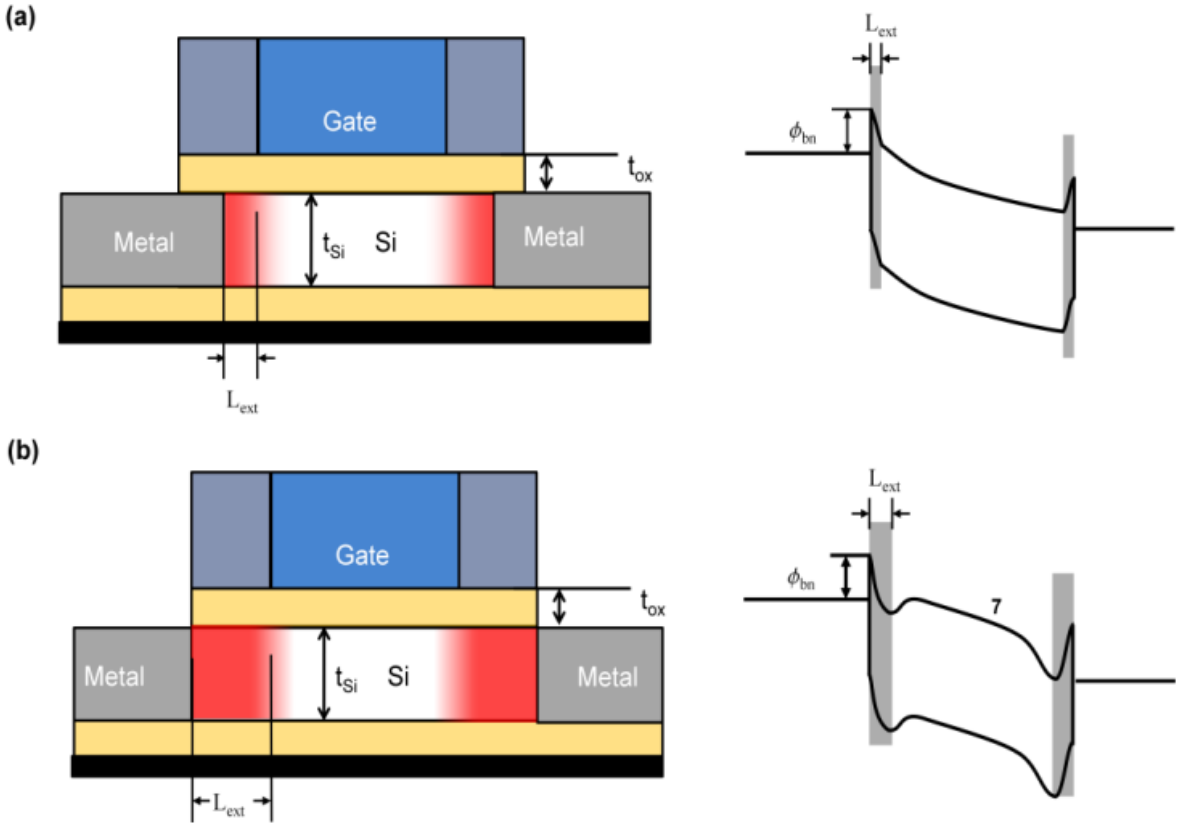


Figure:1.12. (a) SB-* MOSFET *with a shallow fully depleted extension. (b)* MOSFET *with a thicker partially depleted doped extension, which essentially functions as a doped-S/D device connected to small highly doped M-S contacts.

To evaluate the W_s , it is necessary to know the potential drop across the contact V, which would require numerical simulations. Since the ND is large enough to be degenerate, then ψ_{bi} ψ_b and V is small, we can write

$$W_s \approx \sqrt{\frac{2\varepsilon_{si}}{qN_{ext}}\phi b} \quad \text{.....(18)}$$

Given a certain doping concentration Next, when L_{ext} is small, the electric field of the contact increases as L_{ext} is increased, when L_{ext} > W_s the becomes independent of Lext and becomes an ohmic contact with contact resistivity (ρ_c) That depends only on Next and ϕ_b. In these

devices one can consider a Schottky contact resistance (R_{sb}) And extension resistance (R_{ext}). To maximize the electric field at the interface Lext > W_s is needed but having Lext longer than that will only increase R_{ext}needlessly. In this case the R_{sb}= ρ_c /t_{si}[Ωμm] and R_{ext}= ρsLext/t_{si}[Ωμm]. To estimate the resistances involved in $R_{sb}$and R_{ext}a simple example will be shown. Assume ϕ_bn = 0.67 eV (barrier height of NiSi to ntype Si) and Next = 1020 cm (about 33.46 ft)-3. Then ρc = 3·10-8 Ωcm 2 and ρs = 10-3 Ωcm. Assuming t_{si}= 10 nm and Lext = 15 nm, we get R_{sb}= 300 Ωμm and Rext = 15 Ωμm. Thus, the extension length is not of primary importance, except that in real devices the junction surprisingly must be allow for. Therefore, minimizing R_{sb} is the primary concern. As discussed above, the elevated S/D solution has been used to increase the contact area, but that adds complexity to the process. However, if it is possible to increase Next towards 1021 cm (about 33.5 ft)-3, the R_{sb} would be decreased sufficiently for implementation in CMOS technology. A promising method to introduce enough dopants at the interface to obtain low contact resistance is the use of dopant segregation.

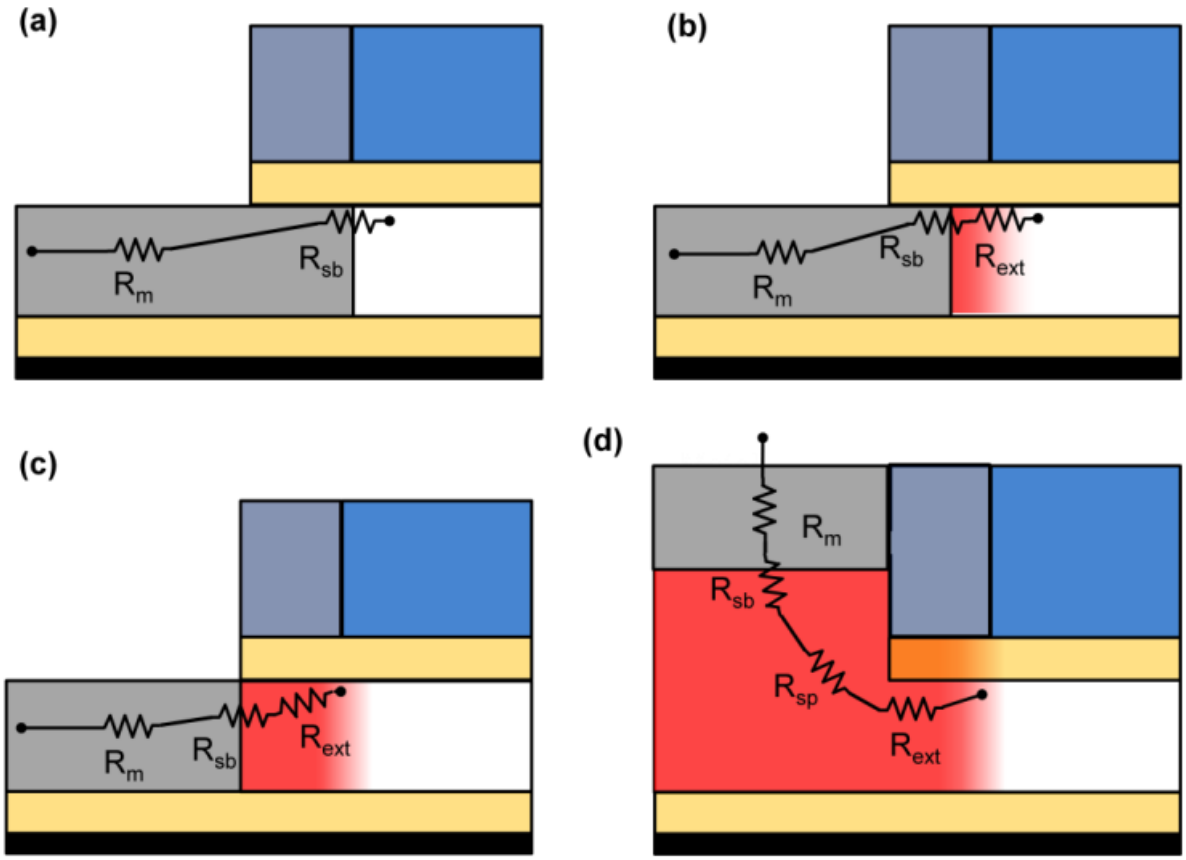


***Figure:1.13. Resistance components of (a) SB-* MOSFET *(b) SB-* MOSFET *with fully depleted extension (c) SB-* MOSFET *with partially depleted extension, and (d) elevated S/D* MOSFET**

1.1.5Area of Safe Operation

The safe operating are of MOSFET's is temperature dependent. The safe operating area is at 25^0C.

The safe operating area is the voltage and current conditions over which a MOSFET's operated without permanent damage or degradation. The MOSFET must not be susceptible to conditions outside the safe operating area for an instant. The safe operating area of a MOSFET are bound only by the maximum drain source voltage, and drain current and a thermal limit between them.

The safe operating area of MOSFET's are divided into the following five regions:

1. Thermal limitation
   This area is bound by the maximum power dissipation. In this area power dissipation is constant.
2. Secondary breakdown limitation
   With the shrinking geometric devices, some MOSFET's have exhibited a failure mode like to secondary breakdown in recent years. This area is bounded by the secondary breakdown limit.
3. Current limitation
   This area defines the limited by the maximum drain current ratings. The safe operating area is bounded by maximum drain current for continuous DC current operation.
4. Drain-Source Voltage limitation
   This area defines an area bound by the drain-source voltage with gate shorted.
5. On-state resistance limitation
   This area defines that the theoretically limited by the maximum on-state resistance limit.

1.1.6 Applications of MOSFET

- MOSFET amplifiers are extensively used in radio frequency applications.
- It acts as a passive element like resistor, capacitor and inductor.
- DC motors can be regulated by power MOSFETs.
- High switching speed of MOSFETs make it an ideal choice in designing chopper circuits.
- More, etc.

1.1.7 Advantages of MOSFET

- MOSFETs provide greater efficiency while operating at lower voltages.
- Absence of gate current results in high input impedance producing high switching speed.
- They operate at lower power and draws no current.
- Its mature fabrication technology,

- Its high integration levels,
- Its mixed analog/digital compatibility,
- Its capability for low voltage operation,
- Its successful scaling characteristics,
- And the combination of complementary MOSFETs yielding low power CMOS circuits.
- More

1.1.8 Disadvantages of MOSFET

- The thin oxide layer makes the MOSFETs vulnerable to permanent damage when evoked by electrostatic charges.
- Overload voltages makes the device unstable.
- Thermal runaway occurs due to self-heating effect
- More

Chapter 2

MOTIVATION

2.1 Factors of Motivation

I carefully study the paper [Jitty Jose, 2Keerthi K Nair, 3Ajith Ravindran 1P.G Scholar, 2P.G Scholar, 3Assistant Professor " Analysis of Temperature Effect on MOSFET Parameter using MATLAB" Electronics and communication Engineering, Saintgits College of Engineering, Kottayam India, © 2016 IJEDR | Volume 3 and 4, Issue 3 | ISSN: 2321-9939]
According to the International Technology Roadmap for Semiconductors (ITRS) each lower node is 0.7 times the previous technology creation chip faster by 17% every year. CMOS technologies Scaling down to 22nm has significant in design. By reducing the sizes many challenges like gate leakage, short channel effect (SCE), low voltage operation & delay comes into picture.

Thus paper presents the past work done in design of nanoscale MOSFETs. Use of Silicon on Insulator (SOI) for the thin short channel, Lower parasitic capacitance, Resistance to Latch up & has 10-20% higher switching speed. This paper shows the several challenges in design of MOSFET & various methods or techniques for increasing the performance of MOSFET at lower node.

Since the invention of transistors, the electronic devices on a wide variety of automotive, military, aerospace and other industrial and commercial high temperature applications. MOSFET device scaling plays a great role in the rapid development of the semiconductor industry. The cost per device or per function have been greatly reduced, which is one of the major reason for the widespread adoption of electronics devices. When the number of transistors destroy increases the heat dissipation occurring within the chip increases. This effect is called self-heating effect. It improves to large current, greater junction temperature and can result in thermal runaway and therefore the device useless. There are a number of factors both inside and outside of the semiconductor that resist the high-temperature operation of semiconductor electronic devices and circuits. Proper understanding of these factors is crucial in determining high-temperature applications. The MOSFET device characteristics and circuit behavior that changes with the increase in temperature can be predicted and simulated with a suitable model. Precise modelling of temperature dependency of MOSFET parameter have great importance. A study of the impact of temperature on some of the parameters of MOSFET like threshold voltage, subthreshold leakage current, saturation velocity, are complete by using MATLAB and the variations of MOSFET dc features are studied.

Electrical power is a essential part of our life. Although energy cannot be destroyed, it does change forms and can be lost through work, friction, or dissipated as heat. Therefore, device is heated power consume improved. As a result, there is a limited amount of energy in the

form of electricity. We need to know where power is consumed is necessary improve efficiency and conserve valuable electricity. MOSFETs are popular in electrical components.

MOSFETs are special type of transistors which contain four terminals, namely the Gate, Body, Source and Drain. An electrical connection is opened between the Source and the Drain terminals when a sufficient voltage is supplied from the Gate to the Body terminal. Electrical device, MOSFETs has consume power.

The integral of a function in the (current-voltage) plane is the area under the curve which may be interpreted as the product of current and voltage. Therefore, the power consumption can be determined by finding the integral of the function generated by a MOSFETs . MOSFETs operate in one of three stages:

1) Cutoff mode

2) Triode mode

3) Saturation mode.

During the cutoff region, the gate source voltage is deficient to activate the transistor and the bias between the source and drain terminals stay locked. During the triode region the gate voltage is enough to established a weak bias between the source terminal and the drain terminal. In this mode the transistor acts like a resistor whose resistance is a function of the voltage applied to the gate terminal. Finally, when sufficient voltage is applied to the gate terminal the transistor enters saturation mode and a full connection is established between the source and drain terminals. A MOSFET in cutoff mode will consume no power as there is no connection between the source and drain terminals and a MOSFET in saturation region consumes a fixed amount of power as the bias between the source and drain is fully open. For the remainder of this paper we explored the variable temperature of a MOSFET during its different parameter.

CHAPTER 3

LITERATURE REVIEW

In this chapter we review the latest findings in the domain of various temperature changes of MOSFET parameters. We begin with a review of development of the idea of the MOSFETs, and their future prospects in a theoretical perspective. Then we look at various experimental realizations of temperature and different parameter changes of MOSFETs.
I carefully study The paper,

1). Shruti Kalra1, A.B. Bhattacharya2 "An Analytical Study of Temperature Dependence of Scaled CMOS Digital Circuits Using α-Power MOSFET Model" 1,2Department of Electronics and Communication, Jaypee Institute of Information Technology, Noida, India e-mail: shruti.kalra@jiit.ac.in and paper

2). Jitty Jose, 2Keerthi K Nair, 3Ajith Ravindran 1P.G Scholar, 2P.G Scholar, 3Assistant Professor " Analysis of Temperature Effect on MOSFET Parameter using MATLAB" Electronics and communication Engineering, Saintgits College of Engineering, Kottayam India, © 2016 IJEDR | Volume 3 and 4, Issue 3 | ISSN: 2321-9939

3). F. Gamiz, J. A. L6pez-Villanueva, Member, IEEE, J. Banqueri, "Universality of Electron Mobility Curves in MOSFETs: A Monte Carlo Study" J. E. Carceller, Member, IEEE, and P. Cartujo, Member, IEEE

4). Gayatri Gaikwad 1, Milan Sasmal2 , Sudhir Lande3, "SIMULATION AND ANALYSIS OF TEMPERATURE EFFECT ON 7 nm n-MOSFET" Engineering and Technology, Baramati, India. 1,2,3gayatri.gaikwad@vpkbiet.org1,milan.sasmal@vpkbiet.org2, sudhir.lande@vpkbiet.org3

5). Any other papers After all papers I came to know that the relation between the Temperature and mosfet's parameter, which are briefly describe in next chapter.

CHAPTER 4

Modelling of MOSFET DC Characteristics in Different Temperature Using COMSOL Multiphysics Software.

Software environment with its individual Graphical User Interface. The GUI is used to analyze the I-V characteristics of MOSFET at nanoscale and displays the curves and constraints such that a user can envision the voltage and current differences as well as different type of leakage currents. The user interface too plays a vital role in monitoring the application's concert to suit the user's requirements. The objective of this work is to make an easy understanding of MOSFET at nanoscale using a simple simulator with simple MOSFET equations. This simulator has the capacity to take the input from user, and creates the characteristic curve and equivalent parameters. This parameter is controlled by the device manufacturing and design process. This can be examined from its electrical response.

4.1 Variation of Drain Current Over Drain Voltage in Different Temperature

To analyze the Si MOSFET (n-doped) response in different drain-source voltage, different gate voltage and for different temperature one 2D MOSFET model developed in COMSOL Multiphysics. In this model MOSFET biasing in different temperature (30K, 300K, 320K, 340K, 380K) with different gate (2V, 3V, 4V) and drain (0 to 5 V) voltages has been considered.

MATERIAL:

I used **Si** material in this model. The details of material property is given below.

MESH:

Mesh is a collection of polygons or geometric objects. For that instant, triangles, quads or some various polygons mixtures. A mesh is a simply but more complex shape. Therefore, we have nodal representation of the geometry. The mapped mesh with the specific distribution creates a thin layer elements of the gate. By use the mesh to resolved the large gradient of the carrier concentration.

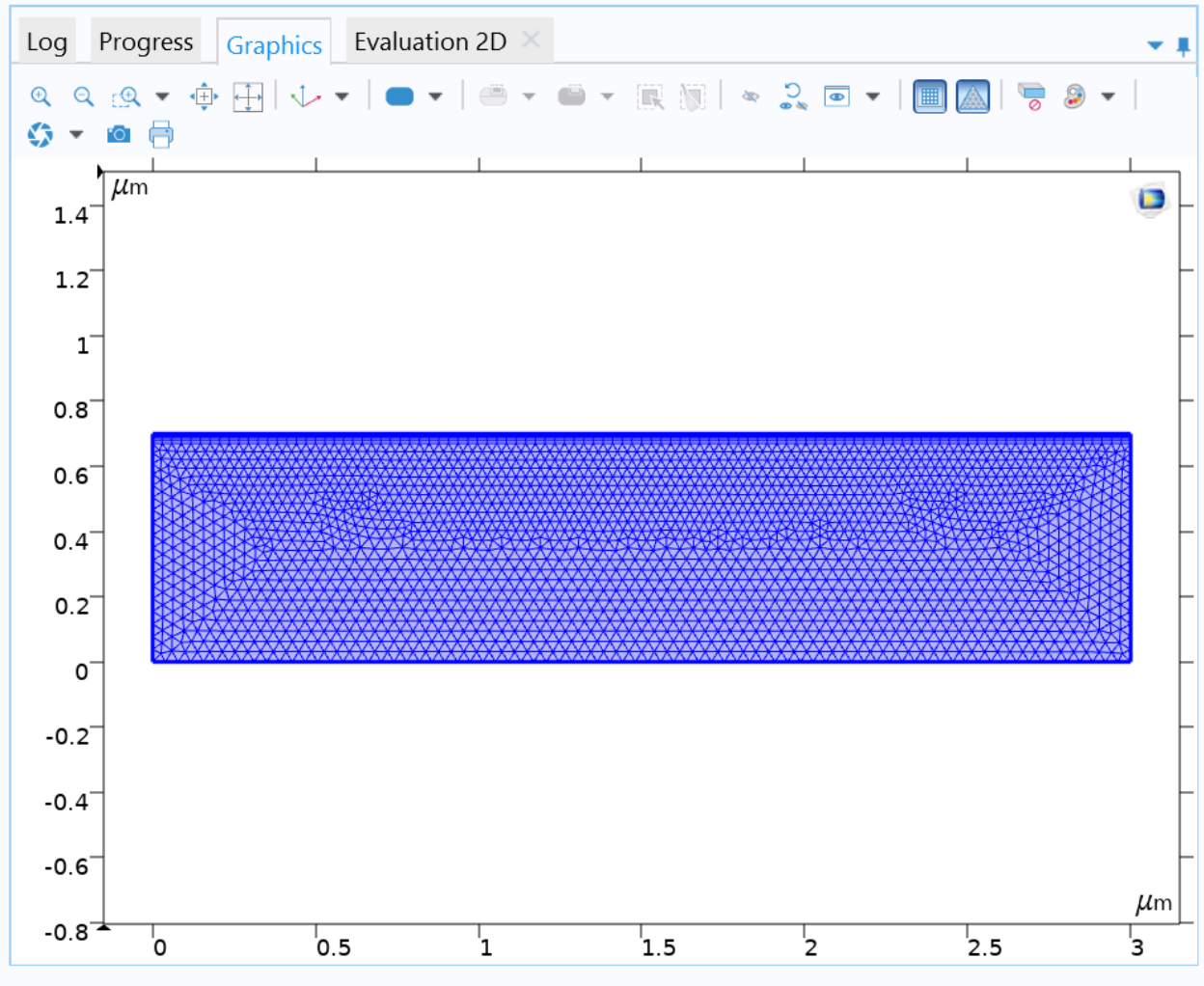


Figure4.1: The user defined mapped Mesh

Geometry:

Table:1: Parameter is used in the geometry model

Parameter Name	Parameter Value	Parameter
L	1E-6m	Device channel length
Wd	0.6E-6m	Device channel width
Ws	0.1E-6m	Source width
Wdd	0.1E-6m	Drain width
Hd	0.5E-6m	Device hieght
Nd	1E+20/cm^3	Doping concentration

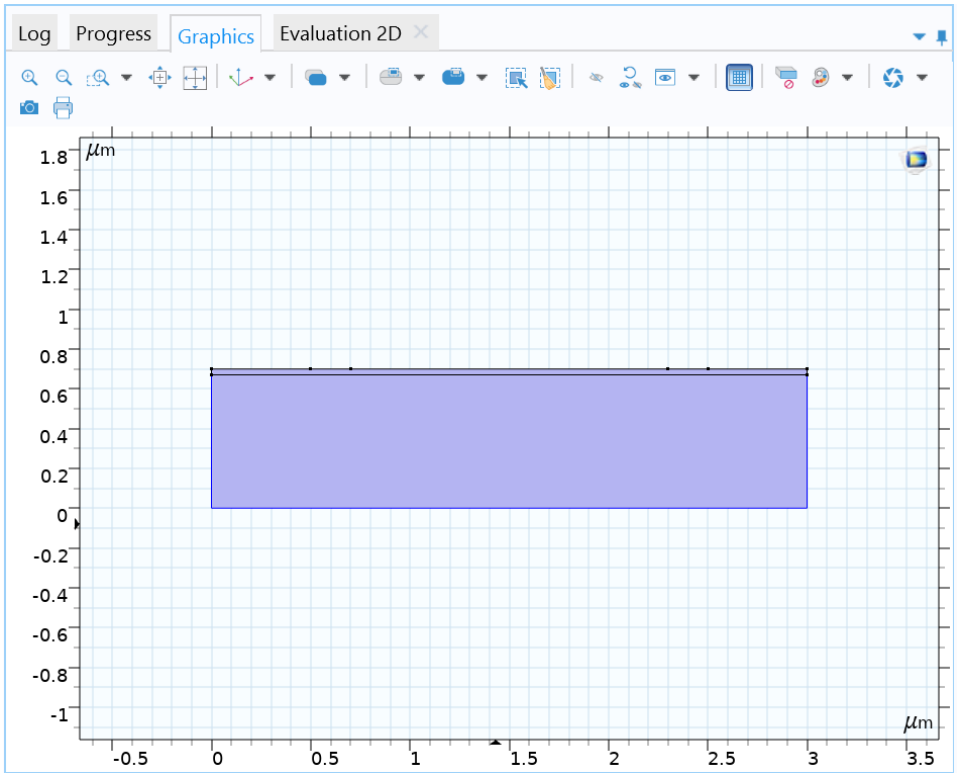


Figure:4.2. a).MOSFET Model Geometry

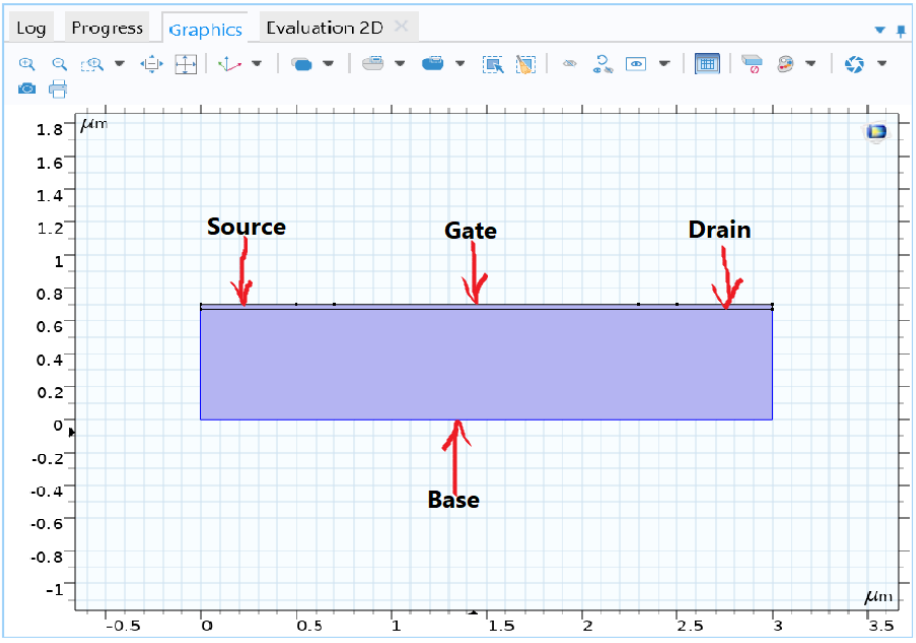


Figure:4.2. b).MOSFET Model Geometry .This Figure Shows The Source, Gate And Drain

MOSFET Different characteristics using COMSOL Multiphysics

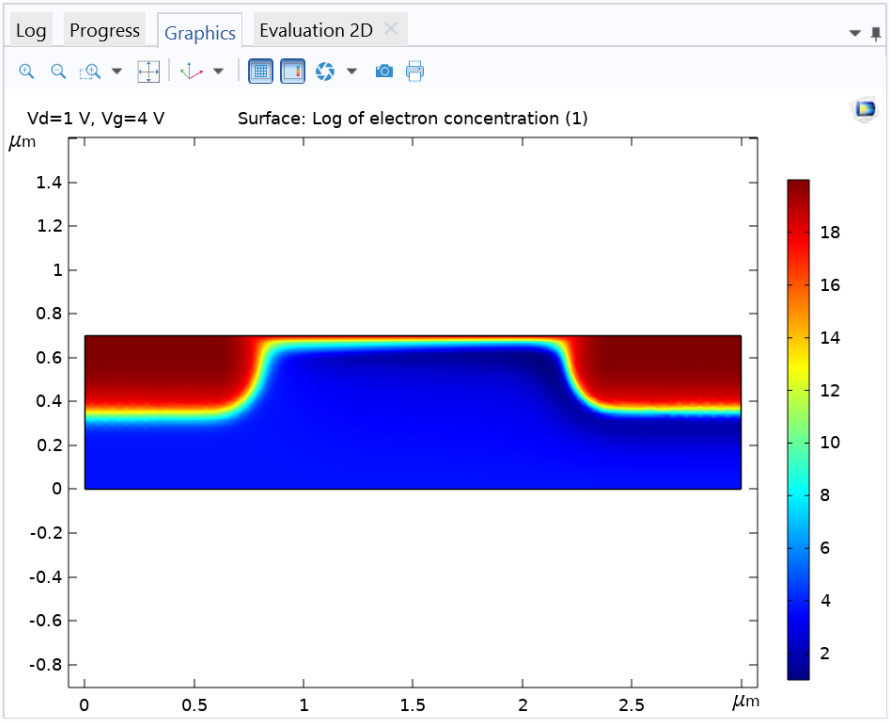


Figure:4.3. The electron concentration of the device at Vd=5v. The pinch-off of the channel is apparent 5v

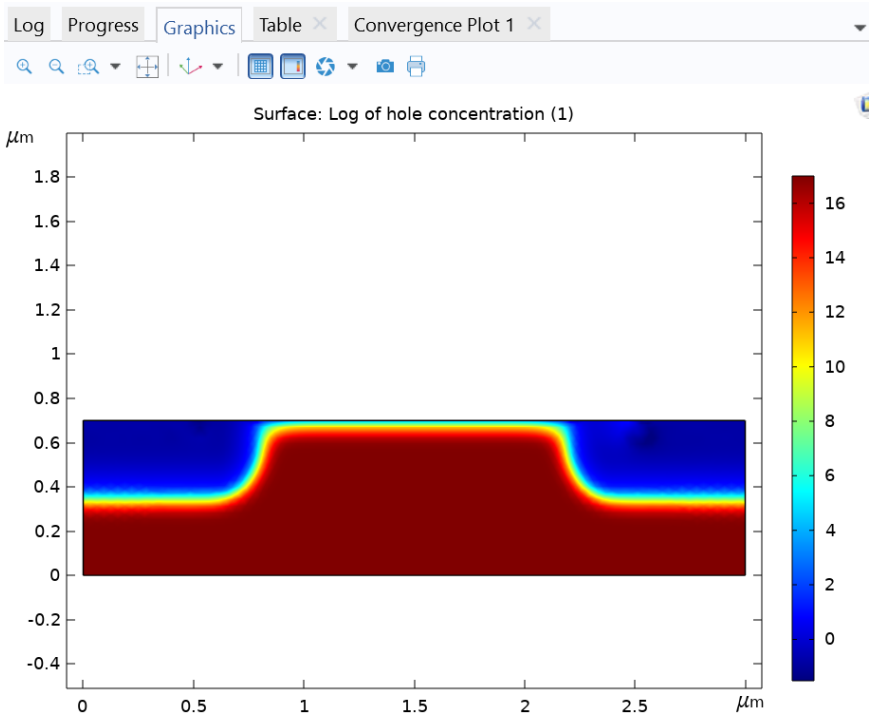


Figure:4.4 The hole concentration of the device at Vd=5V. The pinch-off of the channel is apparent 5V.

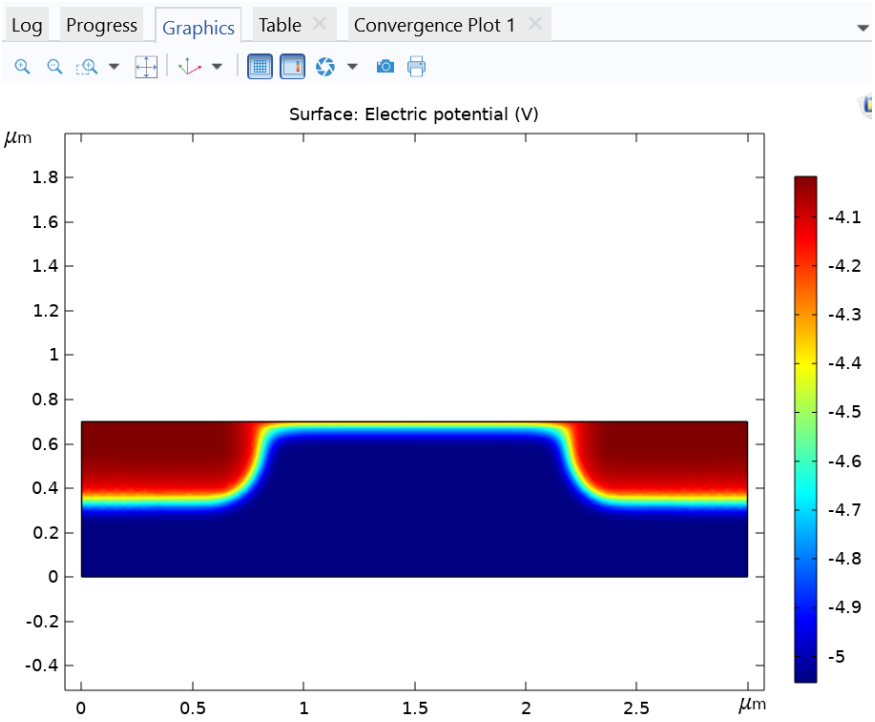


Figure:4.5 The electric potential of the device with Vd=5V.

Characteristic Curve of MOSFET :

This model was computed by different gate voltage (2V, 3V, 4V,) respectively in the drain voltage from 0V to 5V. this simulation was completed in different temperature (30K, 283.15K, 300K, 320K, 340K, 380K). the variation of drain current I_d in different values of drain voltage V_d from 0 to 5v at different temperature.

Table:2: Value of I_d in different temperature with V_g=2V

V_d (Volt)	I_d(μA) T=30K, V_g=2V	I_d(μA) T=283.15K, V_g=2V	I_d(μA) T=300K, V_g=2V	I_d(μA) T=340K, V_g=2V	I_d(μA) T=380K, V_g=2V
0	-0.00108780	-2.62E-04	-4.01E-04	-2.53E-04	-3.37E-04
0.25	11.76405978	17.99569694	18.57279677	19.99345578	21.48289731
0.5	13.73583531	24.65313863	25.72910569	28.39613741	31.21133682
0.75	14.05137587	25.86684545	27.10926718	30.25922505	33.68946861
1.0	14.244498	26.30909401	27.58650016	30.8369026	34.40008501
1.25	14.40461101	26.62709038	27.92360626	31.22509498	34.84884979
1.5	14.54101712	26.89124962	28.20247175	31.5424572	35.21024426
2.0	14.78585096	27.34456555	28.67890514	32.07854377	35.81322312
3.0	15.17836193	28.06821755	29.43853068	32.9305107	36.76771985
4.0	15.51568988	28.66489318	30.06311475	33.62632852	37.54203636
5.0	15.81053628	29.19028697	30.61290623	34.23816259	38.22189173

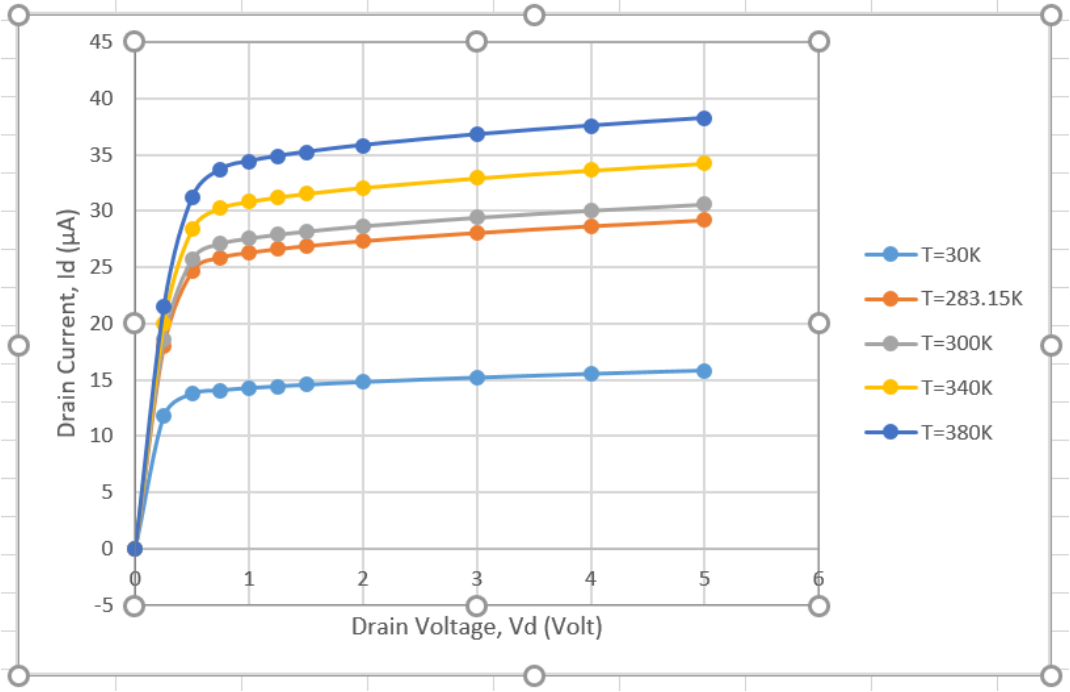


Figure:4.6. V_d-I_d Characteristics in different temperature with Vg=2v

From the above figure it is seen that at higher temperature the value of I_d is higher at a particular value of V_d.

Table:3: Value of I_d in different temperature with V_g=3V

V_d (Volt)	I_d(μA) T=30K, V_g=3V	I_d(μA) T=300K, V_g=3V	I_d(μA) T=320K, V_g=3V	I_d(μA) T=340K, V_g=3V	I_d(μA) T=380K, V_g=3V
0	0.003007463	-8.97E-04	-7.27E-04	-5.54E-04	-7.06E-04
0.25	44.82829805	50.29333659	50.90442044	51.53660495	52.8598593
0.5	77.41570097	88.10151888	89.28894346	90.51613352	93.07942129
0.75	98.6386407	114.3145599	116.0563321	117.8542553	121.6022377
1.0	110.0974649	130.2584546	132.5108799	134.8356662	139.6801677
1.25	115.1584016	138.3776298	141.0204068	143.7543197	149.4682977
1.5	117.5401795	142.2098564	145.0621089	148.0217549	154.236061
2.0	120.2646158	146.0120479	149.0155251	152.1384913	158.7180624
3.0	123.8466915	150.5741602	153.696722	156.9452057	163.7950362
4.0	126.6255026	153.9786676	157.179091	160.5090824	167.5324147
5.0	129.025049	156.8737741	160.1330189	163.5245061	170.6783283

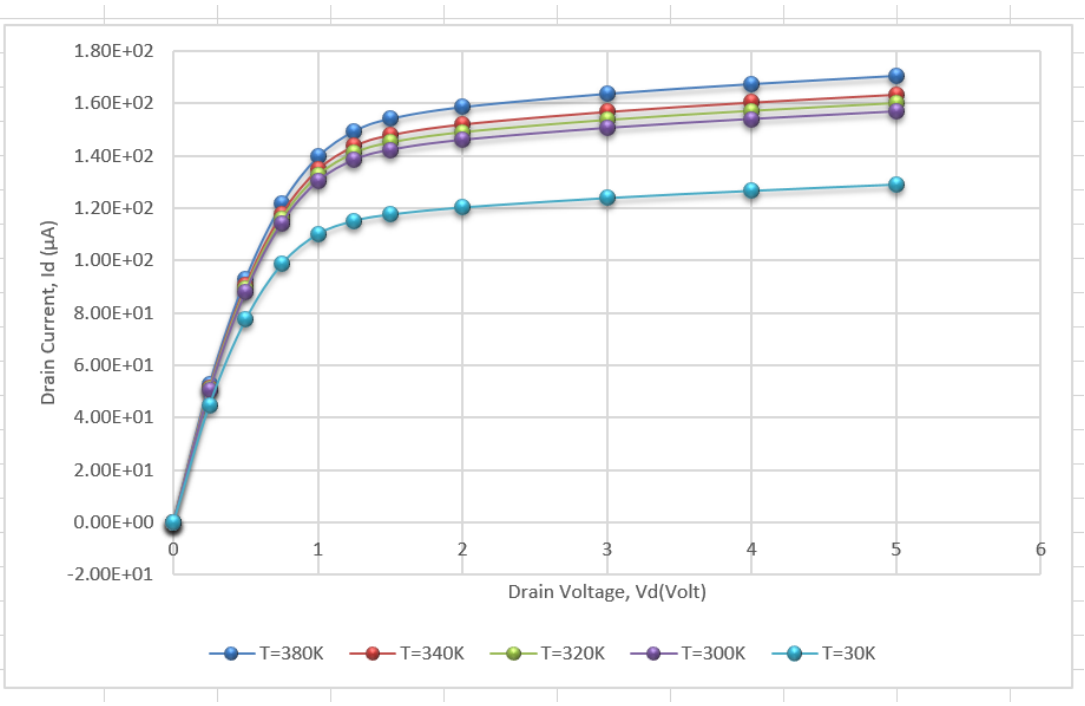


Figure:4.7. V_d-I_d Characteristics in different temperature with Vg=3v

Table:4: Value of $I_d - V_d$ in different temperature with V_g=4V

V_d (Volt)	I_d(μA) T=30K, V_g=4V	I_d(μA) T=300K, V_g=4V	I_d(μA) T=320K, V_g=4V	I_d(μA) T=340K, V_g=4V	I_d(μA) T=380K, V_g=4V
0	-0.00486608	-0.00138233	-0.0011146	-8.52E-04	-0.00106844
0.25	76.95085857	81.98336491	82.55113286	83.14099652	84.37844758
0.5	141.860649	151.5314776	152.6242321	153.7562003	156.1306174
0.75	195.2828217	209.2652868	210.8559996	212.502402	215.9513707
1.0	237.7000044	255.7847	257.8517964	259.9915333	264.4687712
1.25	269.8083927	291.7734475	294.2977389	296.9098226	302.3724739
1.5	292.6313923	318.1471764	321.1002097	324.1562805	330.546525
2.0	317.1669055	347.9639693	351.5942438	355.3573514	363.2419466
3.0	333.313882	367.6623399	371.7699255	376.0395625	385.0227962
4.0	341.9289693	377.5100943	381.7687185	386.1962085	395.5150518
5.0	348.7927843	385.1350562	389.4916052	394.0222054	403.5616988

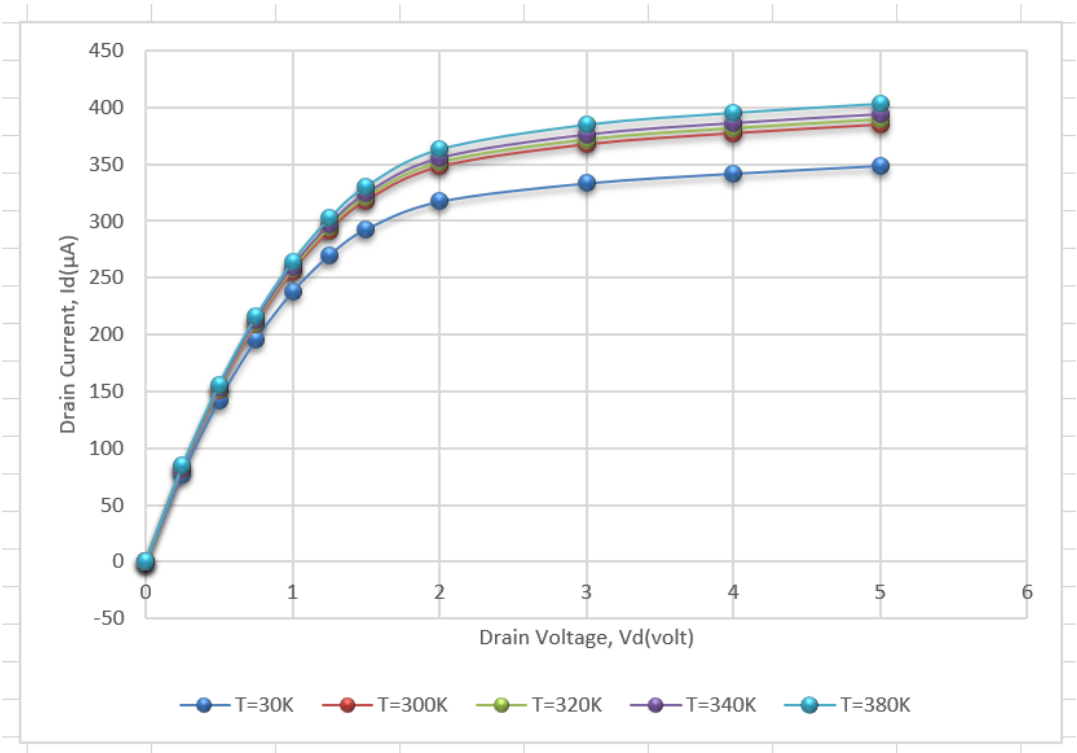


Figure:4.8. V_d-I_d Characteristics in different temperature with Vg=4V

Table:5: Value of I_d in different V_g with V_d=10mV

V_g (volt)	I_d (μA)
0	2.56E-09
0.2	1.28E-07
0.4	1.32E-09
0.6	3.73E-07
0.8	1.95E-05
1	0.001347
1.2	0.051507
1.4	0.242647
2	0.982583
3	2.252506
4	3.517403

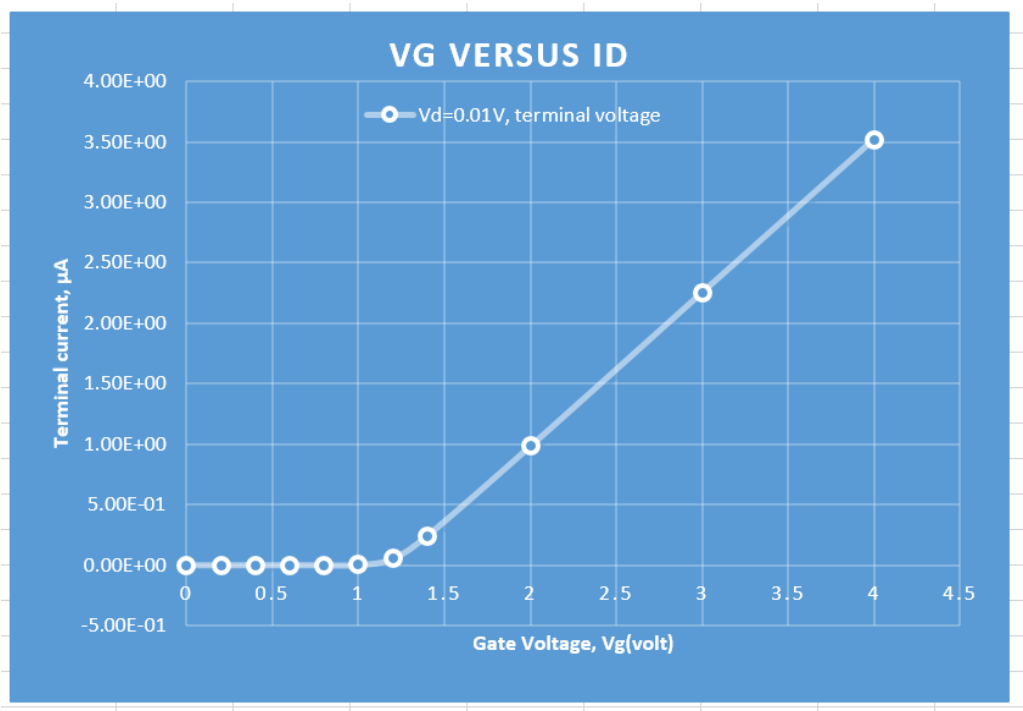


Figure:4.9. This figure shows that the characteristic of gate voltage with zero bias.

From the plot it is clear that the threshold voltage of MOSFET is 1.2V. It is possible to compare the theoretical value given by (S. M. Sze and K. K. Ng. Physics of Semiconductor Devices, Wiley, Hoboken, New Jersey).
The threshold voltage V_T ,

$$V_T \cong V_{FB} + 2\psi_B + \frac{d_{ox}(4\varepsilon_{r,s}\varepsilon_0 qN_a\psi_B)^{\frac{1}{2}}}{\varepsilon_{r,ox}\varepsilon_0} \quad \text{.....(19)}$$

Table:6: Value of I_d in different temperature T with V_g=4V

T(K)	I_d (Vd=0.25) μA	I_d (Vd=0.50) μA	I_d (Vd=0.75) μA	I_d (Vd=1.0) μA	I_d (Vd=1.25) μA
283.015	81.52	150.64	207.97	254.1	289.71
288	81.65	150.9	208.34	254.58	290.3
293.15	81.79	151.17	208.73	255.09	290.93
298	81.93	151.42	209.11	255.58	291.52
300	81.98	151.53	209.27	255.78	291.77
303.15	82.07	151.7	209.51	256.11	292.17
306	82.15	151.86	209.74	256.4	292.53
310	82.27	152.01	210.06	256.81	293.03
320	82.55	152.62	210.86	257.85	294.3
340	83.14	153.76	212.5	259.99	296.91
380	84.38	156.13	215.95	264.47	302.37

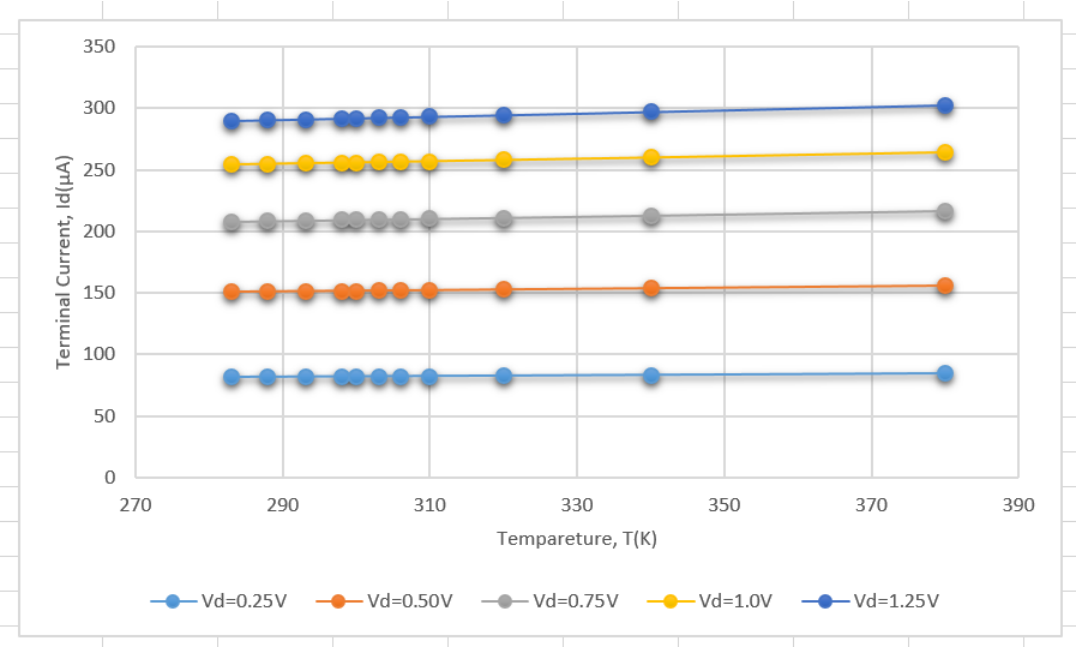


Figure:4.10. Terminal current varies with temperature at constant gate voltage and drain voltage.

In the above figure we see that the terminal current increase in very small with the temperature when applied potentials are fixed. As a result we can say the device is very sensitive.

CHAPTER 5

TEMPERATURE VARIATION OF MOSFET PARAMETERS

5.1 Carrier Mobility

Carrier mobility can be thought about as one of the pivotal temperatures depending on MOSFET parameter. The bearer is commonly mentioned to electrons and holes. In semiconductor physics, the electron mobility mention to how fast an electron will move through a metal or semiconductor material, when pulled by an electric field. In semiconductor, there is a similar quantity for holes, called hole mobility. The viscosity of a semiconductor is directly proportional to the product of carrier concentration and carrier mobility. Whenever all the things are equal, higher mobility leads to better device showing.

Element turn on up on the mobility of carriers in the semiconductors are contributor and go along with concentration, fault concentration, and the temperature. From the Bose - Einstein distribution, it reveals that phonon scattering is actively a temperature depending on enlarge parameter. So the density of phonon increases with the increase of temperature, which causes increase in scattering. Thus, lattice scattering under the carrier mobility increasingly at higher temperature. The carrier mobility is the important parameter for the fractional simulation of the electrical features on semiconductor devices. To catch the vulnerability of mobility on temperature, doping, and the electric field, different numerical models were grown. The carrier mobility is given by the equation

$$\mu(\mathrm{T}) = \mu\,(T_r)\left(\frac{T}{T_r}\right)^{k\mu} \quad \text{.....(20)}$$

for the temperature 0 to 300K

$$\mu(\mathrm{T}) = \mu\,(T_r)\left(\frac{T}{T_r}\right)^{-k\mu} \quad \text{.....(21)}$$

for the temperature 300 to 600K

Where,

T = Absolute temperature, Tr = Room temperature

kμ = Fitting parameter with a typical value of about 0.6

μ (T_r)= ref. temp (300K) = 0.14 m²/v.s

The analytical modelling of carrier mobility is revels the inverse relationship between temperature and carrier mobility.

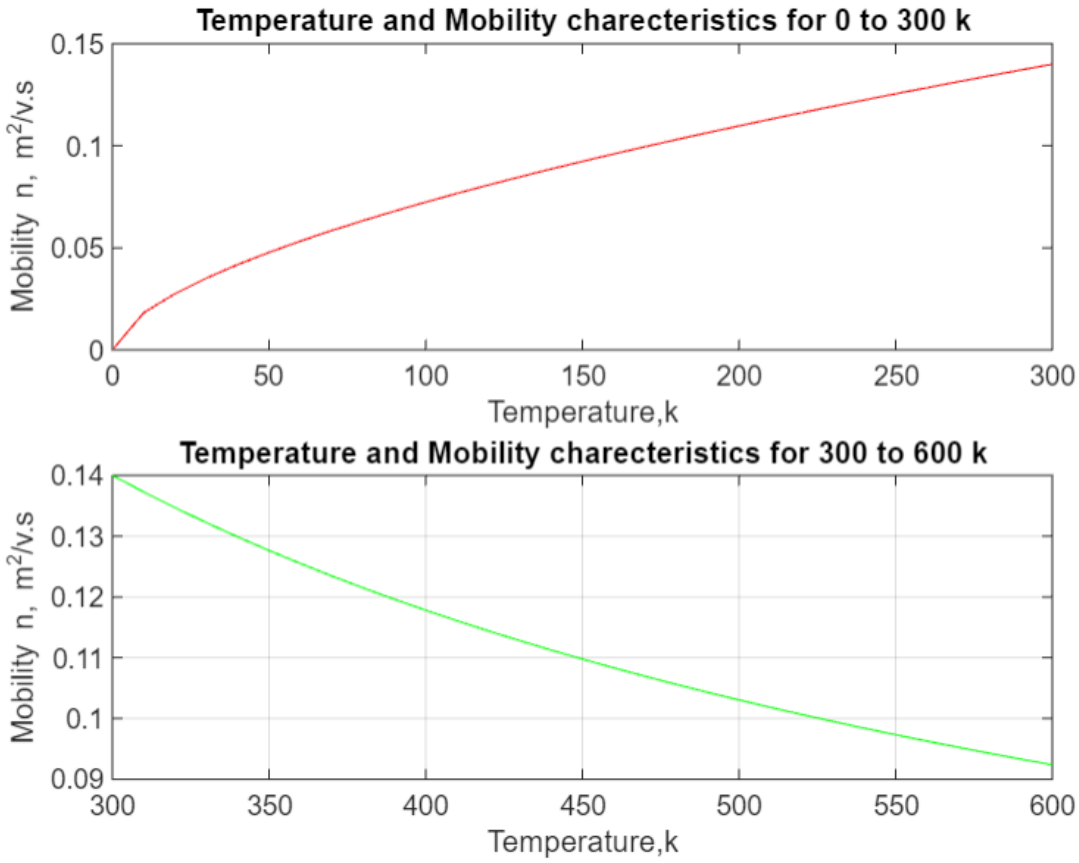


Figure:5.1. This figure shows that the mobility varies with temperatures

The value of carrier velocity for Si at ambient temperature, 300K is 0.14 m² / V.s which matches the conceptual value. A 100 ° C, in temperature may reduce the mobility by as much as 40 %. The result is a corresponding reduce in drain current, for a secure applied voltage.so current consumption of the whole circuit may decrease at giant temperature. The maximum momentum of operation thus reduces in proportion. The change in threshold voltage and mobility impact the drain current, the Trans conductance, and the drain to source ON resistance of MOSFET.

Here we saw that the mobility increase by the temperature increase with 0k to 300k. Therefore, at low temperature, the mobility proportional to the temperature. Again the mobility decrease by the temperature increase with 300k to 600k. so we can say that the mobility is inversely proportional to the temperature, use MATLAB code.

MATLAB code is given on page no. 52

5.2 Contact Region Resistance

The fast-growing CMOS technologies, lack of proper understanding of the physical and analytical apparatus implement of sponging resistance will leads to the depreciation of better showing of device used in various VLSI circuit applications. As CMOS technology push forward, the junction depth of the source / drain and size of other related device features are

being ambitiously reduced so the effect of source / drain resistance on the device performance become increasingly significant. As the CMOS technology advances, the parasitic drain / source resistance component does not scale with device dimensions and thereby donate a substantial fraction of the total resistance, resulting in appreciable degradation of current driving ability. Additionally, for the investigation of Schottky contact MOSFET, require representation of the silicide / Si contact resistance is exploitative. Contact resistance component's freeloading resistance is not adjustable as it directly increases with reduce in junction size equivalent with device scaling. Temperature effects involved in the contact resistance become more momentous in the deep submicron device rule, especially under greater current stress conditions. The exchange of resistance can be deliberate by the calculation

$$R_{DS} = 920 - \frac{4}{3}(T - 300) \quad \text{.....(22)}$$

R_{DS} = Total drain and source contact region resistance at high temperature.

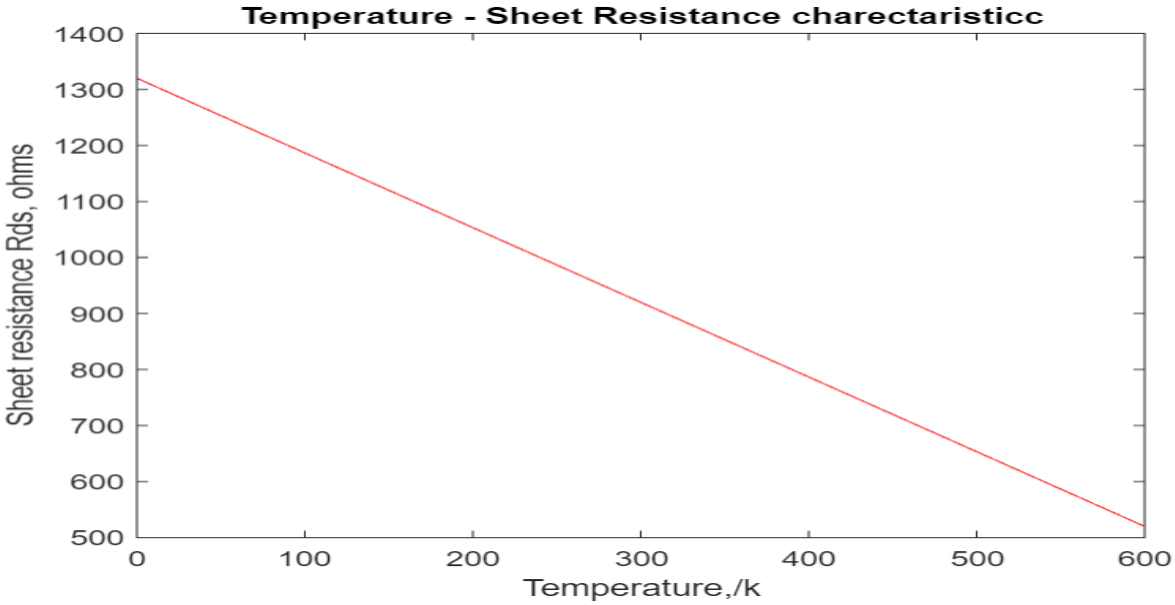


Figure: 5.2 MOSFET drain resistance varies with temperature

The parasitic resistance is also known as sheet resistance. The sheet resistance variation with temperature is shown in figure. From the graph it is observed that the value of sheet resistance at 600 K becomes almost half of the value at 300k Therefore, smaller voltage drop occurs at drain and source contacts, and the channel has more drain to source voltage, which eventually causes the drain current to increase. The resistance values reduce in linear manner. Therefore, a linear approximation has been made in the calculation of the resistances.

MATLAB code is given on page no. 53

5.3 Threshold Voltage and Potential at a Point of the Channel

Threshold voltage (Vth or Vtn) influences the static and dynamic modes of operations of the MOSFET. In digital circuits the threshold voltage is usually generalized as 20 % of the supply voltage while the typical values of threshold voltage vary from 0.5-1.5V and it is perhaps the most variable parameter of a MOS transistor. Moore's law is kept on the go by transistor miniaturization along with increasing packing densities. This leads to densely packed VLSI and ULSI circuits, the major disadvantages of this high-density circuits are the intense heat generated as they operate normally at high temperatures. This results in shame of the subthreshold decline of the device and increasing the power scatter via off state leakage.

These factors lead to show corrupt of the device and leads to integration issues. Threshold voltage is the critical parameter that decides the transistor operation. Almost all the operational characteristics of the transistor depends on the Vth. Even transistor concept is made in terms of threshold voltage, difference in threshold voltage causes severe variations, mainly in the operational frequency, in some cases operational frequency may vary up to 30 % within the same chip. Threshold voltage variations also leads to enlarge leakage current that degrades the overall show of the device in terms of increased power disperse.

The basic MOS current equation gives the drain current and how it is related to gate to source voltage (VGS) and Vth. This reveals that MOSFET current - voltage characteristics are proportional to the square of the difference of gate voltage and threshold voltage. A very small change in the threshold voltage can have a great impact on the output characteristics as it has a squared effect, hence it is important to accurately measure the threshold voltage that changes with the change in temperature of operation.

Mathematical modelling of Vth can be done by manipulating the physical properties of the transistor such as gate metal, channel doping, oxide thickness and pocket implants. Based on these physical quantities one can derive analytical expressions for the threshold voltage,

$$Vtn = Vto + \gamma\left(\sqrt{v_{sb}} + 2\emptyset f\right) - \sqrt{2}\emptyset f \quad \text{.....(23)}$$

$$\gamma = \frac{tox}{sox}\sqrt{2}q\varepsilon_{si}Na \quad \text{.....(24)}$$

$$\emptyset f = \frac{KT}{q}\imath n\frac{Na}{Ni} \quad \text{.....(25)}$$

The intrinsic carrier concentration Ni varies with temperature and is given by Eq

$$Ni = (N_c N_v)^{\frac{1}{2}}\exp(-E_{g//_{2kT}}) \quad \text{.....(26)}$$

where Nc and Nv are the density of states in the conduction and the valence band and is given by

$$N_c \cong 1.73 \times 10^{16} T^{\frac{3}{2}}$$

$$N_v \cong 4.8 \times 10^{15} T^{\frac{3}{2}}$$

of is the fermi potential of the body which increases with the decrease in temperature. Ni is the carrier concentration. of intrinsic silicon, NA is the substrate doping concentration and KT / q = Vt is the temperature dependent potential. y represents the body effect parameter, q the charge of an electron and cox is the permittivity of oxide

The electron concentration in the channel becomes equal to the hole concentration in the substrate when the voltage drop from channel to substrate is equal to two times the fermi potential and this is when the channel is defined as inverted. When no substrate biasing is applied, Ie at VSB = 0 the threshold voltage is represented as Vto . From the Vt verses temperature characteristics, it is clear that on lowering the temperature the threshold voltage decreases and they have a linear relationship. So, operating at lower temperature will be of advantage for MOS device operations as the threshold will be low and hence faster operations becomes possible.

The built in potential can be cancelled out by applying a gate voltage that is equal in magnitude but of the opposite polarity as the built in potential. The gate voltage is called the flatband voltage because the resulting potential profile is flat.

$$V_{GB} - V_{FB} = V_{ox} + v_S \quad \text{.....(27)}$$

If we know that the total charge within the semiconductor (Q'_S), we can find the electric field within the gate insulator (E_{ox}) and hence the voltage drop across the gate insulator(V_{ox}):

$$\oint E.dS = E_{ox}A = \frac{-Q'_S}{\varepsilon_{ox}} \quad \text{.....(28)}$$

$$V_{ox}=E_{ox}t_{ox} = \left(\frac{-Q'_S}{A\varepsilon_{ox}}\right)t_{ox} = \frac{-Q_S}{C_{ox}} \quad \text{.....(29)}$$

Where Q_S is the total area charge density [C/cm^2] in the semiconductor channel(MOSFET)

And $C_{ox} = \varepsilon_{ox}/t_{ox}$is the areal gate capacitance.

The potential at a point of the channel is given by

$$V(x)=(V_{GS} - V_T) - \frac{Q_S}{WC_{ox}} \quad \text{.....(30)}$$

Where W is the width of the channel.

MATLAB code is given on page no. 54

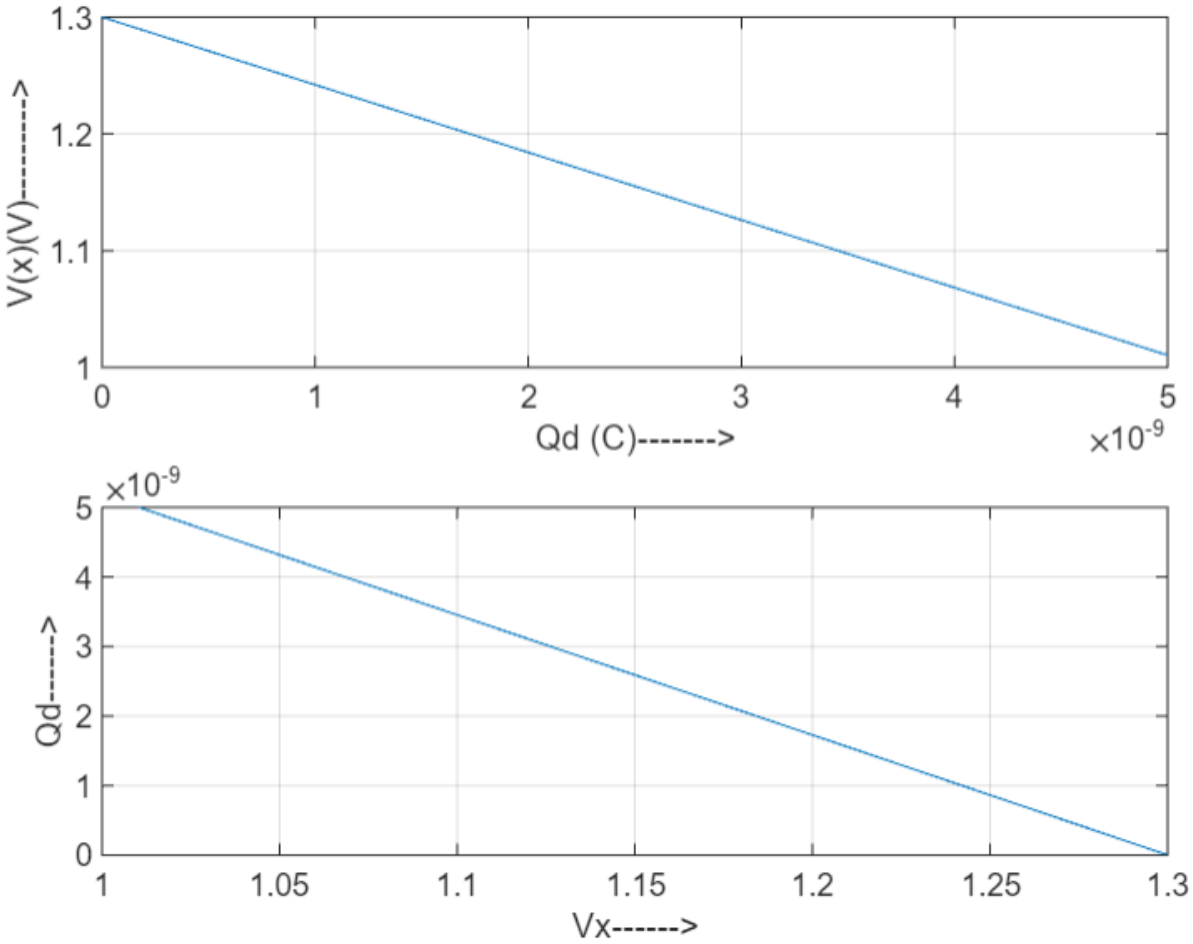


Figure: 5.3. Variation of the charge in the depletion region with voltage at any point of the channel and vice versa.

1.3 Subthreshold Leakage Current

Subthreshold leakage current can be used in case of low power devices like TFETS FINFETs etc. But in normal transistors this leakage problem creates serious issues as it leads to power dissipation in the off-state condition. As temperature rises, the threshold voltage decreases and the subthreshold leakage current increases exponentially with increase in temperature. So, this leakage becomes a severe problem in the case of devices operating at high temperatures. So, leakage current can become a limiting factor in the temperature functionality of MOSFETS.

The subthreshold leakage, usually abbreviate d as las depends exponentially on temperature. The relation or the dependence of leakage current with operating temperature is given by the following expressions.

$$I_{ds} = I_{dso} e^{\frac{V_{gs}-V_t}{nxvt}\left(1-e^{\frac{-V_{ds}}{vt}}\right)} \quad \text{.....(31)}$$

Where,

$$I_{ds0} = \beta vt^2 e^{1.8} \quad \text{.....(32)}$$

$$V_t = V_t(T_r) - k_{vt}(T - T_r) \quad \text{.....(33)}$$

$$V_t = \frac{KT}{q} \quad \text{.....(34)}$$

$$\beta = \frac{\mu_n \times Cox \times W}{L} \quad \text{.....(35)}$$

$$\mu_n = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu} \quad \text{.....(36)}$$

V_t is the threshold voltage, $\upsilon_t$is the thermal voltage, μ_n denote mobility of carriers. kμ is the Fitting parameter, Vgs is the gate to source voltage, Vds is the drain to source voltage, T denotes temperature in Kelvin, q the charge of an electron, Cox is the oxide thickness, and W & L. are the width and length of the device.

The standby power of a device depends on the subthreshold leakage current, as it is related exponentially to the temperature. Stand by power also increases exponentially with the grow in temperature. This exponential rise in the subthreshold behavior is because of to the exponential entire dependence of the minority charge carriers and their density. The la exponentially rises with temperature as the supply voltage. So, in general t go for reducing the leakage issue, scaling down of the supply voltage is done.

The rapidly rise in the leakage current. This is the basic restriction of the MOSFET that is as scaling Free Poor done the OFF current grow exponentially leading to increased power dissipations and limiting the temperature-based functionality of the device. The case room temperature in the case of MOSFET, the leakage roughly equal to 1m which is current that is la is around equal to 1mA which is negligible and as the temperature increases, the leakage increases leading to increased OFF state current or increased stand by power. At 400K the subthreshold current is 25mA which of which is a very high value, so this limits the

temperature-based functionality of the device. Far away this 400K the normal deductive is made as when the temperature is increased by 10 degrees or 10K the leakage current gets doubled.

MATLAB code is given on page no. 53

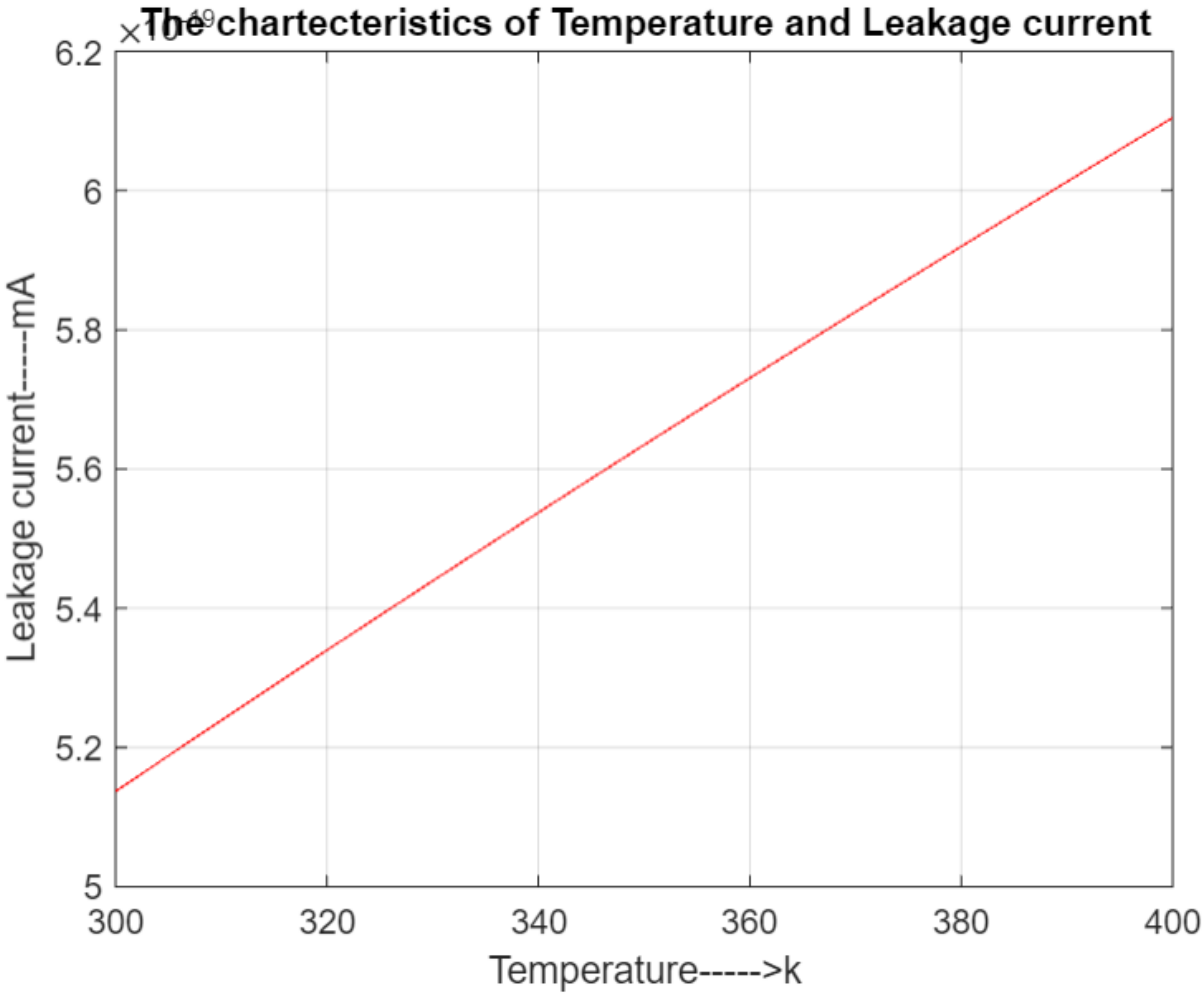


Figure: 5.4. The relation of the dependence of leakage current with operating temperature

1.3 Source to Drain On Resistance

The study of temperature dependency on source to drain resistance of MOSFET is highly relevant because it determines the maximum current rating and loss. In a MOSFET source to drain ON resistance may be named as the total resistance between source and drain during the ON condition. In order to decrease the origin to drain ON resistance, trench technique and probity of the chip 15 used. The source to drain ON resistance of MOSFET are given by the formula.

Where, R_N denotes the resistance between source region and N + diffusion region. This parameter can be ignored in high voltage MOSFETS. RCH is the channel resistance. The factors turn on channel resistance are ratio of channel width to the length, the thickness of oxide. and the gate drive voltage, R_A indicates the accumulation region resistance which is depended on the mobility of the carriers at the the surface. R_J is the resistance uniting N ° epi regions between the P - bodies. RD is the resistance in between top of the substrate and p body. The resistance of substrate region is indicated by R_S.

Spring to drain ON resistance have positive temperature coefficient. This is cause mobility of carriers (holes and electrons) reduce with increase in temperature. The temperature result of source to drain on resistance is given by the equation.

$$R_{DS(on)}(T) = R_{DS(on)}(25℃)\left(\frac{T^n}{300}\right) \quad \text{.....(37)}$$

1.3 MOSFET Characteristics:

Metal Oxide semiconductor field effect transistor(MOSFET) is a four-terminal device semiconductor device. The terminals are the gate, source, drain and substrate. There are two types of MOSFET, such as the enhancement type and depletion type. The channel between the source and drain to be induced by applying a voltage on the gate in enhancement MOSFET. In the depletion type MOSFET there exist a channel between the source and drain. The oxide insulation between gate and the channel MOSFET have high input resistance. MOSFET can be operated in three modes: cut-off, triode and saturation regions. The enhancement type MOSFET is widely used, the presentation in this section will be done using an enhancement type MOSFET. The channel between the source and drain to be induced by applying a voltage on the gate. The voltage needed to create the channel is called the threshold voltage, V_T. For n-channel enhancement type mosfet, V_T is positive and p-channel device it is negative.

5.6.1 Cut-Off Region

For an For n-channel MOSFET, if the gate-source voltage V_{GS} ,

So $V_{GS} < V_T$

Then the device is cut-off. This implies that the drain current is zero for all values of the drain-to-source voltage.

5.6.2 Triode Region

When $V_{GS} > V_T$ and V_{DS} is small, the mosfet will be in the triode region. In the latter region, the device behaves as a non-linier voltage-controlled resistance. The I-V characteristics are given by

$$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \text{.....(38)}$$

$provided$

$$V_{DS} \leq V_{GS} - V_T$$

$where$

$$K_n = \frac{\mu_n \varepsilon \varepsilon_{ox}}{2t_{ox}} \frac{W}{L} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \quad \text{.....(39)}$$

and

μ_n	is surface mobility of electrons
ε_{ox}	is dielectric constant of SiO_2
ε	is permittivity of free space (8.85E-14 F/cm)
t_{ox}	is thickness of the oxide
L	is length of the channel
W	is the width of the channel

5.6.3 Saturation Region

MOSFET can operate in the saturation region. A MOSFET will be in saturation provided

$$V_{DS} \geqslant V_{GS} - V_T$$

$and\ I - V\ charecteristics\ are\ given\ as$

$$I_D = K_n(V_{GS} - V_T)^2 \quad \text{.....(40)}$$

The dividing locus between the triode and saturation regions is obtained by substituting

$$V_{DS} = V_{GS} - V_T$$

In to the drain current equation, so we get

$$I_D = K_n {V_{DS}}^2 \quad \text{.....(41)}$$

5.6.3.1 MOSFET Drain Current with Drain Source Voltage with Different Gate Source Voltage.

$I_D = K_n(V_{GS} - V_T)^2$ in saturation region .....(42)

$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ in triode region .....(43)

$I_D = 0$ in cut-off region

$I_D = drain\ current$

$K_n = temperature\ mobility\ factor = 10^{-3}$

$V_{GS} = gate\ to\ source\ voltage = 4, 6, and\ 8\ volt$

$V_T = threshold\ voltage = 1.5\ volt$

$V_{DS} = drain\ to\ source\ voltage = 0\ to\ 12\ volt$

MATLAB code is given on page no. 57

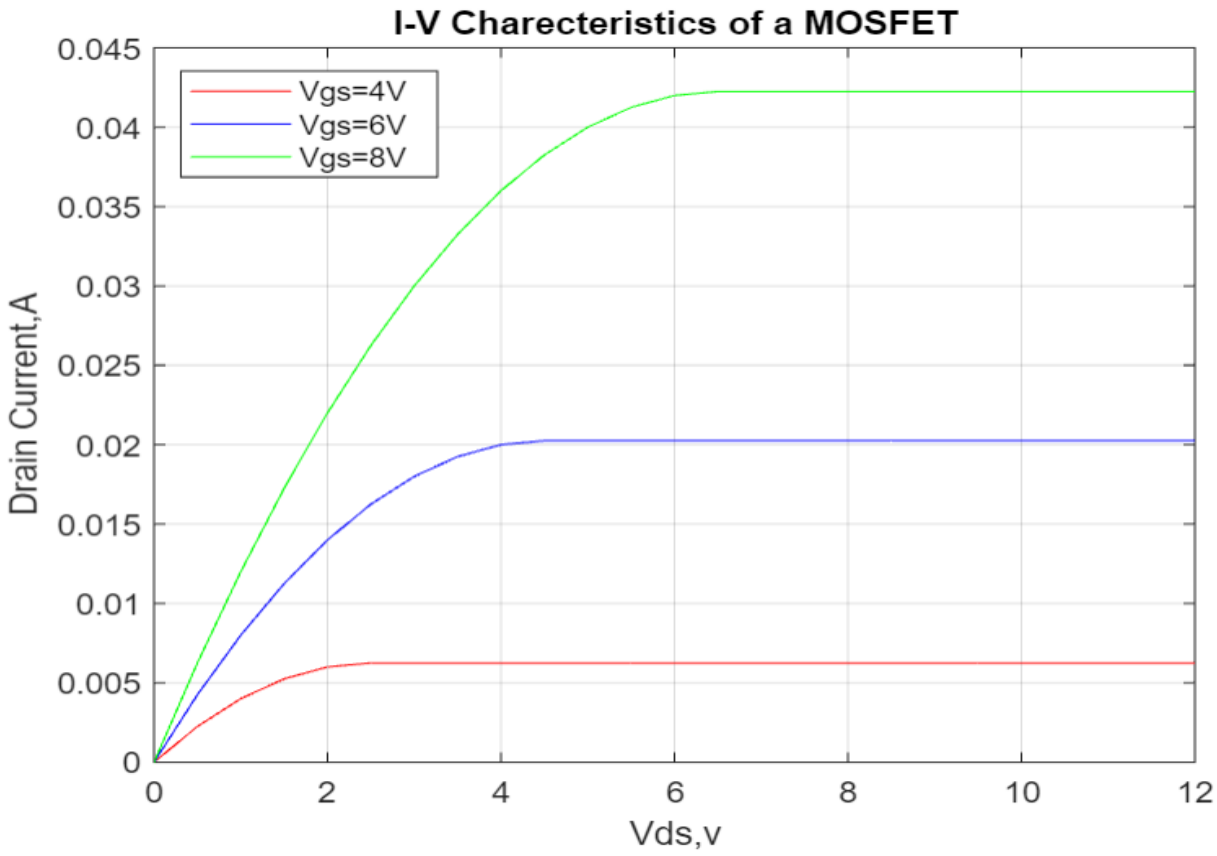


Figure: 5.5. $I_D - V_{DS}$ with different gate voltage of MOSFET

5.6.3.2 MOSFET Drain Current with Drain Source Voltage with Different Temperature.

$I_D = K_n(V_{GS} - V_T)^2$ in saturation region .....(44)

$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ in tride region .....(45)

$I_D = 0$ in cut-off region

$I_D = drain\ current$

$K_n = temperature\ mobility\ factor = \frac{\mu_n \varepsilon \varepsilon_{ox}}{2t_{ox}} \frac{W}{L}$ .....(46)

$\mu_n = surface\ mobility\ of\ electrons$ which is depend with temperature

$$\mu_n = \mu\,(T_r)\left(\frac{T}{T_r}\right)^{-k\mu}$$

$\mu\,(T_r)$=

$T_r = 300K$

$k\mu = 0.6$

$\varepsilon = permitivity\ of\ free\ space = 8.85X10^{-14}F/cm$

$\varepsilon_{ox} = dielectric\ constant$

$t_{ox} = thickness\ of\ the\ oxide$

L=length of the channel

W= width of the channel

T= 300K to 500K

$V_{GS} = gate\ to\ source\ voltage = 4\ volt$

$V_T = threshold\ voltage = 1.5\ volt$

$V_{DS} = drain\ to\ source\ voltage = 0\ to\ 12\ volt$

MATLAB code is given on page no. 58

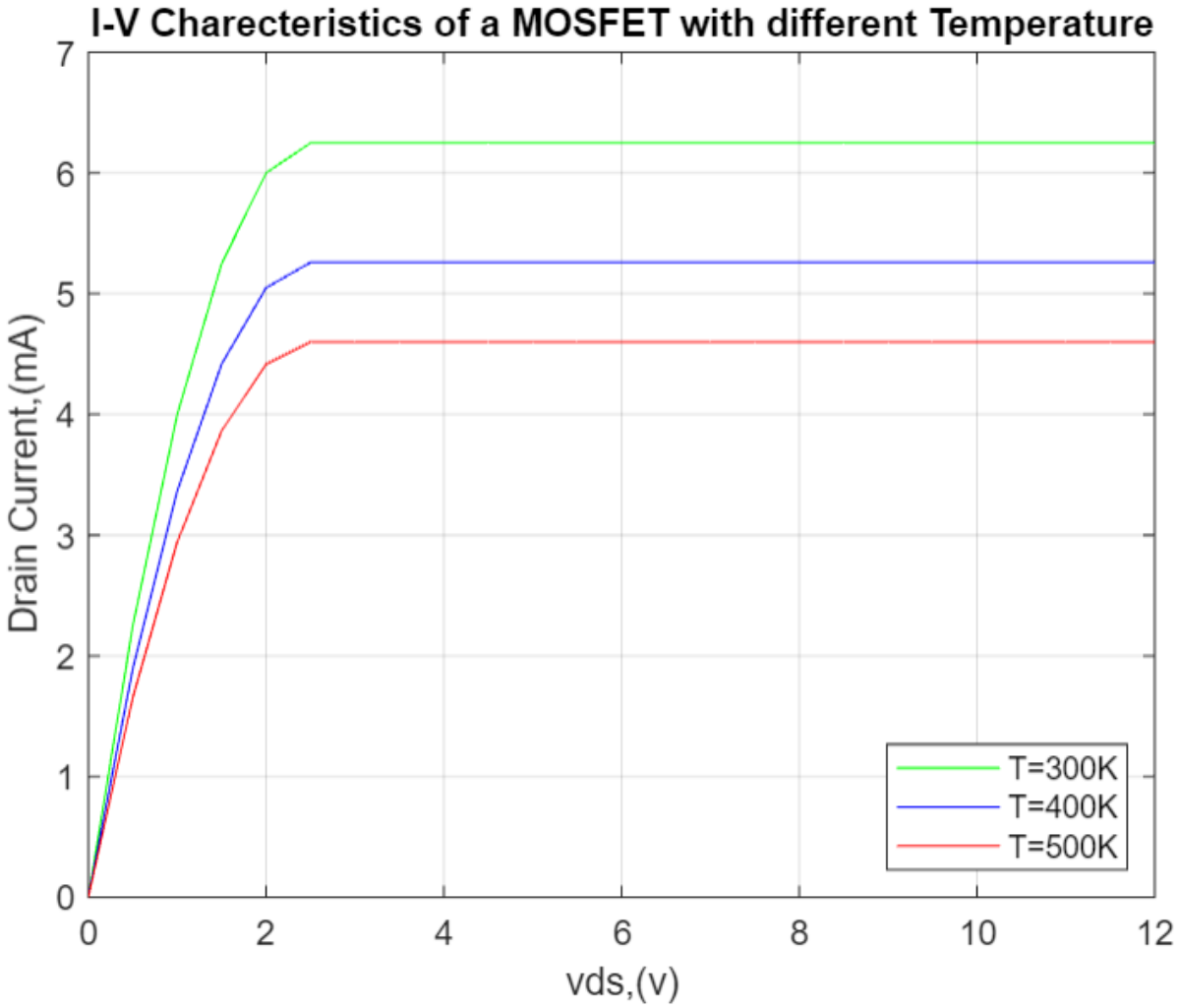


Figure: 5.6. $I_D - V_{DS}$ with different operating temperature of MOSFET

5.6.3.3 MOSFET Drain Current with Gate Source Voltage with Different Mobility.

$$I_D = 0.5 * \mu_n * C_{ox} * \frac{w}{L} * (V_{GS} - V_T)^2 \quad \text{.....(47)}$$

$I_D = drain\ current$

$$\mu_n = 300 * 10^{-4}\ ,\ m^2\ \text{/V.S}$$

$$= 500 * 10^{-4}, m^2\ \text{/V.S}$$

$$= 700 * 10^{-4}, m^2\ \text{/V.S}$$

$C_{ox} = \frac{\varepsilon\varepsilon_{ox}}{t_{ox}}$= 3.9*8.85*$10^{-3}$/2

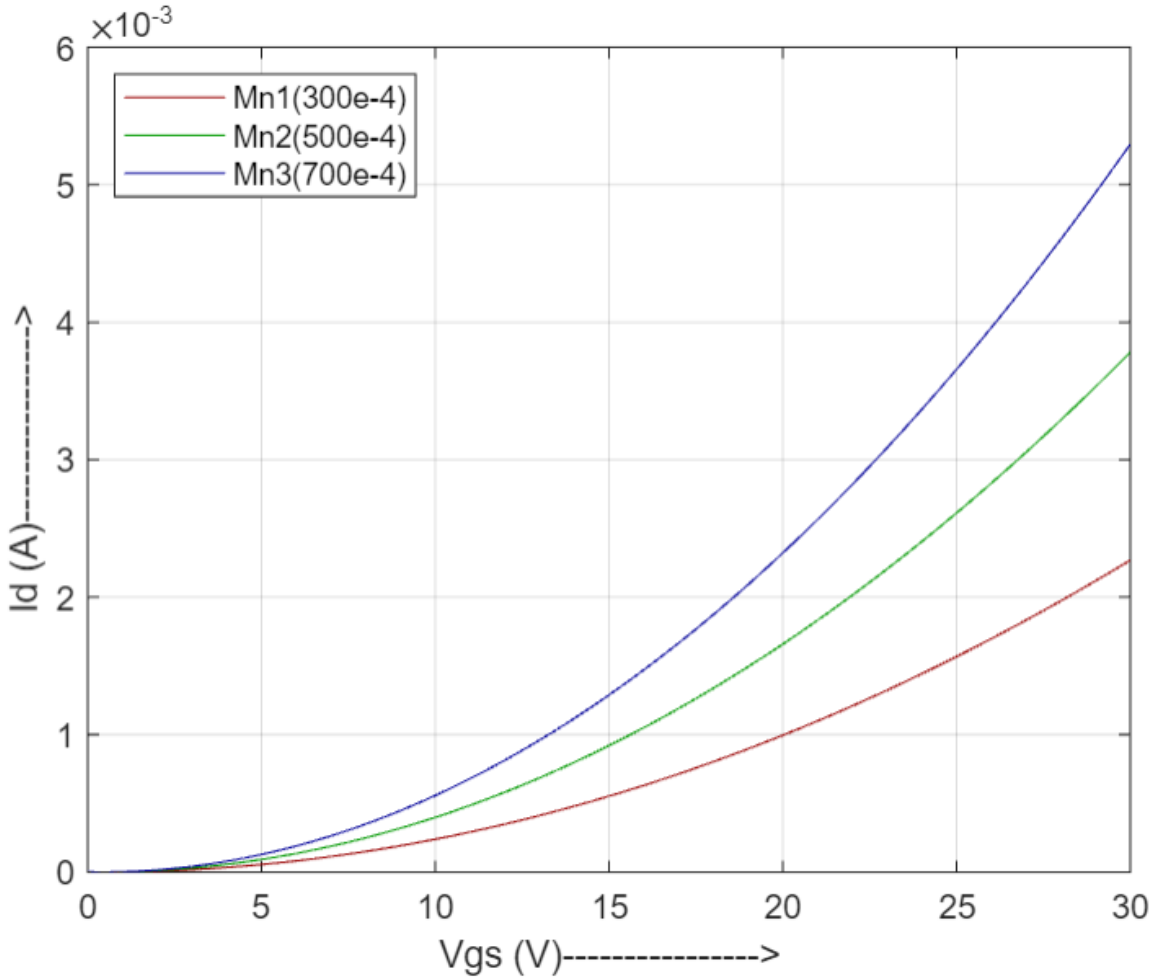
W=10^{-9}µm

L=10^{-7} µm

$V_{GS} = gate\ source\ voltage = 0\ to\ 30\ volt$

$V_T = threshold\ voltage = 0.4\ volt$

MATLAB code is given on page no. 59



5.6.3.4 Short Channel Effects of MOS Transistor.

We know that the drain current I_D -

$$I_D = \left(\frac{W}{L}\right) * \mu_n * C_d * V_T^2 * e^{\frac{V_{GS}-V_T}{\eta V_T}} * (1 - e^{-\frac{V_{DS}}{V_T}}) \quad \text{.....(48)}$$

Where $V_T = V_{t0} * \eta * V_{DS} + \gamma((\Phi_S + V_{sb})^{\frac{1}{2}} - {\Phi_S}^{1/2})$ .....(49)

$C_d = depletion\ capacitance = (q * E_{si} * \frac{N_{sub}}{4*0.65})^{1/2}$ .....(50)

$I_D = drain\ current$

$\mu_n = mobility\ of\ the\ electrons$

$C_{ox} = oxide\ capacitance$

W= width of the MOSFET=10^{-6} µm

L= channel length=10^{-8} µm

$V_{DS} = drain\ to\ source\ voltage = 5\ volt$

$V_{GS} = gate\ to\ source\ voltage$

$V_T = threshold\ voltage = 0.7\ volt$

$V_{t0} = thermal\ voltage = 0.02585\ volt$

$N_{sub} = 10^{15}$

$\eta = chain\ induced\ barrier\ lowering$ =0.8

γ=body effect factor=0.35

MATLAB code is given on page no.56

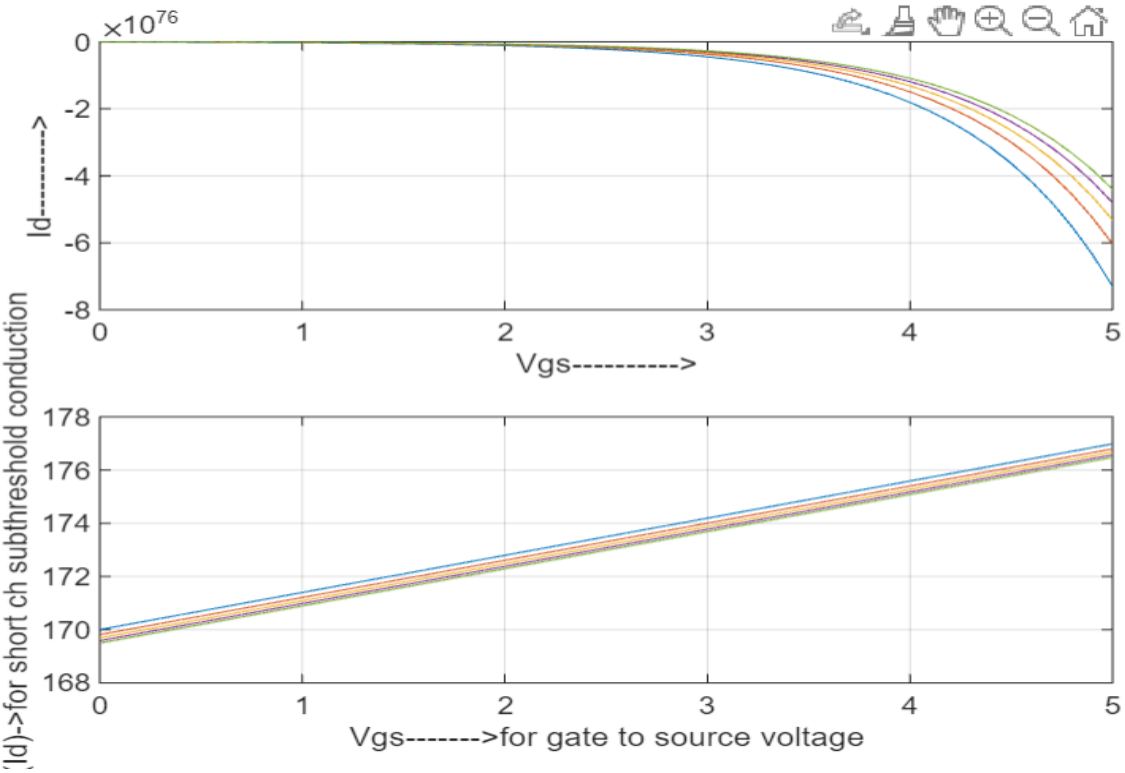


Figure: 5.8. Characteristic of short channel effect, drain current with gate voltage.

5.6.3.5 MOSFET drain current with gate source voltage with different channel length(L) and channel resistance varies with channel length .

Drain current is given by

$I_D = K_n(V_{GS} - V_T)^2$ in saturation region

$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$ in tride region

$I_D = 0$ in cut-off region

$I_D = drain\ current$

$K_n = temperature\ mobility\ factor = \frac{\mu_n \varepsilon \varepsilon_{ox}}{2t_{ox}} \frac{W}{L}$

$\mu_n = surface\ mobility\ of\ electrons$ which is depend with temperature

$\mu_n = \mu\ (T_r)\left(\frac{T}{T_r}\right)^{-k\mu}$

$\mu\ (T_r)$=

$T_r = 300K$

T= 300K

$k\mu = 0.6$

$\varepsilon = permitivity\ of\ free\ space = 8.85X10^{-14} F/cm$

$\varepsilon_{ox} = dielectric\ constant = 3.9 * 8.854 * 10^{-12}$

$t_{ox} = thickness\ of\ the\ oxide = 10^{-9}$ µm

L=length of the channel=$2 * 10^{-8}, 4 * 10^{-8}$,$6*10^{-8}$,$8*10^{-8}$, $10*10^{-8}$ µm

W= width of the channel =10^{-6} µm

T= 300K

$V_{GS} = gate\ to\ source\ voltage = 3\ volt$

$V_T = threshold\ voltage = 0.7\ volt$

$V_{DS} = drain\ to\ source\ voltage = 0\ to\ 2.5\ volt$

MATLAB code is given on page no. 55

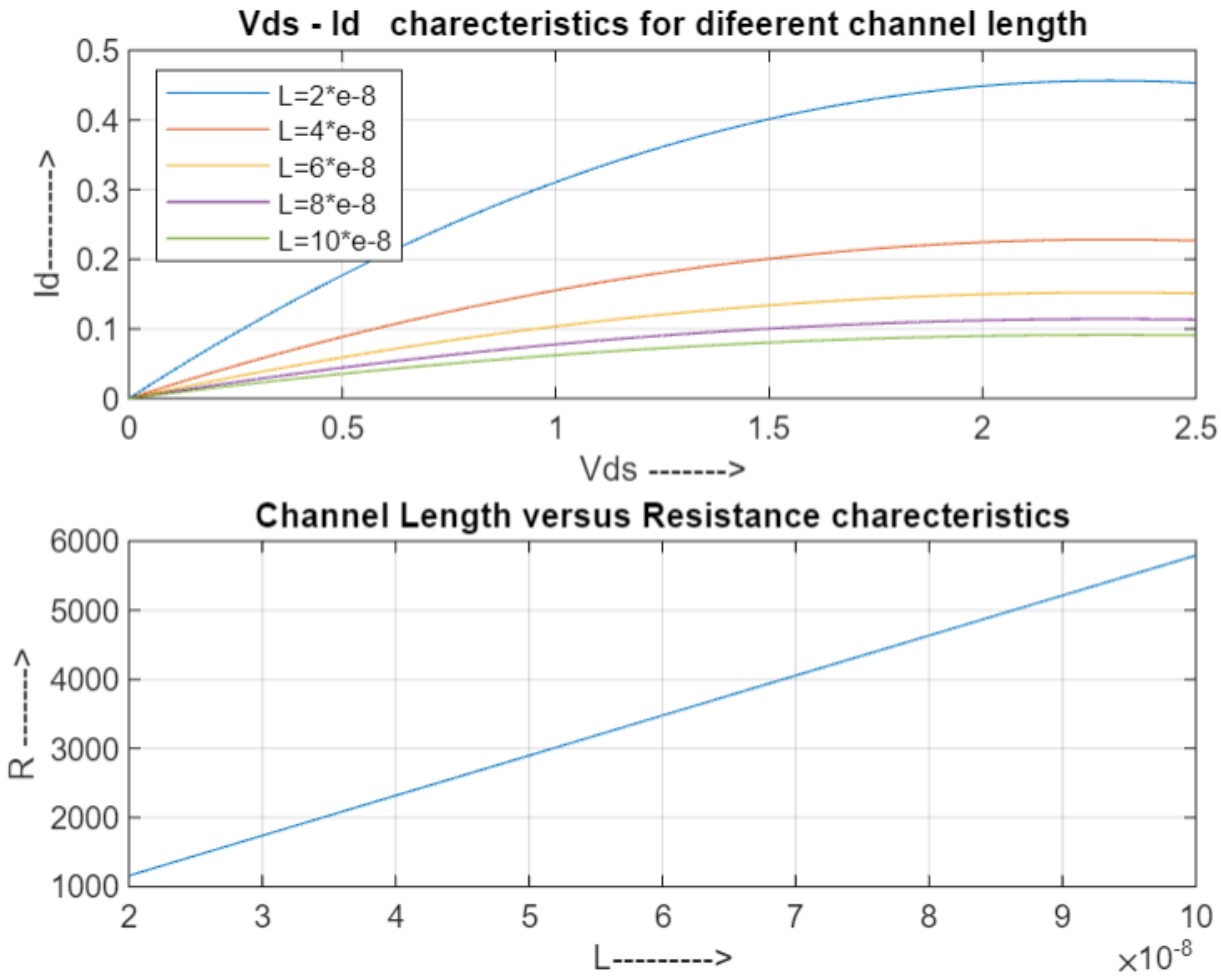


Figure: 5.9. $I_D - V_{DS}$ with different channel length and resistance with channel length characteristics.

5.7 The characteristics of mobility with doping concentration

$$\mu_n = \frac{5.1\times10^{18}+92\times n_c^{0.91}}{3.75\times10^{15}+n_c^{0.91}} \quad \text{.....(51)}$$

$$\mu_p = \frac{2.90\times10^{15}+47.7\times n_c^{0.76}}{5.86\times10^{12}+n_c^{0.76}} \quad \text{.....(52)}$$

$\mu_n = mobility\ of\ electron$ $\mu_p = mobility\ of\ hole$

$n_c = doping\ concentration$

MATLAB code is given on page no. 57

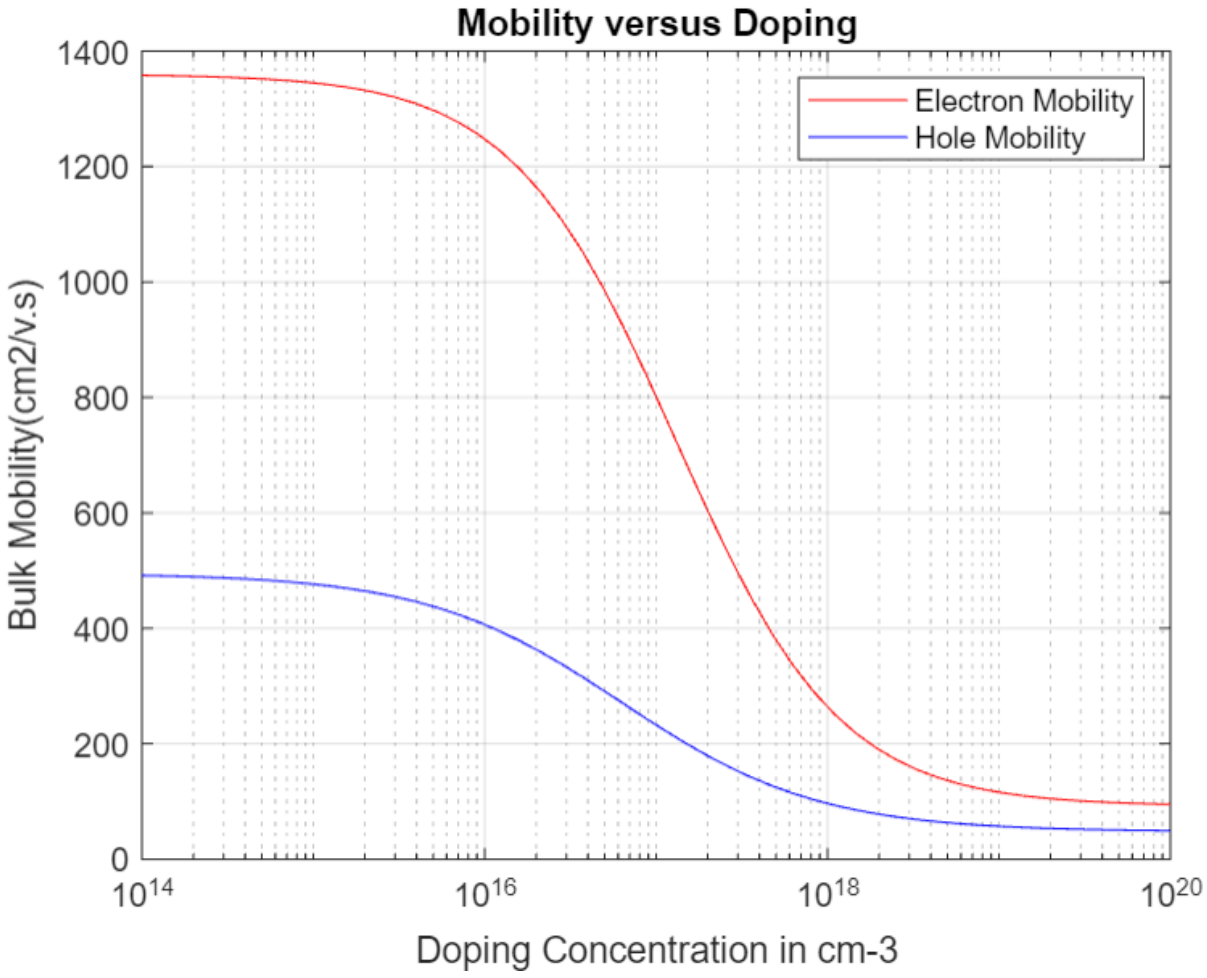


Figure: 5.10. the characteristic of bulk mobility and doping concentration

5.8 Carrier mobility varies with applied electric field

The dependence of drift velocity of electron on the applied field is the important factors of the MOSFET analysis.

For low electric field, the carrier velocity is directly proportional to the electric field.

$$V(E) \alpha E \quad \ldots\ldots(53)$$

$$V(E)=\mu_0 E \quad \ldots\ldots(54)$$

μ_0 : the mobility of electron at low electric field which is constant

When the electric field is applied the electron transfer and decrease the carrier velocity and here negative mobility creates. This decrease results in the variation of the drift velocity of the carriers is non-linier.

$$\mu=\frac{\mu_0+V_S(\frac{E^3}{E_C^4})}{1+(\frac{E}{E_C})^4} \quad \ldots\ldots(55)$$

$$V=\mu_1 E=\frac{\mu_0+V_S(\frac{E^3}{E_C^4})}{1+(\frac{E}{E_C})^4} E \quad \text{.....(56)}$$

The relation between mobility and electric field is defined by

$$\mu=\frac{V_S}{E} * tanh(\frac{E}{E_C}) \quad \text{.....(57)}$$

μ is the mobility

$E_c = 0.65 * 10^6$

$E = electric\ field\ (0\ to\ 8 * 10^5)$

$V_s = supply\ voltage$

MATLAB code is given on page no. 59

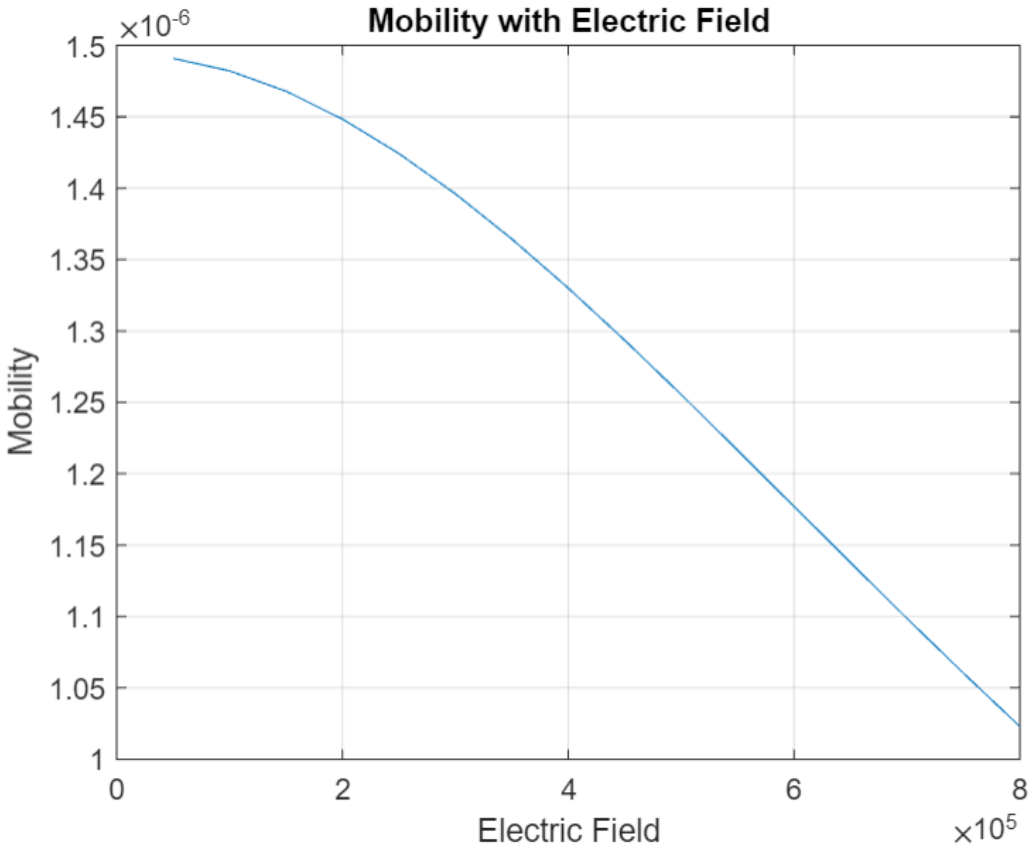


Figure: 5.11 This figure shows the Carrier mobility varies with applied electric field

Here the mobility decrease with the increase of electric field at 300K.

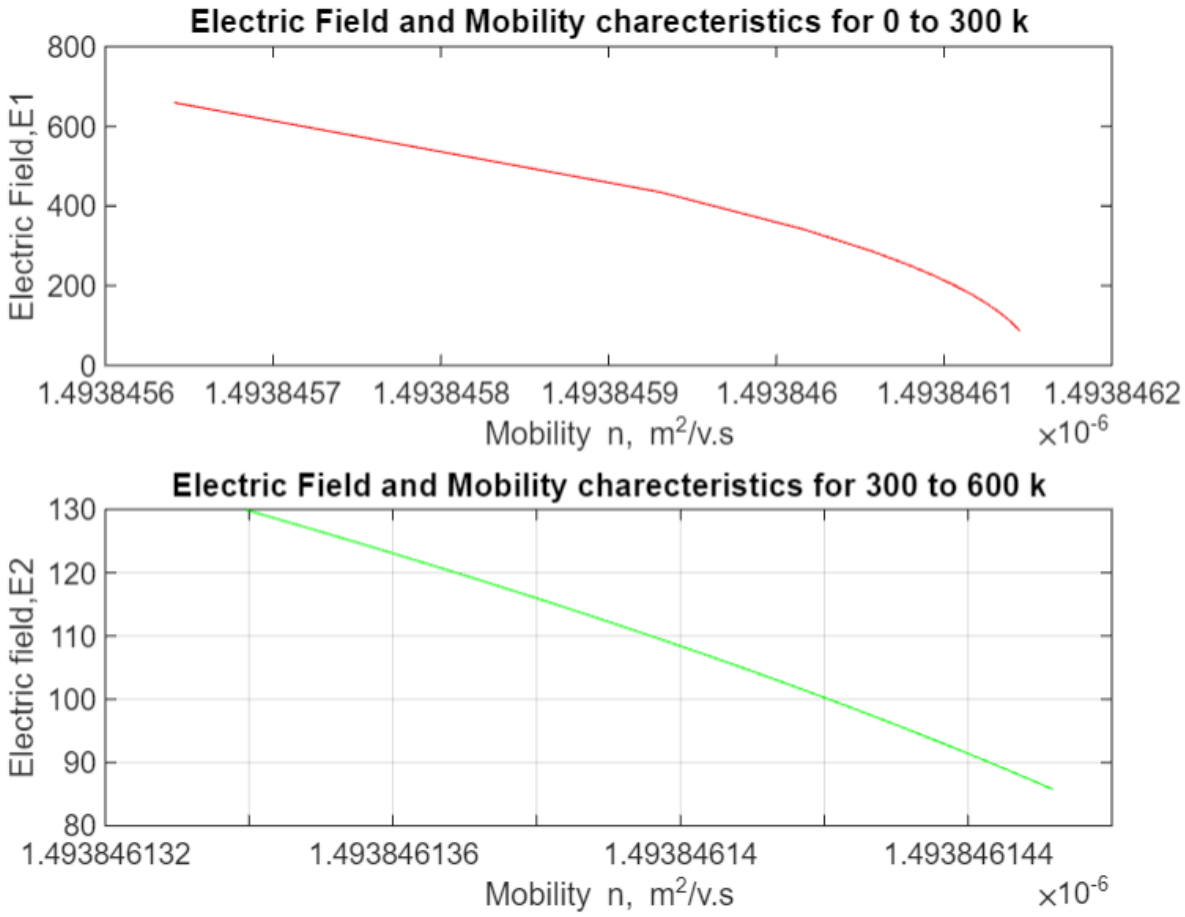


Figure 5.12: The characteristics of mobility with electric field

MATLAB code given in the page no: 60

In figure 5.12. the electric field decrease with the increase of mobility at temperature 0 – 600K.

CHAPTER 6

MATLAB CODE

1. *Study of the Mobility characteristics with temperature 0K to 600K.*

```
%Temperature and Mobility characteristics for 0 to 600 k
V=12;
T1=0:10:300;
utr=0.14; % ref. temperature(300K)=0.14 m2/v.s
n1=utr*(T1/300).^0.6;
E1=V./(n1);
subplot(2,1,1);
plot(T1,n1,'r');
xlabel('Temperature,k');
ylabel('Mobility n, m^2/v.s');
title('Temperature and Mobility charecteristics for 0 to 300 k');
%end;
T2=300:10:600;
utr=0.14; %ref. temperature(300K)=0.14 m2/v.s
n2=utr*(T2/300).^-0.6;
E2=V./(n2);
subplot(2,1,2);
plot(T2,n2,'g');
xlabel('Temperature,k');
ylabel('Mobility n, m^2/v.s');
title('Temperature and Mobility charecteristics for 300 to 600 k');
%end;
grid on;
```

where,

V	Applied voltage
T1	0K to 300K tempareture
T2	300K to 600K tempareture
utr	Reference mobility at 300K
n1	Mobility at T1 tempareture
n2	Mobility at T2 tempareture

2. *Study of the drain-source resistance with the change of temperature*

```
      % Temperature - Sheet Resistance charectaristicc
clc;
clear all;
T=[0:10:600]; % T is the absolute temperaature
Rds=920-(4/3)*(T-300); % Rds is the total drain and source contact
region resistance
plot(T,Rds,'r')
xlabel('Temperature,/k');
ylabel('Sheet resistance Rds, ohms');
title('Temperature - Sheet Resistance charectaristicc');
grid;
hold on;

where,
T     Tempareture varies with 0K to 600K
Rds   Total Drain and Source contact resistance at high tempareture
```

3. *To study the relation or dependence of leakage current with operating temperature*

```
      %Temperature vs Leakage current
clc;
clear;
close all;
T=[300:5:400];
vt=0.02585; %vt is the thermal voltage%
cox=3.45*10^-18;
w=100*10^-8;
L=4*10^-9;
vgs=2;
n=1;
vds=5;
Tr=300;
    m=0.14*(T/Tr).^0.6; %m for mobility%
B=m*cox*w/L;
Idso=B*(vt^2)*exp(1.8);
Ids=Idso*exp((vgs-vt)/n*vt)*(1-exp(-vds/vt));
plot(T,Ids,'r');
xlabel('Temperature----->k');
ylabel('Leakage current-----mA');
title('The charteceristics of Temperature and Leakage current')
grid;
hold on;
```

Where,

Vt	Threshold voltage
Cox	Oxide capacitance
W	Width of the device
L	Length of the device
Vgs	Gate voltage
Vds	Drain voltage
T	Operating tempareture in kelvin
Tr	Referance tempareture
m	Mobility

4. *To study of the potential at a point of the channel on the variation of the charge*

```
%Variation of the charge in the dipletion region with voltage
at any point of the channel
clc;
clear all;
close all;
Qd=[0:10^-9:5*10^-9];
Vgs=2;
Vt=0.7; %thermal voltage
W=10^(-6); % width of the channel
Cox=(3.9*8.854*10^(-12))/(2*10^(-9));
for i=1:length(Qd)
Vx(i)=((Vgs-Vt)-(Qd(i)/(W*Cox)));
end
subplot(2,1,1);
plot(Qd,Vx);
grid;
xlabel('Qd (C)------->');
ylabel('V(x)(V)--------->');
subplot(2,1,2);
plot(Vx,Qd);
grid on;
xlabel('Vx------>');
ylabel('Qd------>');
```

5. *To study the Drain characteristics and channel resistance*

```
% Drain source voltage and Drain current Charecteristics and
L-R Charecteristics
clc;
clear all;
close all;
Vds=[0:0.05:2.5];
Vt=0.7;
Vgs=3;
Mn=1000*10^(-4);
Eox=3.9*8.854*10^(-12);
tox=10^(-9);
Cox=Eox/tox;
L=[2*10^(-8):2*10^(-8):10*10^(-8)];
W=10^-6;
subplot(2,1,1);
for j=1:length(L)
for i=1:length(Vds)
Id(i)=(Mn*Cox*W*(((Vgs-Vt)*Vds(i))-(Vds(i)^(2)/2))/L(j));
end
plot(Vds,Id);
xlabel('Vds ------->');
ylabel('Id--------->');
title('Vds - Id   charecteristics for difeerent channel length')
legend('L=2*e-8','L=4*e-8','L=6*e-8','L=8*e-8','L=10*e-
8','location','northwest')
grid;
hold on;
end
for m=1:length(L)
Vds=2.3
Id1(m)=(Mn*Cox*W*(((Vgs-Vt)*Vds)-(Vds^(2)/2))/L(m));
Vds=2.29
Id2(m)=(Mn*Cox*W*(((Vgs-Vt)*Vds)-(Vds^(2)/2))/L(m));
end
for k=1:length(L)
R(k)=0.01/(Id1(k)-Id2(k));
end
subplot(2,1,2);
plot(L,R);
xlabel('L--------->');
ylabel('R ------->');
title('Channel Length versus Resistance charecteristics')
grid;
hold on;
```

6. ***To study the gate source voltage and drain current for short channel effect***

%Gate -source voltage Vgs vs Id and Vgs vs log Id for short channel subthreshold conduction (Short channel effect).

```
clc;
clear all;
close all;
VT=.02585;
Vto=.7;
Esi=3.9*8.854*10^-12; %Permitivity of Silicon
q=1.6*10^-19;         %Charge of electron
Nsub=10^15;
cd=sqrt(q*Esi*Nsub/(4*.65));
Y=.35;
w=10^-6;
l=10^-8;
n=.08;
u=.05;
Qs=.2;
cox=Esi/(2*10^-2);
N=1+(cd/cox);
vds=5;
vsb=[0:.5:2];
vgs=[0:.1:5];
for i=1:length(vsb)
for j=1:length(vgs)
vt=(Vto*n*vds) + Y*(sqrt(vsb(i)+Qs)+sqrt(Qs));
Id(j)=(w/l)*u*cd*(VT)^2*(exp((vgs(j)-vt)/(N*VT)))*(1-exp((vds)/VT));
end
subplot(2,1,1)
plot(vgs,Id);
xlabel('Vgs---------->');
ylabel('Id---------->');
grid
hold on;
subplot(2,1,2)
plot(vgs,log(Id));grid
hold on;
end
ylabel('log(Id)->for short ch subthreshold conduction' );
xlabel('Vgs------->for gate to source voltage' );
grid
hold on;
```

7. *Study the mobility characteristic with doping concentration*

```
% Mobility vs doping Concentration%
clc;
clear all;
close all;
nc=logspace(14,20); % doping concentration
un=(5.1e18+92*nc.^0.91)./(3.75e15+nc.^0.91);
up=(2.90e15+47.7*nc.^0.76)./(5.86e12+nc.^0.76);
semilogx(nc,un,'r',nc,up,'b')
xlabel('Doping Concentration in cm-3')
ylabel('Bulk Mobility(cm2/v.s)')
title('Mobility versus Doping')
legend('Electron Mobility','Hole Mobility','location','northeast')
grid on;
```

8. *To study the I-V Characteristic of MOSFET*

```
% I-V charecteristics of MOSFET
clc;
clear all;
close all;
kn=1e-3;
vth=1.5;
vds=0:0.5:12;
vgs=4:2:8;
m=length(vds);
n=length(vgs);
for i=1:n
    for j=1:m
        if vgs(i)<vth
            curr(i,j)=0;
        elseif vds(j)>=(vgs(i)-vth)
            curr(i,j)=kn*(vgs(i)-vth)^2;
        elseif vds(j)<(vgs(i)-vth)
            curr(i,j)=kn*(2*(vgs(i)-vth)*vds(j)-vds(j)^2);
        end
    end
end
plot(vds,curr(1,:),'r',vds,curr(2,:),'b',vds,curr(3,:),'g');
xlabel('Vds,v');
ylabel('Drain Current,A');
title('I-V Charecteristics of a MOSFET');
legend('Vgs=4V','Vgs=6V','Vgs=8V','location','northwest')
%{
text(6, 0.009,'vgs=4v');
text(6, 0.023,'vgs=6v');
```

```
text(6, 0.045,'vgs=8v');
%}
grid on;
hold on;
```

9. *To study the I-V Characteristic of MOSFET with different temperature*

```
% 'I-V Charecteristics of a MOSFET' of different temperature
clc;
clear all;
close all;
%kn=1e-3;
vt=1.5;
vds=0:0.5:12;
vgs=4;
T=300:100:500;
m=length(vds);
n=length(T);
for i=1:n
    kn=(T(i)/300).^-0.6;
    for j=1:m
        if vgs<vt
            curr(i,j)=0;
        elseif vds(j)>=(vgs-vt)
            curr(i,j)=kn*(vgs-vt)^2;
        elseif vds(j)<(vgs-vt)
            curr(i,j)=kn*(2*(vgs-vt)*vds(j)-vds(j).^2);
        end
    end
end
plot(vds,curr(1,:),'g',vds,curr(2,:),'b',vds,curr(3,:),'r');
%grid on;
xlabel('vds,(v)');
ylabel('Drain Current,(mA)');
title('I-V Charecteristics of a MOSFET with different Temperature');
%text(6, 4.5,'T=500k');
%text(6, 5,'T=400K');
%text(6, 6,'T=300');
grid;
hold on;
legend('T=300K','T=400K','T=500K','location','southeast')
```

10. Characteristics of Id-Vgs with different mobility

```
% Gate-Source Voltage Vs Drain Current with different mobility
clc;
clear all;
close all;
Vgs=[0:0.5:30];
Vt=.4;
Mn1=300*(10^(-4));
Mn2=500*(10^(-4));
Mn3=700*(10^(-4));
Cox=((3.9*8.854*(10^(-3)))/2);
W=10^(-9);
L=(10^(-7))
for i=1:length(Vgs)
    Id1(i)=(0.5*Mn1*Cox*W*((Vgs(i)-Vt)^2)/L);
    Id2(i)=(0.5*Mn2*Cox*W*((Vgs(i)-Vt)^2)/L);
    Id3(i)=(0.5*Mn3*Cox*W*((Vgs(i)-Vt)^2)/L);
end
plot(Vgs,Id1,'Color',[.6 0 0]);grid;
hold on;
plot(Vgs,Id2,'Color',[0 .6 0]);grid;
hold on;
plot(Vgs,Id3,'Color',[0 0 .6]);grid;
hold on
xlabel ('Vgs (V)----------------->');
ylabel ('Id (A)----------------->');
legend('Mn1(300e-4)','Mn2(500e-4)','Mn3(700e-
4)','Location','northwest')
```

11. To study the carrier mobility varies with applied electric field at 300K

```
% carrier Mobility for MOSFET varies with Applied Electric field

u0=.374;
vs=.971;
Ec=0.65e6;
E=0e5:0.5e5:8e5;
u1=(vs./E).*tanh(E./Ec);

plot(E,u1);

xlabel('Electric Field');
ylabel('Mobility');
title('Mobility with Electric Field');
grid on
```

12. To study the carrier mobility varies with applied electric field and temperature

```
% Electric field varies with mobility with the change of Temperature 0K to 600K on
the MOSFET
%Electric Field and Mobility charecteristics for 0 to 600 k
V=12;
T1=0:10:300;
utr=0.14; %mobility at ref. temperature(300K)=0.14 m2/v.s
Mn1=utr*(T1/300).^0.6;
E1=V./(Mn1);
u0=.374;
vs=.971;
Ec=0.65e6;
%E=0e5:0.5e5:8e5;
u1=(vs./E1).*tanh(E1./Ec);
subplot(2,1,1);
plot(u1,E1,'r');
ylabel('Electric Field,E1');
xlabel('Mobility n, m^2/v.s');
title('Electric Field and Mobility charecteristics for 0 to 300 k');
%end;
T2=300:10:600;
utr=0.14; %mobility at ref. temperature(300K)=0.14 m2/v.s
Mn2=utr*(T2/300).^-0.6;
E2=V./(Mn2);
u0=.374;
vs=.971;
Ec=0.65e6;
%E=0e5:0.5e5:8e5;
u1=(vs./E2).*tanh(E2./Ec);
subplot(2,1,2);
plot(u2,E2,'g');
ylabel('Electric field,E2');
xlabel('Mobility n, m^2/v.s');
title('Electric Field and Mobility charecteristics for 300 to 600 k');
%end;
grid on;
```

CHAPTER 7

CONCLUSION AND FUTURE WORK

In this chapter we provide conclusion and future scope of work

7.1 CONCLUSION

An analytical model [*Effects of temperature variation (0–300 K) and (300–600 K) in MOSFET modeling in 6H–silicon carbide Md. Hasanuzzaman a,*, Syed K. Islam a,b, Leon M. Tolbert a,b]* to study and explain the behavior of the MOSFET output characteristics at different temperatures. The model has been evaluated for 6H–SiC material system. It includes the change in the threshold voltages, carrier mobility, the body leakage current, and the drain and source contact resistances. The MOSFET output characteristics and parameter values are compared with standard data. There is a good agreement between the model outputs and the experimental data. The model can be used to predict the characteristics of MOSFET parameters with change of temperature.

Here temperature dependence is found out and their diverse effects are analyzed. The negative temperature dependence found that the Threshold voltage, subthreshold leakage current, and source to drain on resistance increases with temperature. The change in the operating temperature of a device will affect its characteristics and therefore circuit performance.

Temperature dependent parameters on MOSFET's DC characteristics will effects are also analyzed by plotting with MATLAB.

The study of these temperature effects play recreates a major role in designing a grade IC's.

Table:7: Parameter comparison table.

Parameter 1	Parameter 2	Parameter 3
Vd increase	Id increase	With increase of Temperature
T increase	Mobility increase	T= 0-300K
T increase	Mobility decrease	T= 300-600K

T increase	R decrease	T= 0-600K
T increase	Idso (leakage current) increase	T increase
Vgs increase	Id increase	With different mobility
Vds increase	Id increase	With different channel length
Channel length increase	Resistance increase	
Doping concentration Nd increase	Mobility increase	
Electric field increase	Mobility decrease	
Mobility increase	Electric field decrease	With T

In the above table if the parameter 1 changes then parameter 2 changes with the change of parameter 3. As a result, a thermal runaway creates and the device burn-out.

7.2 FUTURE WORK

An IC does not always work under the room temperature. Some effects are not conspicuous in room temperature. Have conflicting effect in higher temperature ranges. Temperature analysis done in dependability conviction can be used for performance enhancement. Now a day the pre analysis and post analysis of temperature dependent MOSFET parameters are essential for the device used in higher temperature application.

We can reduce the self-heating effect in future work.

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