Threshold Voltage Variation in TG JLFET and Cylindrical JLFET due to Random Dopant Fluctuation

This thesis is submitted for the partial fulfilment of the requirement for the Degree of **Masters of Engineering (M.E)** in the **Department of Electronics and Tele-Communication Engineering (ETCE)** under the Specialization of **Electron Devices**.

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CERTIFICATE

This is to certify that the thesis entitled, **"Threshold Voltage Variation in TG JLFET and Cylindrical JLFET due to Random Dopant Fluctuation"** submitted by **Abhishek Paul** (Roll No.: **002010702007**) of Jadavpur University, Kolkata is a record of legitimate research conducted under my supervision and guidance that may be accepted in partial completion of the requirements for the Master of Engineering in Electronics and Tele-communication Engineering with a specialisation in Electron Devices from the Institute. Any other paper submitted for the award of a degree to any other University or Institute does not include the research results reported in this thesis.

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ABSTRACT

With advancement in recent VLSI technology, there is an increase in complexity of the circuits. To cope up with this complexity and also to reduce the chip size at the same time, we need to scale the MOSFET devices to deep sub-micron levels. However, traditional MOS transistors comprising of juctions cannot combat the SCEs without degrading the device performance. As a result, to withstand this aggressive scaling without reducing performance, junctionless transistors(JLTs) were developed.

In this thesis, different models of JLTs were proposed and their performance especially due to RDF effect were measured especially under short channel length. The variation of threshold voltage (V_{th}) is used as the parameter for analyzing the effectiveness of these junctionless structures to operate properly when the channel length of thse devices are significantly reduced and all the results were plotted as well as compared using MATLAB simulator.

It was quite evident from the plots, that the cylindrical JLFET (GAAFET) performs better TG-JLFET (FinFET) because of its structural advantge over FnFET. It is because in a GAAFET the gate is wrapped around the channel from all the sides and, whereas in a FinFET the gate covers only three sides of the channel. So GAAFET provides better electrostatic over the channel compare to a FinFET thereby improving performance. The effect of quantum confinement of carriers was also considered for both the devices when the channel was reduced to a very small size from all dimensions. It was also shown in the plots that how the V_{th} variation increases as a result of this effect.

LIST OF ABBREVIATIONS:

Abbreviation	Meaning
FET	Field Effect Transistor
JLT	Junctionless Transistor
JLFET	Junctionless Field Effect Transistor
GAA	Gate All Around
SOI	Silicon on Insulator
SCE	Short Channel Effect
DG	Double Gate
JAM	Junction Accumulation Mode
TG	Tri Gate
QSE	Quantum Size Effect
RDF	Random Dopant Fluctuation
DIBL	Drain Induced Barrier Lowering
IM	Inversion Mode

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CHAPTER 1

INTRODUCTION

All present transistors contain semiconductor junctions, which are doped with opposite polarity on either side of the junctions and are the essential building blocks of modern electronic devices. The p–n junction, which is created by the contact of a p-type piece of silicon doped with impurities to create an excess of holes and an n-type piece of silicon doped to create an excess of electrons, is the most fundamental type of junction. The two other different kinds of junctions includes a hetero junction, which is simply a p–n junction containing two distinct semiconductors, and the Schottky junction between metal and semiconductor. Both the BJT (bipolar junction transistor) as well as the MOSFET (metal oxide–semiconductor field-effect transistor) have two p–n junctions present in their structures. The MESFET (metal– semiconductor field-effect transistor) on the other hand possess Schottky junction, while the JFET (junction field-effect transistor) has common p–n junction. From all of the above transistors models, Integrated circuits(ICs) rely basically on MOSFET.

The ability to fit hundreds of millions of transistors on a single chip has been enabled by shrinking the transistor’s dimensions below 90 nm. Consumers as well as the semiconductor device manufacturers have been benefited from the greater functionality and lower cost of a wide range of integrated circuits and systems. Low manufacturing costs, faster data transfer speeds, computer processing power, and the ability to do several jobs simultaneously are only a few of the significant benefits acquired as a result of transistor scaling. The microelectronic industry has reaped huge benefits from MOSFET size shrinking during the last three decades.

Now apart from the benefits of MOSFET scaling, it also comes with several other adverse short channel effects. One of the most important disadvantage of MOSFET scaling is RDF which leads to threshold voltage variation resulting in unequal gate voltage requirement of two identical transistor on the same die. The present thesis, illustrates how this random dopant fluctuation effect influences the threshold voltage of different devices and how such influence can be minimized to a desired level.

CHAPTER 2

BACKGROUND & LITERATURE REVIEW

As technology advances, MOSFETs undergo continuous downscaling, the trend of which came into existence due to the prediction of Gordon Moore, co-founder of INTEL Corporation. It became the main industry driver and is called *Moore's Law*.

2.1 MOORE'S LAW:

Moore's law states that transistors are doubled every year. As a result, the number of transistors on the most complicated chips is limited by this law. This rate has been retained through 2007, according to recent patterns. As microchip and electronics makers fought to build faster, smaller, and cheaper electronic devices, the law became self-fulfilling; by the early twenty-first century, the number of transistors on a standard memory chip had surpassed one billion. It is widely acknowledged that scientific advances in downsizing and microelectronics have advanced to the point where circuits are only a few atoms wide, making further reductions practically impossible. It is becoming extremely difficult to manufacture high-quality junctions as transistors are getting smaller. It is very difficult to alter a material's doping concentration at distances of less than 10 nm. As a result, junctionless transistors may be able to assist chipmakers in continuing to develop smaller and smaller devices.

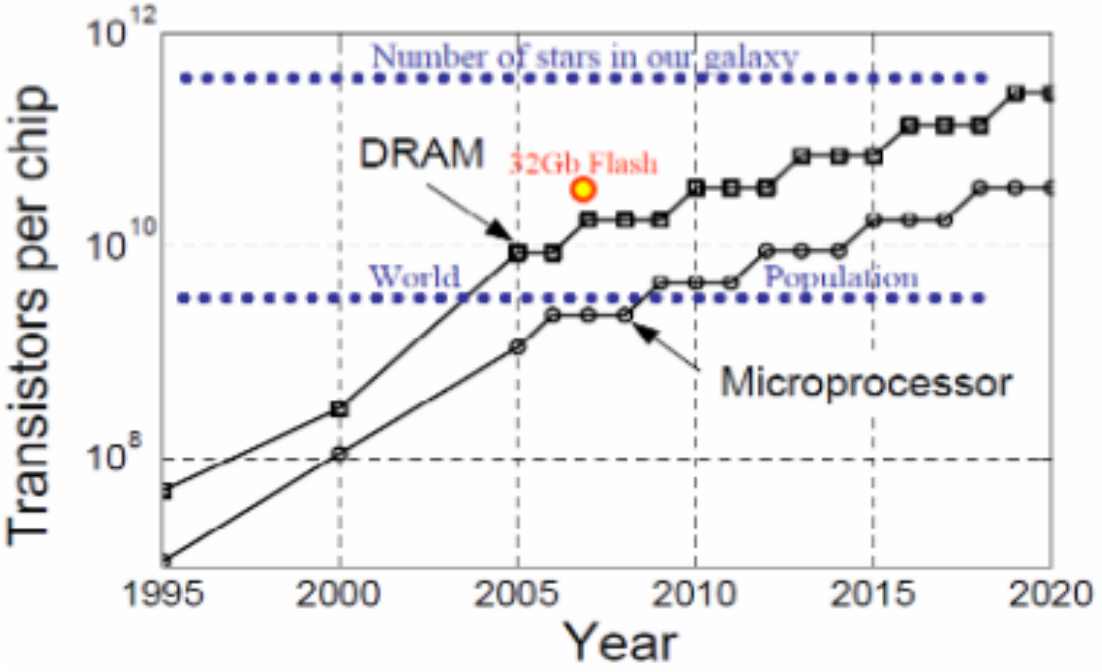


Figure 2.1. Evolution of Moore's Law over the years.

Since the initial edition of the roadmap in the early 1990s, Moore's law and the International Technology Roadmap for Semiconductors (ITRS) have been complementing each other. Moore's law predicted the transistor count that could be integrated onto a microchip over the following ten years (1965-1975), but the pattern stayed virtually unchanged for the next three decades. On the other hand, the ITRS provides a thorough handbook that enables the semiconductor industry to put this observation into practice. The ITRS issued the first white paper in 2005, in which the names "More than Moore" (MtM) and "More Moore" (MM) were first used.

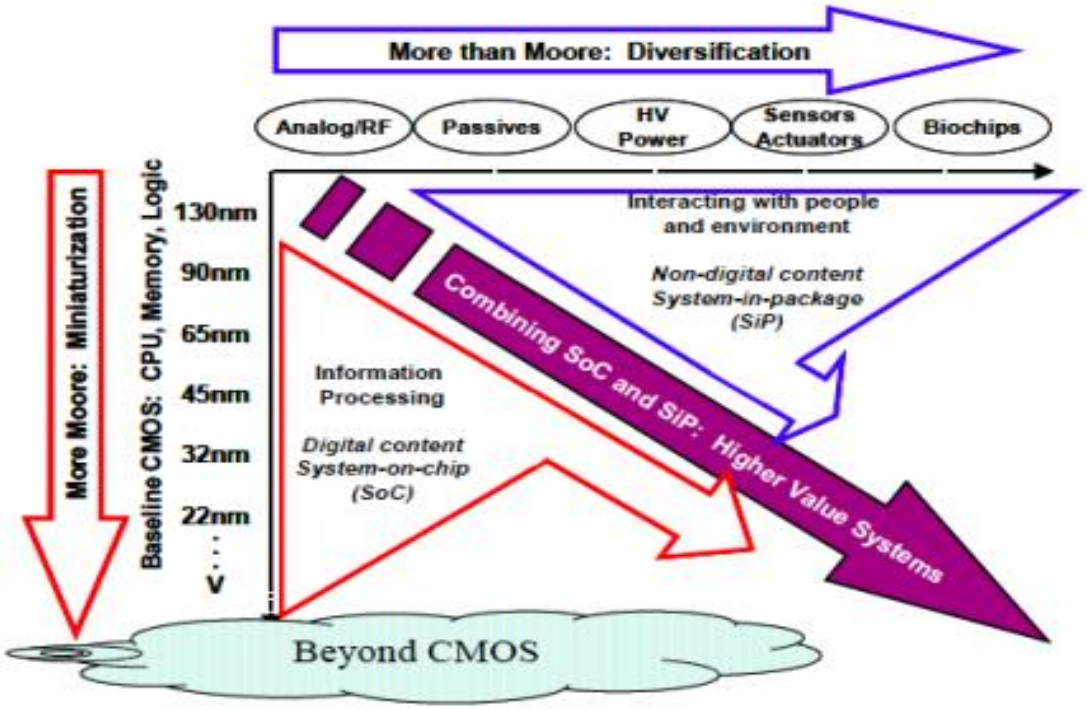


Figure 2.2. Implementation of More than Moore's Law.

2.1.1 HISTORY OF MOORE'S LAW:

While working at Fairchild Semiconductor, Moore first published the observations that would become known as Moore's law in a 1965 editorial for Electronics Magazine. Carver Mead, a professor at the California Institute of Technology (Caltech) in Pasadena, California, created the name "Moore's law" about 1975, according to the Computer History Museum in Mountain View, California. At Caltech, Mead is presently the Gordon and Betty Moore Professor Emeritus of Engineering and Applied Science. Professor Mead has been a Caltech professor for more than 40 years. His early work cleared the door for enhanced semiconductor designs that took use of Moore's law's predictions.

2.1.2 BENEFITS OF MOORE'S LAW:

The complexity of semiconductor process technologies has always risen. Moore's law is fueled by this phenomenon, which is known as the "innovation engine." The rise in complexity has been accelerated in recent years. Transistors have evolved into three-dimensional devices with unusual properties. Advanced process technologies appropriate for incredibly small feature sizes necessitate numerous exposures (multi-patterning) to precisely recreate these features on a silicon wafer. The design process has become significantly more complicated as a result of this.

Moore's law has delayed as a result of all this intricacy. Moving to a new process node is still an option, but due to its tremendous complexity and cost, migration has stalled. Furthermore, each new manufacturing node currently produces less significant density, performance, and power reduction results. The exponential benefits of Moore's law are being slowed as semiconductor process technology evolves to molecular limits.

2.1.3 IS MOORE'S LAW PRESENTLY DEAD?

Moore's law has slowed, prompting many to wonder, "Is Moore's law dead?" This does not, in fact, happen. While Moore's law continues to offer exponential gains, they are occurring at a slower rate. However, the rate of technological advancement is not slowing. Rather, the development of hyperconnectivity, big data, and artificial intelligence applications has accelerated innovation and raised the demand for "Moore's law-style" technology breakthroughs.

Moore's law and the semiconductor industry's exponential technology growth were driven for many years by scale complexity. As the ability to scale a single chip decreases, the industry must find new ways to keep growing exponentially.

Systemic complexity is driving this new design trend. Some features of this new design approach have been labeled "more than Moore." This term primarily refers to 2.5D and 3D integration methods.

However, the overall landscape is far larger and has greater potential for effect. Aart de Geus, chairman and co-CEO of Synopsys, gave a keynote talk at the 2021 SNUG World meeting of Synopsys Users Group members from around the world. Moore's law is now merging with new breakthroughs that utilize systemic complexity, according to de Geus' presentation. As a shorthand for this new design paradigm, he invented the word SysMoore. For the foreseeable future, the SysMoore era will fuel semiconductor innovation. It brings with it a slew of design issues that must be addressed.

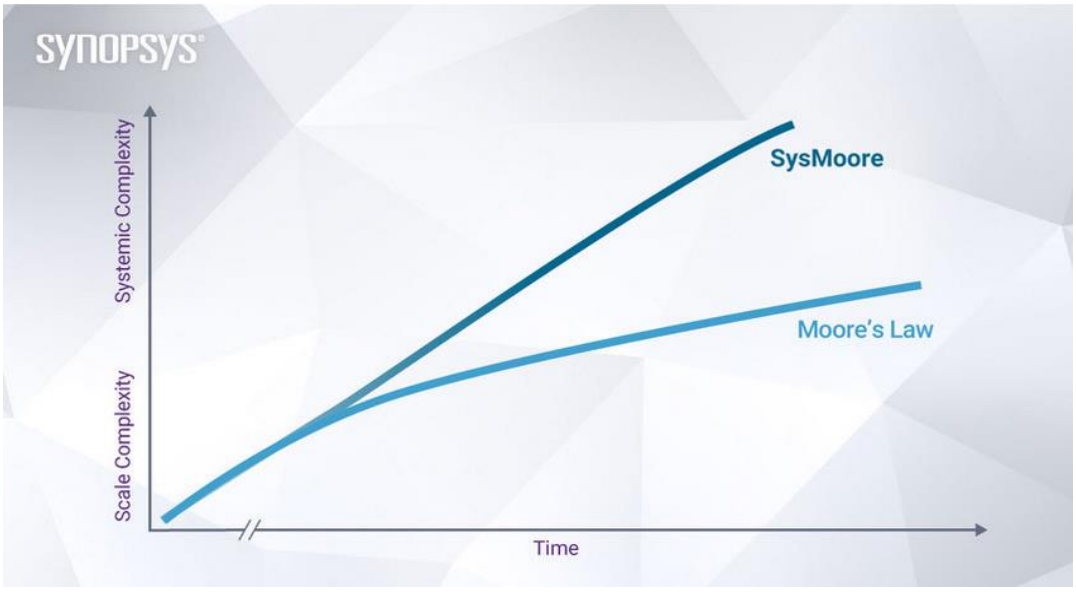


Figure 2.3. With an increase is circuit complexity Moore's Law is modified to SysMoore.

2.2 SHORT CHANNEL EFFECTS:

Short-channel effects are a set of phenomena that occur as the MOSFET's channel length approaches that of the space charge regions of the source and drain junctions with the substrate. Polysilicon gate depletion effect, threshold voltage roll-off, drain-induced barrier lowering (DIBL), velocity saturation, reverse leakage current rise, mobility degradation, hot carrier effects, and other annoyances are only a few of the problems they cause. The reduced threshold voltage makes it difficult to totally switch off the transistor. Electrostatic coupling between the source and drain causes the gate to become inefficient due to the DIBL effect. The current drive is reduced by velocity saturation. The power dissipation is increased by the leakage current. Increased surface scattering reduces charge carrier mobility, lowering output current. Aside from these issues, impact ionization and hot carrier effects degrade MOSFET performance and lead the device to behave differently than long-channel devices. The utilization of high-dielectrics, strain engineering, and other notable solutions include the reduction in gate oxide thickness. Nonetheless, the aforementioned phenomena significantly reduce the performance of planar CMOS transistors at process nodes below 90 nm.

2.3 RANDOM DOPANT FLUCTUATION:

Random dopant fluctuation (RDF) is a type of process variation caused by changes in the concentration of implanted impurities. RDF in the channel region of MOSFET transistors can change the transistor's characteristics, particularly the threshold voltage.

Because the total amount of dopants in contemporary process methods is lower, and the insertion or removal of a few impurity atoms can drastically modify transistor's electrical characteristics, and thus RDF has a stronger effect. RDF is a type of local process variation in which two identical transistors on a same silicon die with similar dopant concentrations may have considerably different dopant concentrations. ***Fig 2.4*** depicts the variations in the structure of a scaled device.

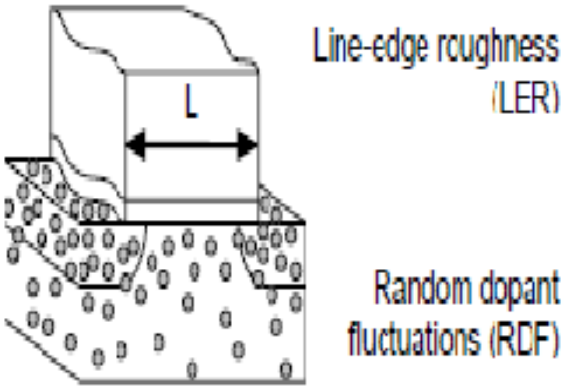
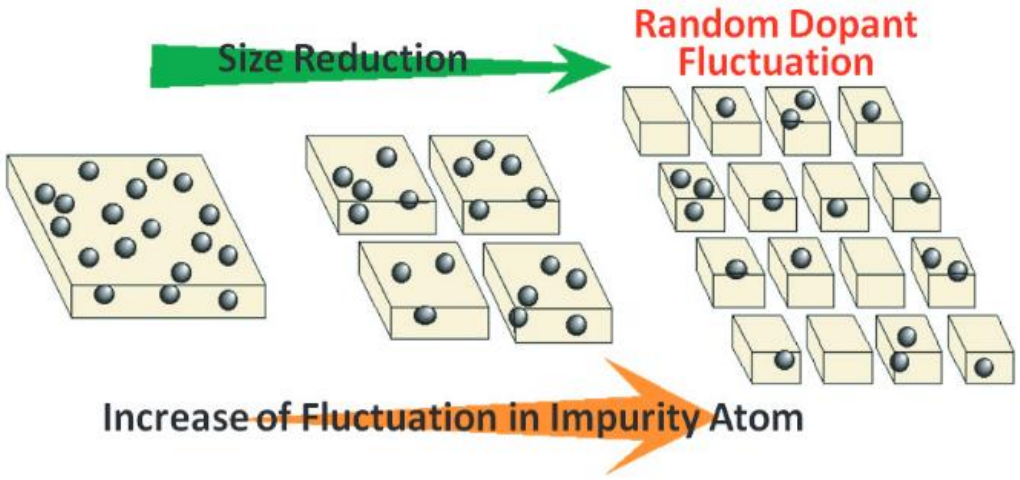


Figure 2.4 . Primary sources of variation in a nanoscale device.

These variations interact with one another, affecting every aspect of circuit performance. The RDF effect is primarily a random effect. The uncertainty in charge location and numbers, such as the discrete placement of dopant atoms in the channel region that follow a Poisson distribution, causes this well-known phenomenon. The overall number of channel dopants reduces as the device size shrinks, resulting in a wider fluctuation in dopant quantities and a considerable impact on threshold voltage. This is illustrated in the ***fig 2.5*** below.



Schemetic presentation for Figure 2.5 . Appearance of RDF increases with reduction in size of semiconductor bulk.

Impurity atoms are doped into the channel region of a transistor. Methods like dopant implantation randomly insert these atoms into the channel, resulting in statistical fluctuations in the number of impurities implanted. The threshold voltage and consequently the drive intensity of the transistor shift as the carrier concentration changes. With thousands of dopant atoms per channel region in prior technologies, an absolute divergence of a few atoms was insignificant. Recent technologies, on the other hand, have a nominal number of impurities in the tens, resulting in greater mismatch due to random dopant variation (RDF). Aside from random positioning, variations in the amount of dopant atoms present in the channel region will arise. While small variations in this value are unimportant in suitably large channel sizes, they will become vital in deca-nanometer devices with moderate doping concentrations.

RDF is proportional to dopant density in the channel region of the CMOS transistor for a certain technology, hence lowering RDF

can be accomplished by lowering dopant density.If the dopants were reduced to zero, the RDF would be eliminated completely; however, the CMOS device would no longer function as a controlled switching device because the threshold voltage would be zero. Furthermore, lowering the dopant density lowers the threshold voltage, increasing the device's static power consumption. Methods for on-chip measurement are becoming more important as the number and complexity of variable drivers grows.Through silicon measurements, both systematic and random process fluctuations must be measured and classified. Variability analysis necessitates the acquisition of a vast amount of data, necessitating test structures that are small in size and duration. Thus, for a given technology, the CMOS device must be designed to function at the lowest possible dopant density, resulting in the lowest RDF value, and then a footer transistor must be employed to restore the threshold voltage to the desired value in order to decrease static power.

2.3.1 CAUSES OF RDF EFFECT:

The various causes of random dopant fluctuation effect in nano scale transistors are:

- Wafer-to-wafer variance can be induced by changes in machine conditions over time in the production process.
- Any on-wafer non-uniformity, such as temperature and gas flow, can induce wafer level variation. Time-dependent lithography exposures could potentially be to blame.

- Since pattern exposure is done die-by-die, die level variance is usually caused by lithography stages. It can be induced by either reticle imperfections or non-ideality in lens systems.
- Layout dependent variation, like die level variation, has a spatial periodicity, but it differs in that it is significantly connected with the layout of patterns, such as density, distance from adjoining patterns, and so on. Mechanical stress pattern dependence and annealing temperature may also be the issue.

2.4 JUNCTIONLESS TRANSISTORS (JLT)

Recent advancements in semiconductor technology have given us the ability to investigate alternate techniques for producing transistors with the goal of lowering their sizes even more to increase transistor density and increase their performance. Traditional transistors rely on semiconductor junctions, which are created by doping atoms on a silicon substrate to create p-type and n-type areas. When the dimensions of such transistors is reduced to the nanometer scale, the junctions comes increasingly near, which becomes highly difficult due to the requirement of extremely large doping concentration gradients. Implementing junctionless transistors provides one of the most promising alternatives to this problem. The first junctionless transistor was manufactured in 2010, and many others have been proposed and explored since then (such as FinFET, Gate-All-Around, and Thin Film). Although all of these semiconductor devices have junctionless architectures, they differ when it comes to the impact of technological parameters on their electrical behavior and efficiency.

A junctionless transistor is a wrap-around gate, evenly doped nanowire with no junctions. Compared to a traditional transistor comprising of junctions, junction less transistor have less mobility degradation with gate voltage and temperature, very low leakage currents and, a near-ideal sub threshold slope.

2.4.1 DEVICE STRUCTURE OF JLT:

The NPN and PNP notations for bipolar devices and p- and n-type FETs with sources and drains came from the regulation of electron flow across junctions, which gave rise to the common NPN and PNP nomenclature for bipolar devices and p- and n-type FETs with sources and drains. The current in the device can be turned ON and OFF by controlling the junction. The properties and quality of the transistor are determined by the precise construction of such a junction, which is also a major element in the manufacturing cost. However, as a result of Moore's Law's projected recurring shrinkage, leading-edge transistors are getting so small that traditional transistor layouts are becoming extremely difficult to fabricate on chip.

One of the main purpose of using a JLFET is to reduce DIBL. It is one of the major short channel effect degrading the performance of conventional MOSFET devices with junctions. In DIBL, because of the short channel length, the drain depletion region reaches the source depletion region after a given time interval, lowering the barrier potential. The stretching of the depletion region from the drain to the source in short channel device is known as punch through. As a result, electrons moving from the source to the drain does not have to overcome a large potential barrier, resulting in leakage current through the device. Even when $V_{GS} < V_{th}$, the device remains ON due to the presence of this leakage current. As a result, the gate loses control of the drain current, increasing the device's static power dissipation.

But in case of JLFET, as no physical junctions are present within the device so the problem of *DIBL* is eliminated.

The Lilienfield transistor, like modern metal oxide semiconductor (MOS) devices, is a field-effect device. A thin semiconductor film is put on top of a narrow insulator layer, which is deposited on top of a metal electrode. The device's gate is made up of the latter metal electrode. Through operation, current can flow in the resistor between two contact electrodes, similar to how drain current flows in a conventional MOSFET between the source and drain. The Lilienfield device is a simple resistor in which the introduction of a gate voltage causes the carriers in the semiconductor layer to be depleted, changing its conductivity. In an ideal scenario, it should be feasible to deplete the semiconductor layer of carriers completely, resulting in a quasi-infinite resistance to the device. Unlike all other types of transistors, the Lilienfield transistor does not have a junction. The word 'transistor' is a shortened form of 'trans-resistor,' which is a solid-state active device that controls current flow. The Lilienfield transistor is a gated trans-resistor, which means it's a resistor with a gate that regulates carrier density and therefore current flow. Lilienfield's transistor would never have been able to construct a working device because it is the simplest and first trademarked transistor structure.

A junctionless nanowire gated resistor is shown schematically in ***fig. 2.6***.

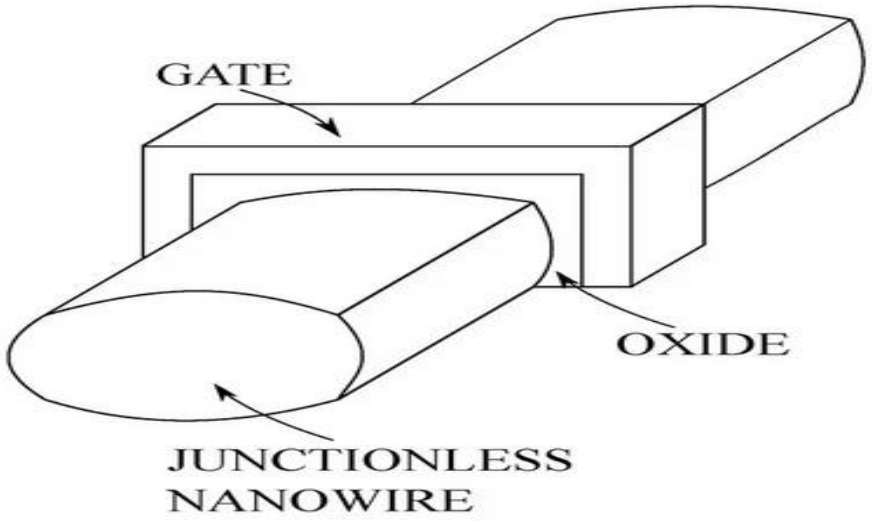


Figure 2.6 . Basic structure of the junctionless nanowire transistor.

The absence of a junction is a significant benefit. Present transistors are so small that ultra-sharp doping concentration gradients in junctions are required: generally, doping must switch from n-type with a concentration of $1x10^{19}$ cm^{-3} to p-type with a concentration of $1x10^{18}$ cm^{-3} in a matter of nanometres. This places severe constraints on the thermal budget of the processing and necessitating the development of expensive millisecond annealing procedures. The doping concentration in the channel of a junctionless gated resistor, on the other hand, is similar to that in the source and drain. No diffusion can occur since the gradient of doping concentration between source and channel or drain and channel is zero, removing the requirement for expensive ultra fast annealing procedures and allowing the fabrication of devices with shorter channels. Several researchers have successfully explored the gated resistor's operating principle using simulations.

2.4.2 OPERATION OF JLT:

Increase the channel doping concentration above traditional values to make a junctionless transistor with reasonable current drive. The use of doping levels considerably higher than $10x18cm^{-3}$ is generally discouraged, owing to the fact that bulk electron mobility drops below 100 $cm^2V^{-1}s^{-1}$ when the doping concentration approaches above $10x19cm^{-3}$.

In source and drain, as well as source and drain extensions, doping concentrations of 10^{19}–10^{20} cm^{-3} are commonly employed, but not in device channels. An n-channel junctionless transistor is made up of a single piece of N+ material rather than the usual N+-P-N+ sandwich found in inversion-mode (IM) MOSFETs.

The development of a thin and narrow semiconductor layer that allows for complete depletion of carriers when the device is turned off is critical to building a high-performance junctionless transistor (JLT). To allow for a reasonable quantity of current flow when the device is turned on, the semiconductor must be substantially doped. When these two restrictions are combined, nanoscale dimensions and large doping concentrations are required.

The device is turned off by full depletion of the channel region, rather than a reverse-biased junction, as in a standard IM MOSFET. The work function difference between the gate material and the doped silicon in the nanowire causes this depletion. The energy-band diagram for an n-channel JLT with a P + polysilicon gate electrode is shown in ***fig 2.7***.

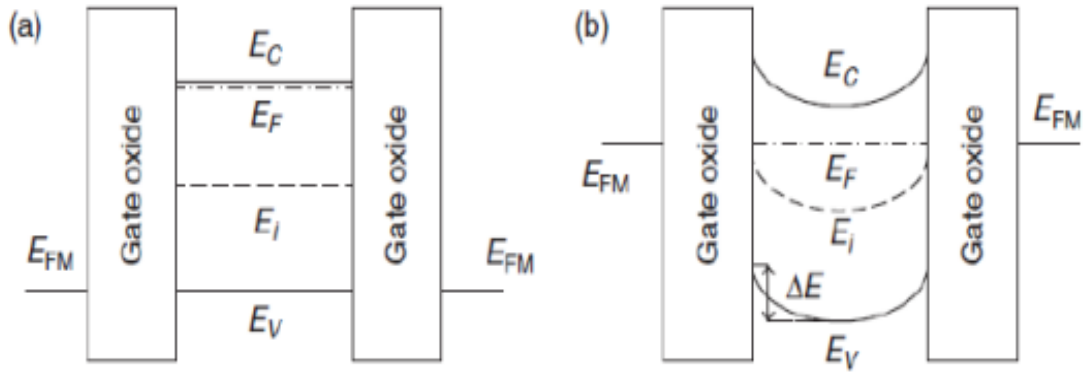


Figure 2.7. Energy-band diagram for an n-channel JLT **(a)** in the *ON* state (when the device is in flat-band condition) and **(b)** in the *OFF* state (i.e. the channel region is completely depleted).

When a positive gate bias equal to the work function difference between the nanowire and the gate material is applied to the gate, a flat-band state is achieved ***fig 2.7a***. The device is turned on in that situation. By constructing surface accumulation channels, a gate voltage greater than V_{FB} will boost current drive. The channel area is completely depleted when a zero gate bias is applied ***fig 2.7b***.

2.4.3 OPERATING MODES OF JLT:

The JLT's mechanics differ significantly from that of ordinary inversion mode multigate FETs. Here, we'll look at an n-channel device.The strongly doped nanowire is depleted, resulting in a significant electric field perpendicular to current flow below the threshold. If quantum-mechanical confinement effects are ignored, the electric field in the channel area is equal to zero under flatband bias circumstances (V_{FB}=0.5 V for a midgap metal gate and V_{FB}=1V for a P+ polysilicon gate). A surface accumulation layer with an accompanying electric field eventually

emerges at higher gate voltages. The electric field in the channel perpendicular to the current flow direction results in a decrease in channel carrier mobility in typical IM devices. The electron mobility in the channel of an IM MOSFET can fall below 20 cm^2/V s in the absence of strain-based mobility enhancement, considering an equivalent gate oxide thickness (EOT) of 1 nm and V_G= 1V.

Due to the screening effect, the electric field in the channel perpendicular to the current flow in a JLT is effectively equal to zero in the bulk of the nanowire, ensuring values equal to bulk mobility or greater. In addition, the device can be operated in a weak-accumulation mode. Because of the screening of Coulomb scattering centers by majority carriers, the resulting mobility (bulk + accumulation) can exceed textbook bulk mobility.

In n-channel junctionless SOI MOSFETs with a channel doping concentration of 10x17 cm^{-3} and an SOI body thickness of 48 nm, the screening effect was seen. The mobility of bulk MOSFETs was found to be greater than the universal mobility, as determined by conductance and carrier concentration (capacitance) tests. Because of the screening effect, the mobility enhancement is attributable to an increase in mobility in the SOI body above bulk mobility levels, rather than a greater mobility in the accumulation layer. For n- and p-type doping concentrations of 10x18cm^{-3}, screening effects were calculated using a tight-binding method, and transport properties were calculated using a Landauer-Buttiker/functions Green's approach and the linearized Boltzmann transport equation in the first Born approximation in GAA silicon nanowire transistors. The mobility of electrons in

accumulation-mode nanowires is substantially higher than in inversion-mode devices, according to these estimates. Acceptors act as tunnel barriers for electrons in IM nanowires, but carriers in accumulation-mode devices regard impurities as quantum wells, resulting in Fano resonances (resonant scattering phenomena) in the transmission. As a result, at low carrier density, electron mobility in phosphorus-doped nanowires is substantially higher than in boron-doped nanowires, but it can be higher in boron-doped nanowires at high carrier density. According to these estimates, mobility rises as the diameter of the nanowire decreases, whereas it remains constant or declines in IM devices.

The operation of inversion-mode, accumulation-mode, and JLT devices is compared in ***fig 2.8***.

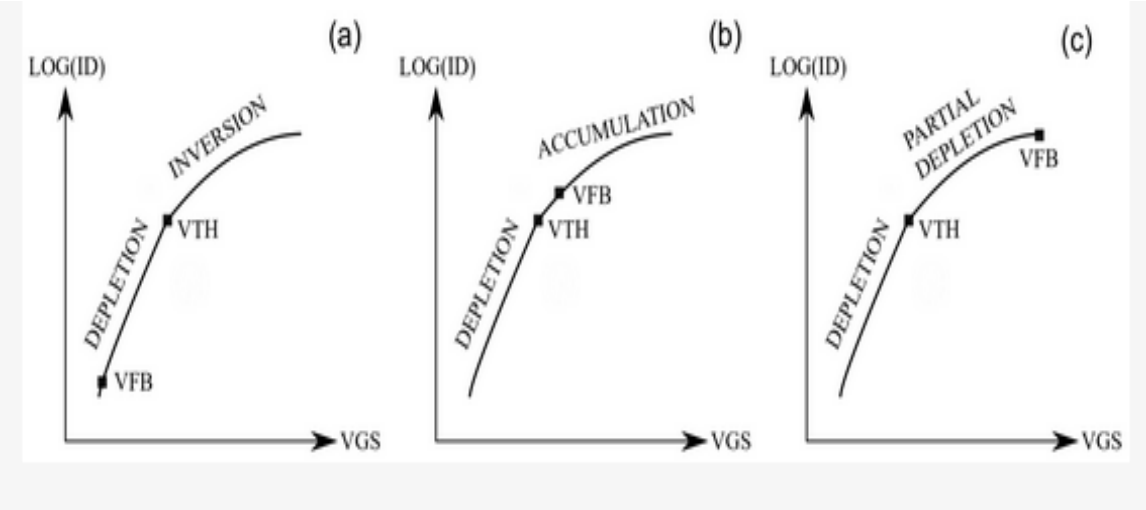


Figure 2.8 . Current drive in (a) inversion-mode, (b) accumulation-mode and, (c) junctionless mode.

The substrate in an n-channel IM device is p-type, and the flatband voltage, V_{FB}, is much below the threshold value, V_{TH}. The silicon is depleted in subthreshold operation, which occurs

between V_{FB} and V_{TH}. The silicon surface is strongly inverted for $V_G > V_{TH}$. It should be emphasised that if the silicon film is thin enough, bulk (volume) inversion can occur due to quantum confinement phenomena. The substrate in an n-channel accumulation-mode device is lightly doped n-type. Silicon is depleted during subthreshold operation. When a section of the silicon becomes neutral (i.e. no longer depleted), the threshold voltage is attained. In this neutral channel, a modest bulk current flows. When the entire silicon sheet is neutral, a somewhat greater gate voltage is used to achieve flatband voltage. The gadget is largely drained between V_{TH} and V_{FB}. Any additional rise in gate voltage results in the formation of a surface accumulation layer.

The substrate in an n-channel junctionless device is strongly doped n-type. The silicon is completely depleted during subthreshold operation. When a section of the silicon becomes neutral, the threshold voltage is attained. The device is partially depleted at this stage. Because the doping concentration in the channel region is substantially higher, the bulk current flowing in this neutral channel is much bigger than the bulk current flowing in the accumulation-mode device. Depletion reduces as gate voltage rises, but the diameter of the neutral channel expands. The entire channel region turns neutral when the gate voltage hits flatband voltage (assuming low V_{DS}). The creation of an accumulation layer occurs as the gate voltage is increased more. Because the transition from bulk to accumulation conduction is smooth in the $I_D(V_G)$ curve and its derivatives, flat-band voltage is difficult to obtain from current–voltage characteristics in extensively doped accumulation-mode and junctionless

transistors. Instead, because the transition between depletion and accumulation is clearer at flatband, the gate capacitance can be used to detect flatband. The electron concentration for various operating modes is illustrated in the ***fig 2.9*** below.

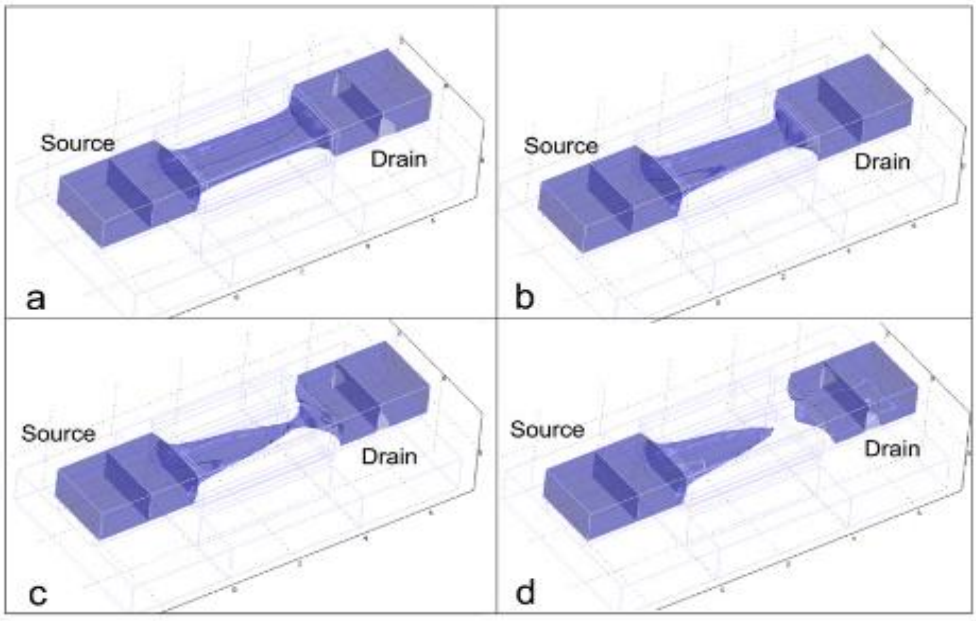


Figure 2.9. Electron concentration plots in an n-channel JLT. **a:** V_D = 50 mV; **b:** V_D = 200 mV; **c:** V_D = 400 mV; **d:** V_D = 600 mV. $V_G > V_{TH}$. Device parameters are: L = 40 nm, W_{si} = 20 nm, t_{si} = 10 nm, t_{ox} = 2 nm N_D = 10x19 cm^{-3}.

2.4.4 COMPARISON WITH JUNCTION TRANSISTOR:

In junctionless transistors, the electric field perpendicular to the current flow is substantially lower than in ordinary inversion-mode or accumulation-mode field-effect transistors. Because this electric field reduces inversion channel mobility in metal-oxide semiconductor transistors, junctionless transistors may have a benefit in terms of current drive for manometer-scale complementary metal-oxide semiconductor applications. When

quantum confinement is present, this observation still holds true. A Junction transistor's large carriers in the channel region act as a barrier to carrier scattering, but a Junctionless transistor does not have this problem, resulting in a high current drive. The JL transistors have the advantage of being simple to fabricate due to the absence of junction implantation and annealing; thus, a simple process results in a lower cost. For junction transistors, these advantages are hard to accomplish. Without the so-called short-channel effects (SCEs), standard CMOS devices confront a slew of challenges in achieving low-cost mass manufacture. The electric field of a transistor with and without junction is shown in the ***fig 2.10***.

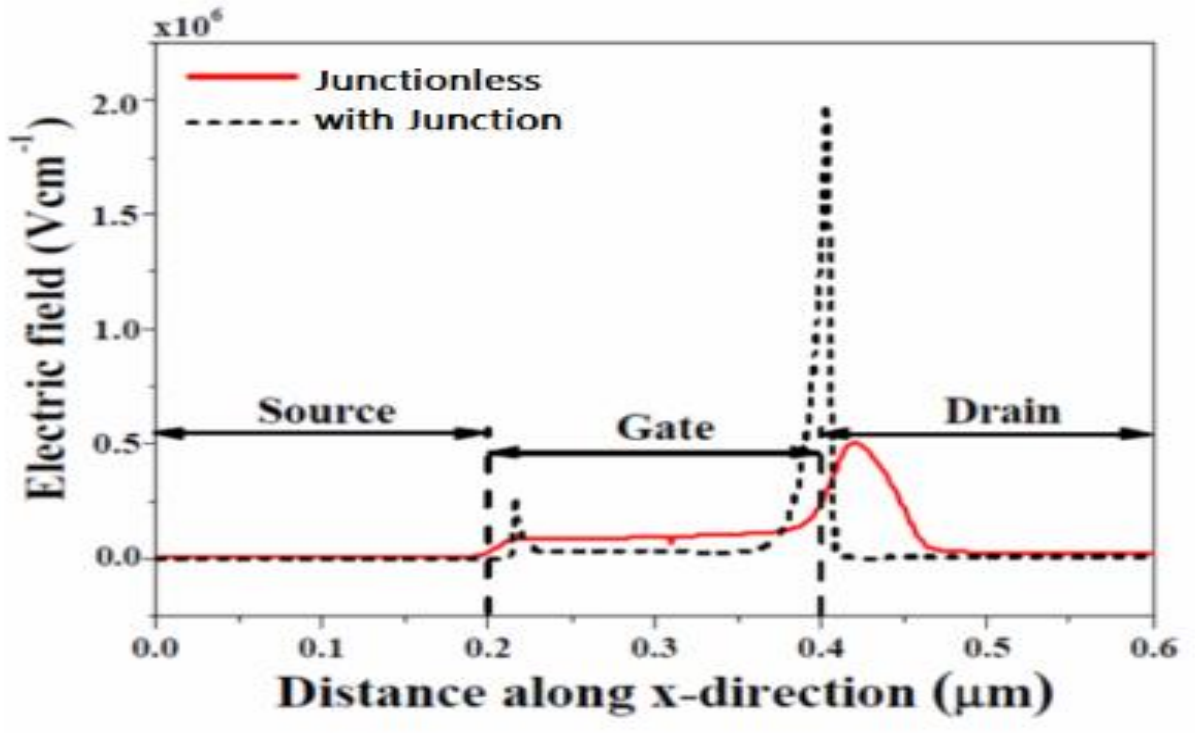


Figure 2.10. Comparison of electric field variation of transistors with junction and without junction.

2.5 CLASSIFICATION OF JLT:

Depletion-based and tunnel-based JLTs are the two primary types of junctionless transistors. The amount of current that passes through a depletion-based device is usually determined by the size of the depletion region, which is regulated by the applied gate voltage. Band-to-band tunneling controls the electrical current in tunnel-based devices (BTBT). The material composition of the channel, geometrical shape, and gate structure can all be used to classify JLT categories. A single gate junctionless transistor controls the current through the device by a single gate on the top of the channel. A Double Gate junctionless transistor is one that has a second gate below the channel. Thin Film junctionless transistors have a very thin channel thickness (less than 10 nm) and do not use monocrystalline silicon as the channel material. A gate electrode that completely surrounds the transistor's channel, which might be cylindrical or rectangular, distinguishes Gate-All-Around JLTs. The transistor channel is called junctionless Nanowire when it has a tube-shaped nanostructure. The electronic device is known as a junctionless FinFET if it is a fin-shaped transistor.

2.5.1 SINGLE GATE JLT:

As shown in ***fig 2.11***, the single gate JLT has two types of structures: bulk and SOI. Because the bulk structure can be doped and biased, it gives you more control over the device's characteristics. It is possible to improve the hot carrier effect and hence reduce the I_{off} current by positively biasing the well when using an n-type JLT with p-type bulk. However, by raising the

bulk bias, the threshold voltage can be reduced while DIBL and SS are increased. If the channel length is less than 20 nm, the degradation is considerably more noticeable. The I_{off} current is decreased when the substrate doping concentration is high. Furthermore, when compared to SOI, bulk junctionless transistors have a lower effective thickness; for example, a bulk SGJLT with a physical thickness of 10 nm has an effective thickness of 5 nm due to the built-in junction potential. The bulk SGJLT has better analog performance than the SOI structure, with better output transconductance, output resistance, early voltage, and inherent gain. The junctionless transistors were shown to be more sensitive to the T_{si}/W_{si} ratio and to offer a lower I_{on} when compared to junction transistors. The highly doped channel is responsible for this, as it increases the scattering effect, limiting mobility.

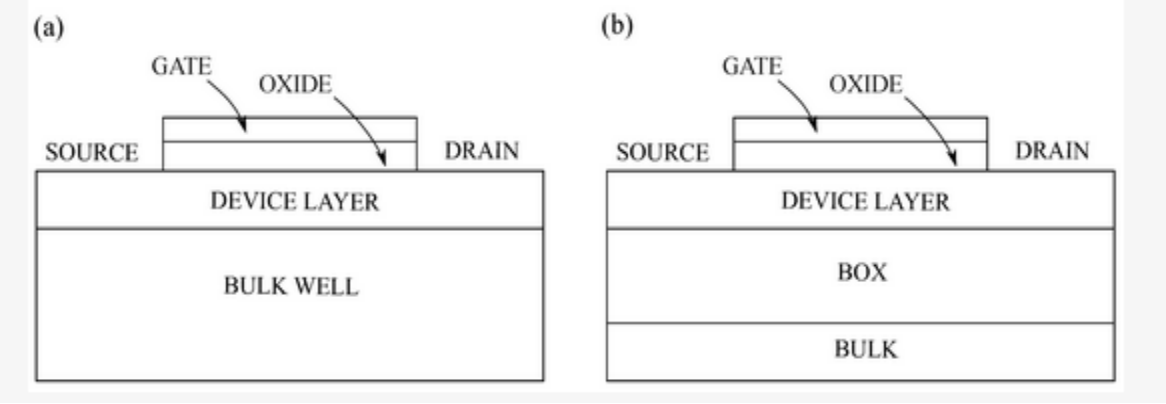


Figure 2.11. Cross-sectional view of: (**a**) Single Gate junctionless transistor (SGJLT) with high-k spacers. (**b**) SGJLT with SELBOX.

2.5.2 DOUBLE GATE JLT:

The structure of a double gate junctionless transistor is shown in the ***fig 2.12***.

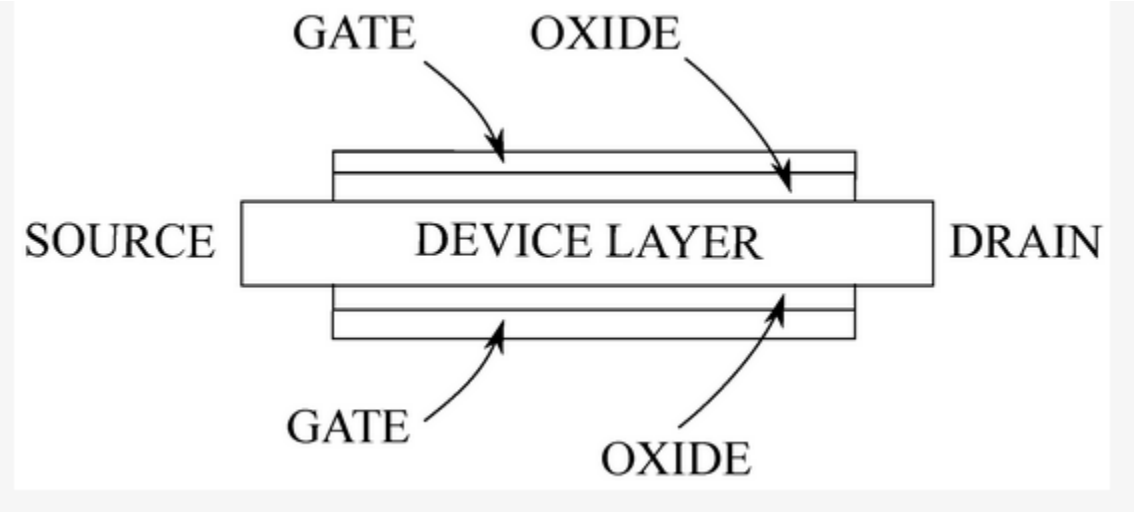


Figure 2.12. Cross-sectional view of a double gate junctionless transistor.

Many models have been presented, and the differences between them are based on the approximations used in the derivation and the effects examined. Many models, for example, ignore short channel and quantum effects, while others are only valid for a limited range of doping concentrations and device layer thicknesses. Because quantum effects can impact the threshold voltage, they are critical. Because the physical behaviour in the two operating regions differs, simulating the transition between the depletion and accumulation regions is a major challenge. To minimize model complexity, an approach utilizing high doping concentration in the device layer can be investigated. This assumption enables for easier depletion width modeling or the use of variable separation in the Poisson equation. Double gate junctionless transistors have a lower leakage current than single gate JLTs. The structure of double gate JLTs can further be

modified to reduce the leakage current through the device. The improved structure of a double gate JLT is illustrated in the ***fig 2.13*** below.

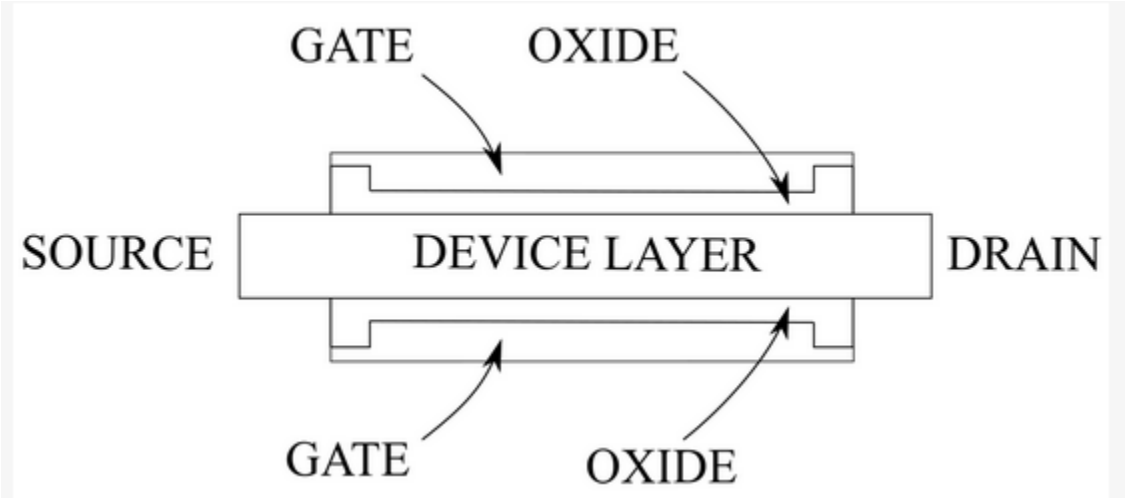


Figure 2.13. Modified Double Gate junctionless transistor (DG JLT). The gate oxide is thicker near to the gate edges.

It can be found out for the above structure that by implementing a thicker gate oxide near the gate edges, the energy bands of the carrier under the gate are modified as well resulting in lower leakage current.

2.5.3 TRI- GATE JLT or FINFET:

A bulk junctionless FinFET is shown schematically in ***fig 2.14a***. As shown in ***fig 2.14b***, the device can also be built on top of an insulator layer. We call it an SOI FinFET in that circumstance. The dimensions of these transistors have a significant effect on the overall performance. In bulk junctionless FinFETs, raising the fin width (W) from 6 nm to 15 nm can result in a 60 percent and 42 percent change in DIBL and SS, respectively; adjusting the gate length (LG) from 12 nm to 21 nm can result in a 52 percent

and 14 percent change in DIBL and SS, respectively. In terms of analog performance, variations in fin height (H) are more important factor of consideration. The junctionless FinFET has a lower I_{off} when compared to the inversion mode device. In the OFF state, this is due to the low carrier concentration and high electric field in the middle of the channel. When compared to SOI FinFETs, the bulk FinFET structure provides an additional design degree of freedom: changing the impurity concentration of the substrate from $1x10^{18}$ cm^3 to $1x10^{19}$ cm^3 results in a 30% variation in the threshold voltage. Additionally, it has a lower SS and DIBL. It can be modeled using traditional triple gate (TG) structures from an analytical standpoint.

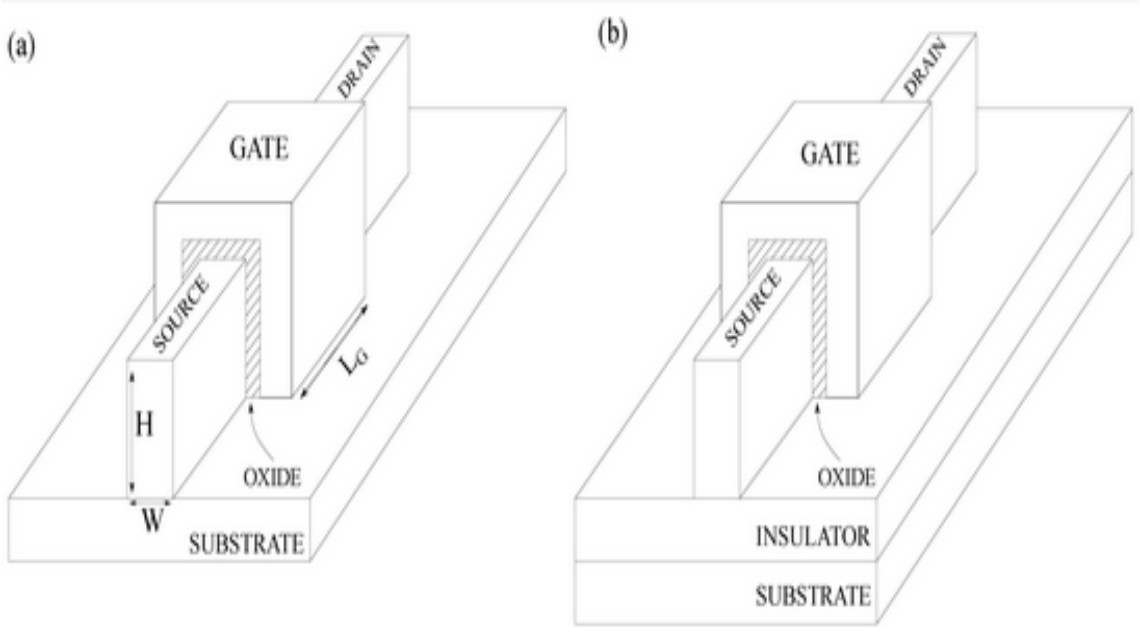


Figure 2.14. 3D TG JLFET or FinFET structure: (**a**) bulk, (**b**) SOI.

2.5.4 GATE-ALL-AROUND JLT or GAAFET:

A model of a cylindrical junctionless Gate-All-Around transistor is shown in ***Fig 2.15***.

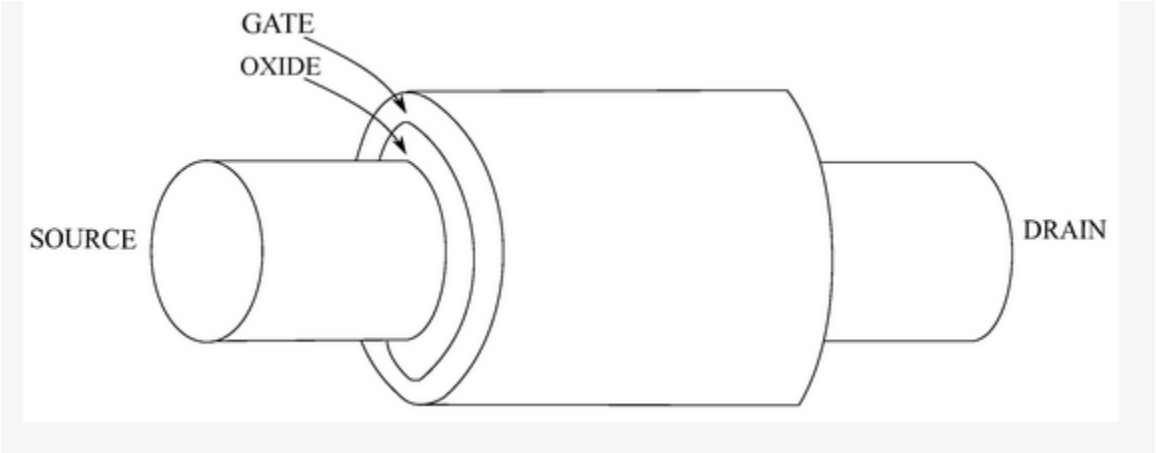


Figure 2.15 . Three-dimensional (3D) structure of a cylindrical junctionless GAAFET.

The device is distinguished by a channel completely enclosed by the gate, as the name implies. The complexity of the equations required to model device behavior is determined by the channel geometry. The cross sectional view of an gate all around JLFET is shown in the ***fig 2.16*** below.

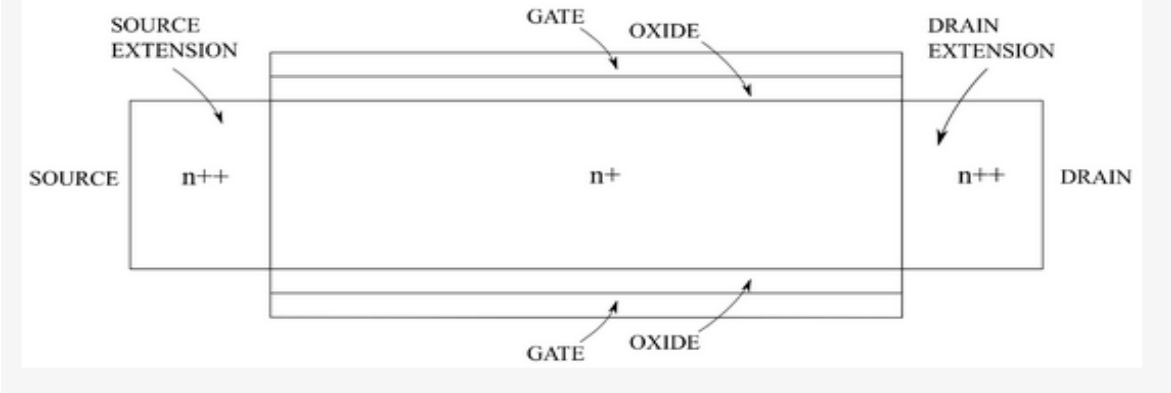


Figure 2.16 . Cross-sectional view of improved cylindrical GAAFET through addition of source and drain extensions

Because cylindrical coordinates must be provided, the solutions to the Poisson equations become more complicated. GAAFETs with rectangular channels have also been described, although their performance is degraded due to corner effects. The channel length is a key factor to consider when designing GAAFETs. The DIBL increases from 12 mV/V to 123 mV/V as the channel length is reduced from 40 nm to 16 nm, while the subthreshold slope increases from 62 mV/dec to 82 mV/dec. GAA JLFET can also have multi gate structure which are illustrated in the ***fig 2.17*** below.

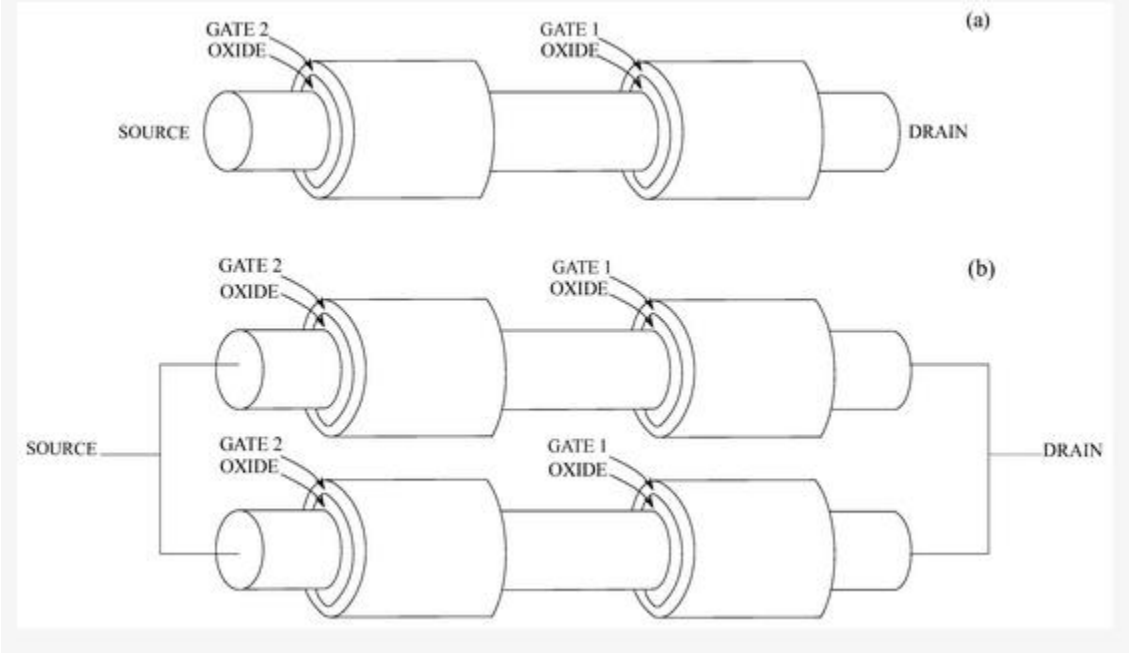


Figure 2.17. 3D Structure of (**a**) dual gate single channel GAAFET, (**b**) dual gate dual channel GAAFET.

CHAPTER 3

THRESHOLD VOLTAGE VARIATION IN TG JLFET DUE TO RDF

In this chapter we will analyze the V_{th} variation in a TG JLFET due to random dopant fluctuation effect. Here we will consider two doping distribution profiles; the first one will be *Normal Dopant Distribution* and the second one will be *Linear Dopant Distribution*.

It is also important to note that whenever we represent any term in our derived equations like ***W*** or ***H*** (in uppercase), it represents fixed value, and whenever we represent any term like ***w*** or ***h*** (in lowercase), it is treated as a variable.

3.1 Analysis of TG - JLFET:

From ref. **[1]** we get the surface potential ($\Phi_{surface}$) as,

$$\Phi_{surface} = \frac{qN_d}{\epsilon_{si}} \left[\frac{WH}{2H+W}\right]^2 \qquad (3.1.1)$$

where,

q = charge of an electron = 1.6 x 10^{-19} C.

N_d = Donor doping concentration.

ϵ_{si} = permittivity of silicon.

W = width of the silicon channel.

H = height of the silicon channel.

So the flat band voltage(V_{FB}) is given by,

$$V_{FB} - V_G - \Phi_{surface} = \frac{Q_{Si}}{C_{ox}} \qquad (3.1.2)$$

where,

V_G = Voltage applied at the gate terminal.

Q_{Si} = Charges present in the depletion region.

C_{ox} = Gate oxide capacitance.

In the above equation,

$$Q_{si} = \varepsilon_{si}.E_{surface}.(2H+W) \qquad (3.1.3)$$

where,

$E_{surface}$ = magnitude of Electric field on the silicon surface which is related to the surface potential as,

$$E_{surface} = \sqrt{(q.N_d.\Phi_{surface})/\epsilon_{si}} \qquad (3.1.4)$$

At threshold voltage condition,

$$V_G = V_{TH} \qquad (3.1.5)$$

Using eqns. (3.1.1) to (3.1.5) we get, the threshold voltage as,

$$V_{TH} = V_{FB} - qN_d\left[\frac{WH}{Cox} + \frac{1}{\epsilon si}\left[\frac{WH}{2H+W}\right]^2\right] \qquad (3.1.6)$$

Eqn 3.1.6 represents the expression of threshold voltage for a linear JLFET.

Effect of Random Dopant Fluctuation:

In eqn. (3.1.6) the device doping is considered to be random but uniform i.e. it is not varying along the dimensions of the device.

But in my assumptions I have considered the doping to be varying with the different dimensions of the device so, we consider two cases as defined below:

3.2: N_d is varying along channel width of TG - JLFET

So here N_d is replaced by $N_d(w)$ as it is varying with width and we modify eqn. (3.1.6) as,

$$V_{TH} = V_{FB} - qN_d(w)\left[\frac{wH}{Cox} + \frac{1}{\in si}\left[\frac{wH}{2H+w}\right]^2\right] \qquad (3.1.7)$$

Modifying the name of constants in eqn (3.1.7) we get

$$V_{TH} = V_{FB} - N_d(w)\left[Z_1(wH) + Z_2\left[\frac{wH}{2H+w}\right]^2\right] \qquad (3.1.8)$$

where,

the constants Z_1 and Z_2 are represented as,

$$Z_1 = {}^{q}/_{C_{ox}}$$

$$Z_2 = {}^{q}/_{\in_{si}}$$

Now differentiating eqn. (3.1.8) with respect to ***w*** we get,

$$\frac{dV_{TH}}{dw} = 0 - dN_d(w)\left[Z_1.H + Z_2\left\{2\left(\frac{wH}{2H+w}\right).\left(\frac{H(2H+w) - wH}{(2H+w)^2}\right)\right\}\right]$$

or,

$$\frac{dV_{TH}}{dw} = -dN_d(w)[Z_1.H + Z_2\{2(\frac{wH}{2H+w}).(\frac{2(H.H)+wH-wH}{(2H+w)^2})\}]$$

or,

$$\frac{dV_{TH}}{dw} = -dN_d(w)[Z_1.H + Z_2\{2(\frac{wH}{2H+w}).(\frac{2H^2}{(2H+w)^2})\}]$$

or,

$$\frac{dV_{TH}}{dw} = -dN_d(w)[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}] \quad (3.1.9)$$

Again from ref.[2] we get,

$$dN_d(w) = \frac{N_d(w)}{w.Lg}\,\delta(w - w_1) \quad (3.1.10)$$

where,

L_g = effective gate length ≈ channel length

w_1 = value of the width at which the rate of fluctuation doping concentration is maximum and L_g is the gate length of the device (here we have assumed effective channel length is equal to the gate length of the device). But in our case we are much more interested in checking the magnitude of variation rather than the shape of variation so we ignore $\delta(w - w_1)$ in our usage.

$\delta(w)$ = delta dirac function dependent on variable w.

A . Normal Dopant Variation Profile:

For a normal doping distribution profile we consider the doping concentration varying with the dimensions of the JLFET as,

$$N_d(v) = N_{do}\exp\left(-\frac{v^2}{2}\right) \qquad (3.1.11)$$

where,

N_d = is the donor concentration dependent on variable v along which the concentration of dopant atoms are assumed to be varying. It can be the width (***w***) or the Height (***h***) of the TG – JLFET or radius (***r***) of the cylindrical JLFET.

N_{do} = represents N_d *at* $v = 0$.

The doping profile varying with transistor dimension is shown in the ***fig 3.1*** below:

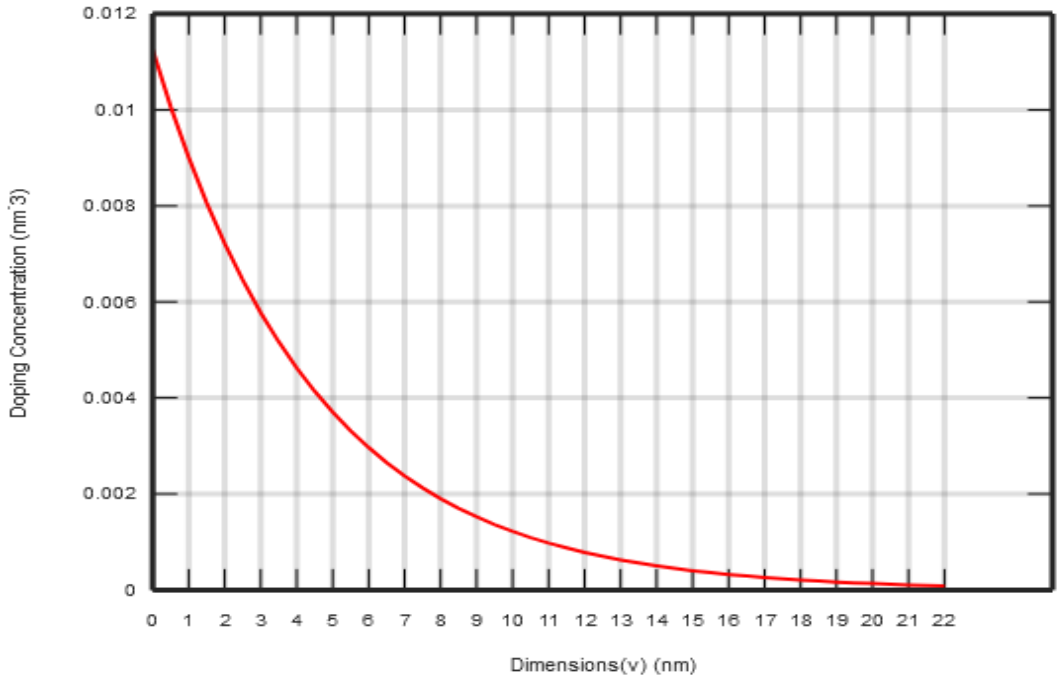


Figure 3.1 Normal dopant distribution along the dimensions.

It is importatant to note that we have considered the peak dopant concentration in nm^{-3} to match the dimensions on both the axes, which is approximately equal to $N_{do} = 0.0125\ nm^{-3} = 1.125\ x10^{19}\ cm^{-3}$.

Now using eqns. (3.1.11) and (3.1.10) in eqn. (3.1.9) we get,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}\exp(-\frac{w^2}{2})}{w.Lg}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right] \qquad (3.1.12)$$

Eqn. 3.1.12 represents the expression variation of threshold voltage (V_{th}) with the channel width(*w*) in TG JLFET for normal dopant distribution.

B . Linear Dopant Variation Profile:

For a linear doping distribution profile we consider the doping concentration varying with the dimensions of the JLFET as,

$$N_d(v) = m.v - N_{do} \qquad (3.1.13)$$

where,

N_d = is the donor concentration dependent on variable ***v*** along which the concentration of dopant atoms are assumed to be varying. It can be the width (***w***) or the Height (***h***) of the TG – JLFET or radius (***r***) of the cylindrical JLFET.

m = slope of variation of doping profile with a particular concerned dimension.

From eqn. (3.1.13), when the doping profile is varying along the width(w) of the TG – JLFET , we get,

$$N_d(w) = N_{do} - \left(\frac{N_{do}}{W_{max}}\right).w \qquad (3.1.14)$$

where,

$\boldsymbol{N_{do}} = N_d$ at $w = 0$,

m = $\left(\frac{N_{do}}{W_{max}}\right)$ is the slope of the doping profile with channel width which can be calculated easily from the ***fig 3.2***.

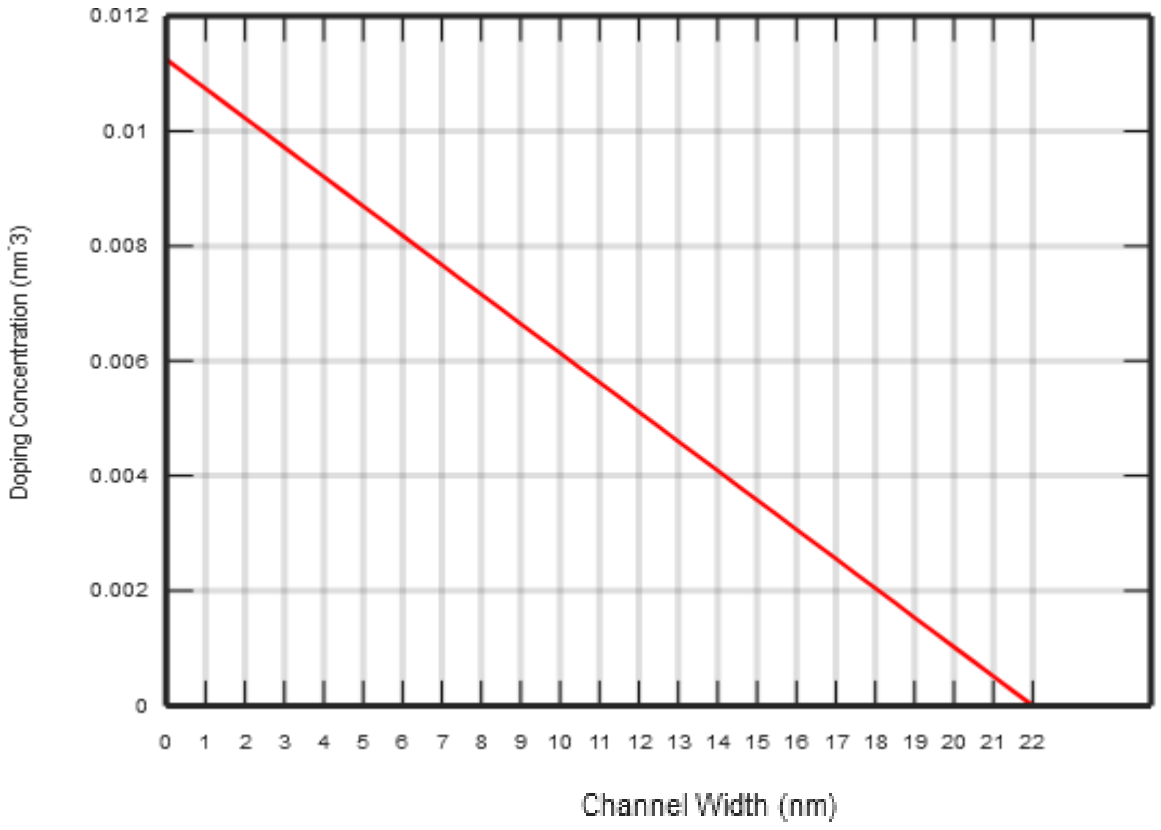


Figure 3.2 Linear dopant distribution along the channel width(*w*).

and,

W_{max} = the maximum width we have considered for a TG – JLFET.

Using eqn. (3.1.14) in eqn (3.1.10) , we get,

$$dN_d(w) = \frac{Ndo - (\frac{N_{do}}{W_{max}}).w}{w.Lg}\,\delta(w - w_1) \qquad (3.1.15)$$

Using eqn. 3.1.15 in eqn 3.1.9 , we get,

$$\frac{dV_{TH}}{dw} = -\left[\frac{Ndo - (\frac{N_{do}}{W_{max}}).w}{w.Lg}\right]\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]$$

or,

$$\frac{dV_{TH}}{dw} = \frac{(\frac{N_{do}}{W_{max}}).w - N_{do}}{w.Lg}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]$$

or,

$$\frac{dV_{TH}}{dw} = -\left[\frac{N_{do}}{w.Lg}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]\right] + \left[\frac{(\frac{N_{do}}{W_{max}}).\cancel{w}}{\cancel{w}.Lg}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]\right]$$

or,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}}{L_g}\left[\frac{1}{w}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right] + \frac{1}{W_{max}}\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]\right]$$

or,

$$\boxed{\frac{dV_{TH}}{dw} = \frac{N_{do}}{L_g}.\left[\frac{1}{W_{max}} - \frac{1}{w}\right].\left[Z_1.H + Z_2\{(\frac{4wH^3}{(2H+w)^3})\}\right]} \qquad (3.1.16)$$

Eqn. 3.1.16 represents the expression variation of threshold voltage (V_{th}) with the channel width(*w*) in TG JLFET for linear dopant distribution.

3.3 : N_d is varying along channel height of TG - JLFET

So here N_d is replaced by $N_d(h)$ as it is varying with height and we modify eqn. (3.1.6) as,

$$V_{TH} = V_{FB} - qN_d(h)[\frac{Wh}{Cox} + \frac{1}{\in si}[\frac{Wh}{2h+W}]^2] \qquad (3.1.17)$$

Modifying the name of constants in eqn 3.1.17 we get

$$V_{TH} = V_{FB} - N_d(h)[Z_1(W.h) + Z_2[\frac{Wh}{2h+W}]^2] \qquad (3.1.18)$$

Now differentiating eqn. (3.1.17) with respect to **h** we get,

$$\frac{dV_{TH}}{dh} = 0 - dN_d(h)[Z_1.W + Z_2\{2(\frac{Wh}{2h+W}).(\frac{W(2h+W)-2Wh}{(2h+W)^2})\}]$$

or,

$$\frac{dV_{TH}}{dh} = -dN_d(h)[Z_1.W + Z_2\{2(\frac{Wh}{2h+W}).(\frac{2Wh+(W.W)-2Wh}{(2h+W)^2})\}]$$

or,

$$\frac{dV_{TH}}{dh} = -dN_d(h)[Z_1.W + Z_2\{2(\frac{Wh}{2h+W}).(\frac{W^2}{(2h+W)^2})\}]$$

or,

$$\frac{dV_{TH}}{dh} = -dN_d(h)[Z_1.W + Z_2\{\frac{2hW^3}{(2h+W)^3}\}] \qquad (3.1.19)$$

Again from ref. **[2]** we get,

$$dN_d(h) = \frac{N_d(h)}{W.Lg}\,\delta(h - h_1) \qquad (3.1.20)$$

where,

$\mathbf{h_1}$ = the value of the height at which the rate of fluctuation doping concentration is maximum

L_g = effective gate length of the device (here we have assumed effective channel length is equal to the gate length of the device).

In our case we are much more interested in checking the magnitude of variation rather than the shape of variation so we ignore $\delta(h - h_1)$ in our usage.

A . Normal Dopant Variation Profile:

Using eqns. (3.1.11) and (3.1.20) in eqn. (3.1.19) we get,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp(-\frac{h^2}{2})}{W.Lg}\,[Z_1.W + Z_2\{(\frac{2HW^3}{(2H+W)^3})\}] \qquad (3.1.21)$$

Simplifying further in eqn. (3.1.21) we get,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\,[Z_1 + Z_2\{\frac{2hW^2}{(2h+W)^3}\}] \qquad (3.1.22)$$

Eqn. 3.1.22 represents the expression variation of threshold voltage (V_{th}) with the channel height (h) in TG JLFET for normal dopant distribution.

B . Linear Dopant Variation Profile:

From eqn. (3.1.18) and (3.1.19) we get,

$$\frac{dV_{TH}}{dh} = -dN_d(h)[Z_1.W + Z_2.\{\frac{2hW^3}{(2h+W)^3}\}] \qquad (3.1.18)$$

and,

$$dN_d(h) = \frac{N_d(h)}{W.Lg}\,\delta(h - h_1) \qquad (3.1.19)$$

From eqn. (3.1.13), when the doping profile is varying along the height(h) of the TG – JLFET , we get,

$$N_d(h) = N_{do} - (\frac{N_{do}}{H_{max}}).h \qquad (3.1.23)$$

where,

$N_{do} = N_d$ at $h = 0$.

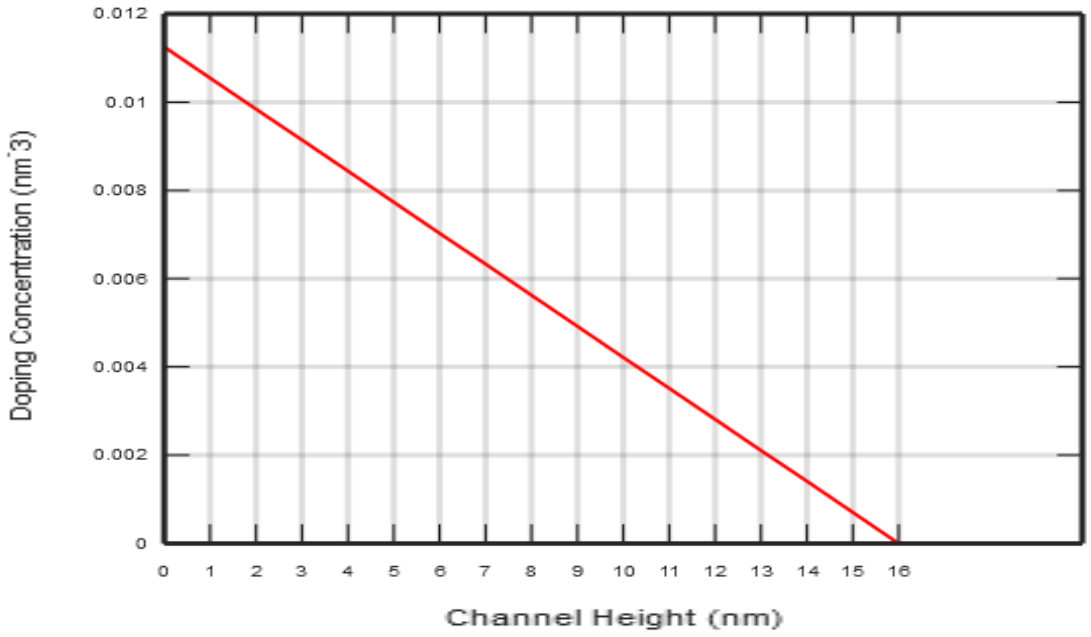


Figure 3.3 Linear dopant distribution along the channel height(*h*).

m = $(\frac{N_{do}}{H_{max}})$, is the slope of the doping profile with channel height which can be calculated easily from the ***fig 3.3***.

$\boldsymbol{H_{max}}$ = the maximum height we have considered for a TG – JLFET.

Using eqn. (3.1.23) in eqn (3.1.19) , we get,

$$dN_d(h) = \frac{N_{do} - (\frac{N_{do}}{H_{max}}).h}{W.Lg}\,\delta(h - h_1) \qquad (3.1.24)$$

Using eqn. (3.1.24) in eqn (3.1.18) , we get,

$$\frac{dV_{TH}}{dh} = -\left[\frac{N_{do} - (\frac{N_{do}}{H_{max}}).h}{W.Lg}\right].[Z_1.W + Z_2.\{\frac{2hW^3}{(2h+W)^3}\}]$$

or,

$$\frac{dV_{TH}}{dh} = \left[\frac{(\frac{N_{do}}{H_{max}}).h - N_{do}}{W.Lg}\right].[Z_1.W + Z_2.\{\frac{2hW^3}{(2h+W)^3}\}]$$

Canceling out *"W"* from numerator and denominator, we get,

$$\frac{dV_{TH}}{dh} = \left[\frac{(\frac{N_{do}}{H_{max}}).h - N_{do}}{Lg}\right].[Z_1 + Z_2.\{\frac{2hW^2}{(2h+W)^3}\}]$$

or,

$$\boxed{\frac{dV_{TH}}{dh} = \frac{N_{do}}{Lg}.[\frac{h}{H_{max}} - 1].[Z_1 + Z_2.\{\frac{2hW^2}{(2h+W)^3}\}]} \qquad (3.1.25)$$

Eqn. 3.1.25 represents the expression variation of threshold voltage (V_{th}) with the channel height (*h*) in TG JLFET for linear dopant distribution.

3.4 VALIDATION OF OUR PROPOSED MODEL:

To proceed further with the problem addressed in the present dissertation, we prefer to check the validity of ou proposed model with the results available in literature.

To verify our proposed model, we compare its threshold voltage variation with the threshold voltage variation of the reference model mentioned in ***Gnudi et. al.*** [2].

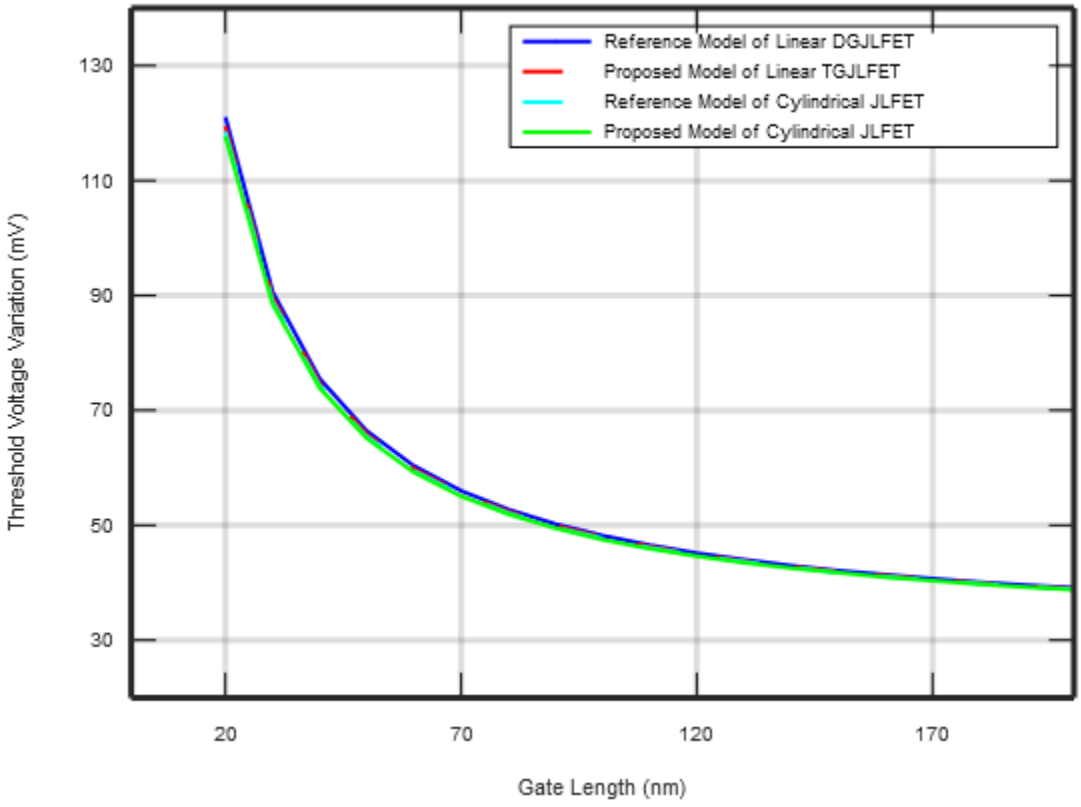


Figure 3.4 Comparison of V_{th} variation in both Linear JLFET and Cylindrical JLFET as per *Gnudi et. al.*

Fig. 3.4 indicates that the threshold voltage variations in our proposed models becomes almost identical to those in the reference model. It thus validates our proposed model and related results which will be applied in subsequent sections.

It is also important to note one thing the the reference model is of DGJLFET whereas the proposed model is of TGJLFET so the short channel length V_{th} variation of our proposed model will be slightly less than reference model, which is also evident from our graph at gate length $(L_g) = 20nm$. However, in the cases of long channel devices, all these structures will behave identically, as the JLFET structures got modified to suit better in case of short channel lengths which is or main area of concern. Here to determine the above result, we have considered radius (***r***) of cylindrical JLFET to be *10nm*.

As the channel length in our reference paper is considered to be very large value so we can observe fom the plot that V_{th} variation of all the devices(both referred device as well as proposed device) gets ovelapped with each other because for a longer channel, all the devices will behave identically because in that case the effect of RDF is negligible. The actual difference is observed in the when we reduce the channel length as illustrated in ***fig. 3.5***.

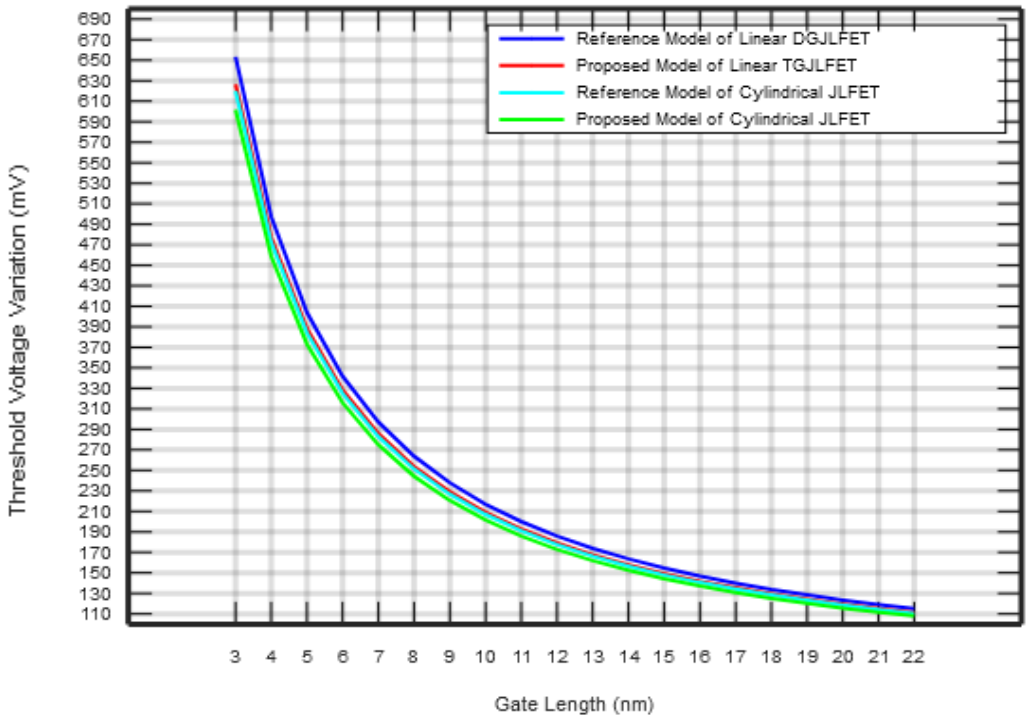


Figure 3.5 V_{th} variation observed for very short channel length between proposed model and reference model on basis of *eqn*. appeared in [*2*].

3.5 Results and Discussion:

To determine the results for V_{th} variation in a TG JLFET, we will consider L_g and w to be varying from 3nm to 22nm and h to be varying from 2.3nm to 16 nm. Here value of W_{max} and H_{max} are considered to be 22nm and 16 nm respectively.

A . For Normal Dopant Distribution:

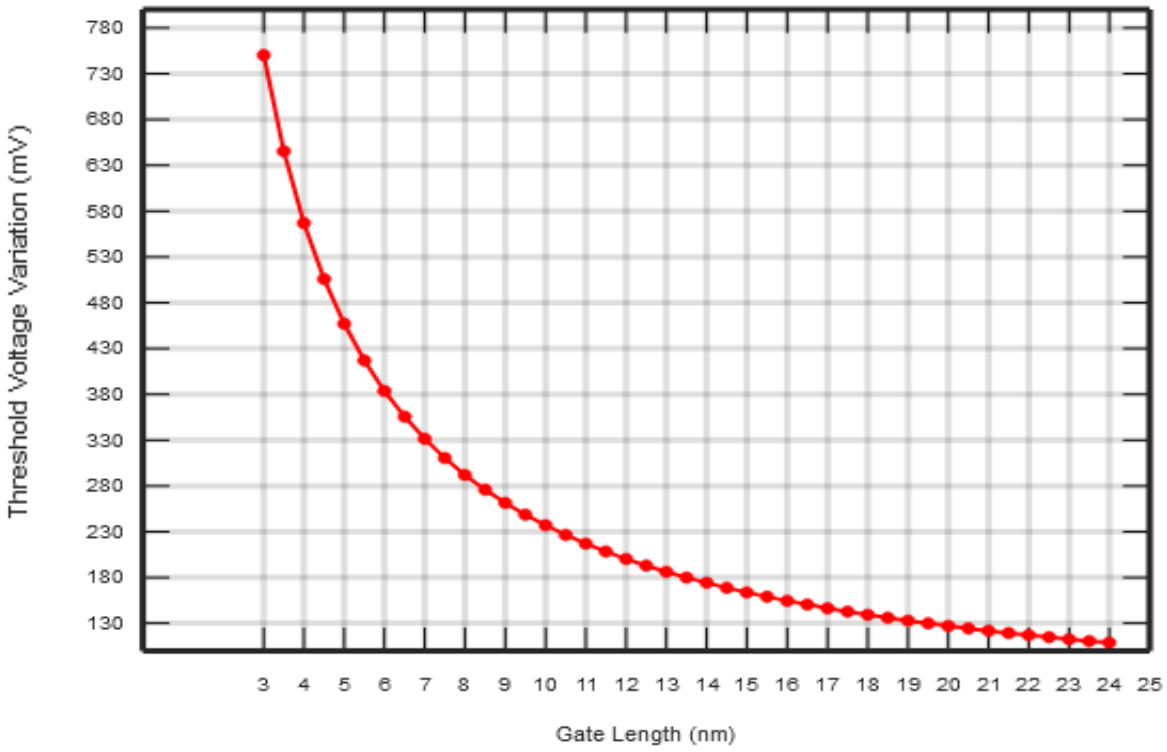


Figure 3.6 V_{th} variation with gate length for *normal doping profile*.

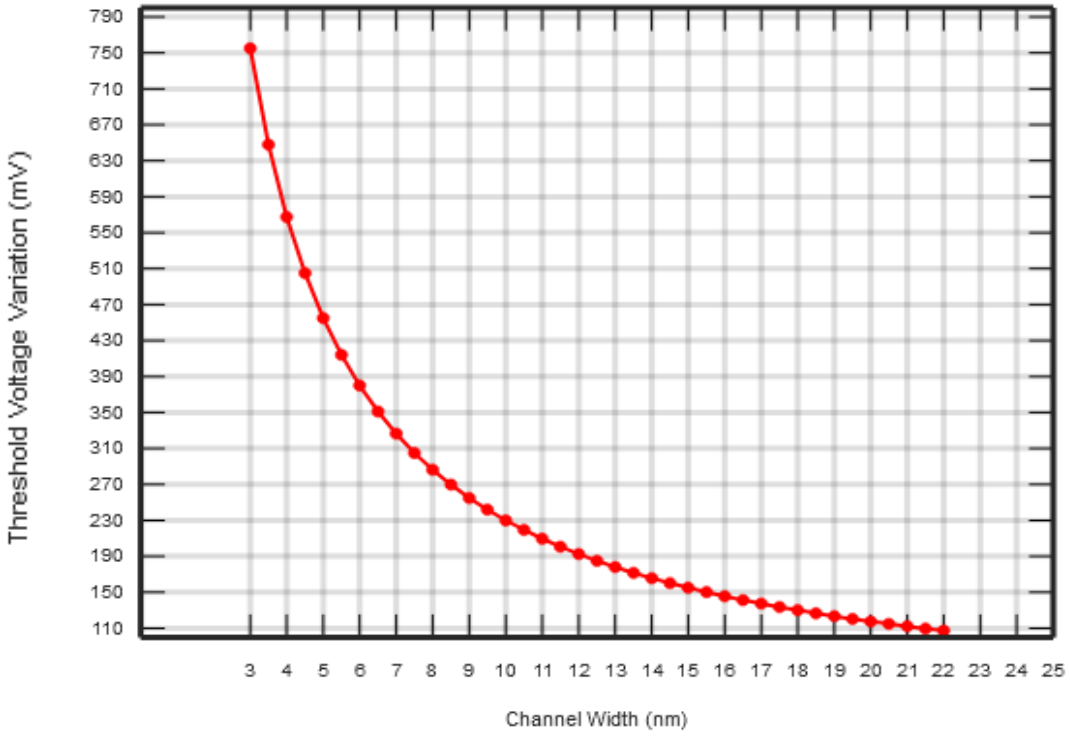


Figure 3.7 V_{th} variation with channel width for *normal doping profile*.

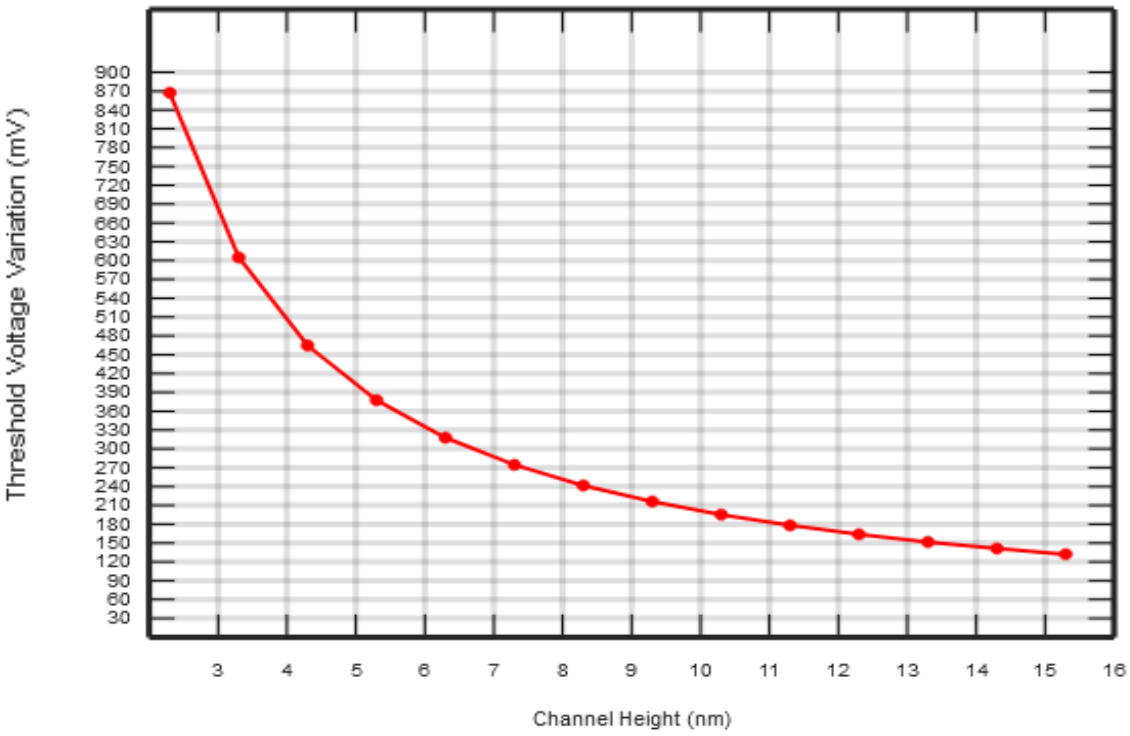


Figure 3.8 V_{th} variation with channel height for *normal doping profile*.

Fig 3.6 shows the plot of V_{th} variation with the gate length($\boldsymbol{L_g}$) due to RDF effect for *normal dopant distribution*. It is quite evident from the above plot that if we reduce $\boldsymbol{L_g}$ i.e. for a short channel device, the variation of V_{th} increases rapidly compared to when $\boldsymbol{L_g}$ is of high value. This is due to the fact that fluctuation of dopant atoms is more prominent in a smaller device than a larger device.

Fig 3.7 and ***fig. 3.8*** illustrates the plot of V_{th} variation with the channel width(***w***) and channel height(***h***) due to RDF effect for *normal dopant distribution* respectively. The reason for rapid increment of V_{th} with reduced ***w*** and ***h*** is same as explained in case of gate length.

B . For Linear Dopant Distribution:

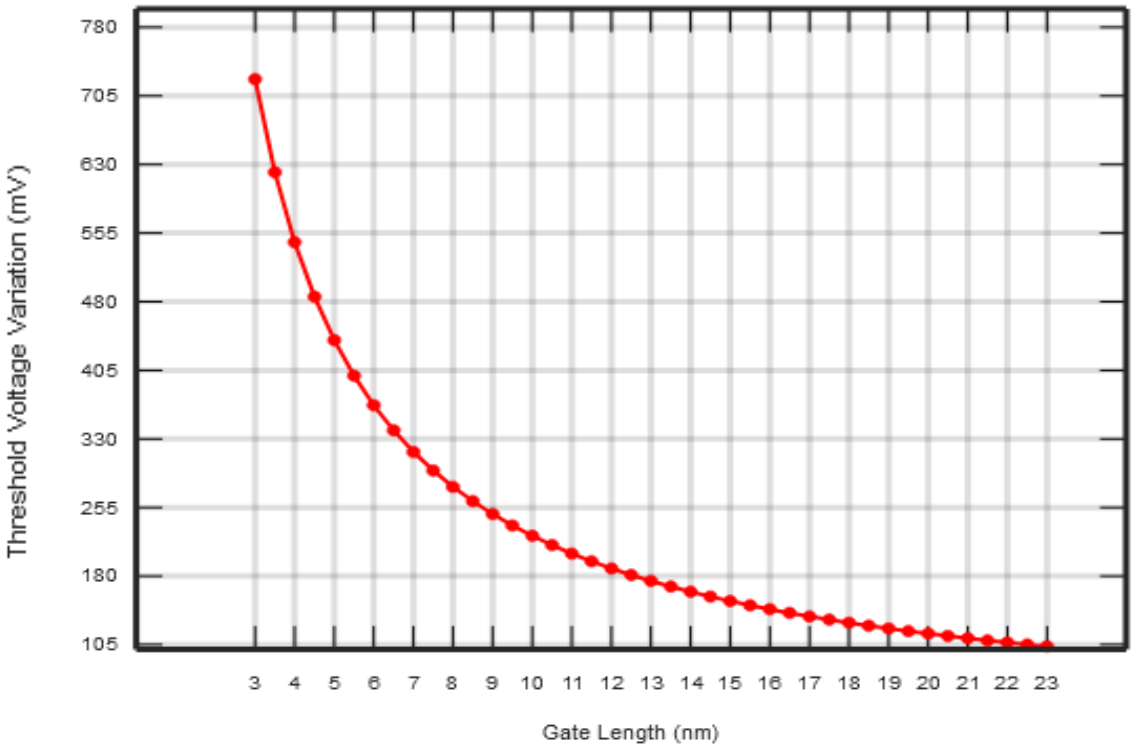


Figure 3.9 V_{th} variation with gate length for *linear doping profile*.

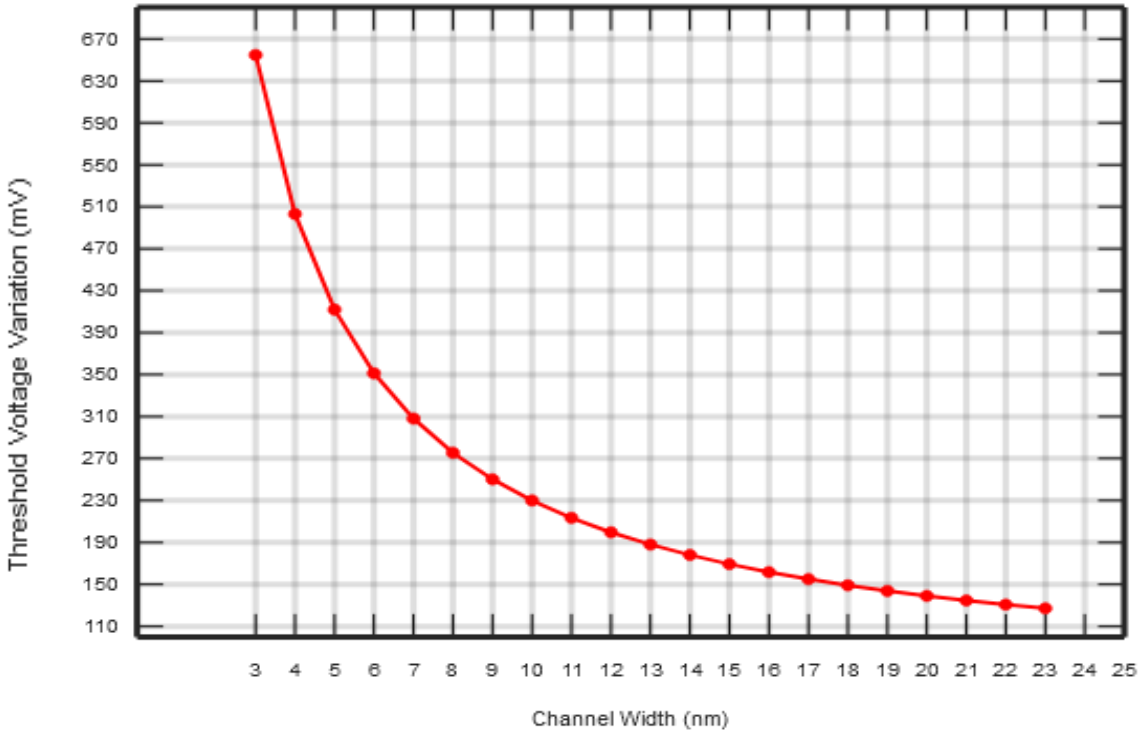


Figure 3.10 V_{th} variation with channel width for *linear doping profile*.

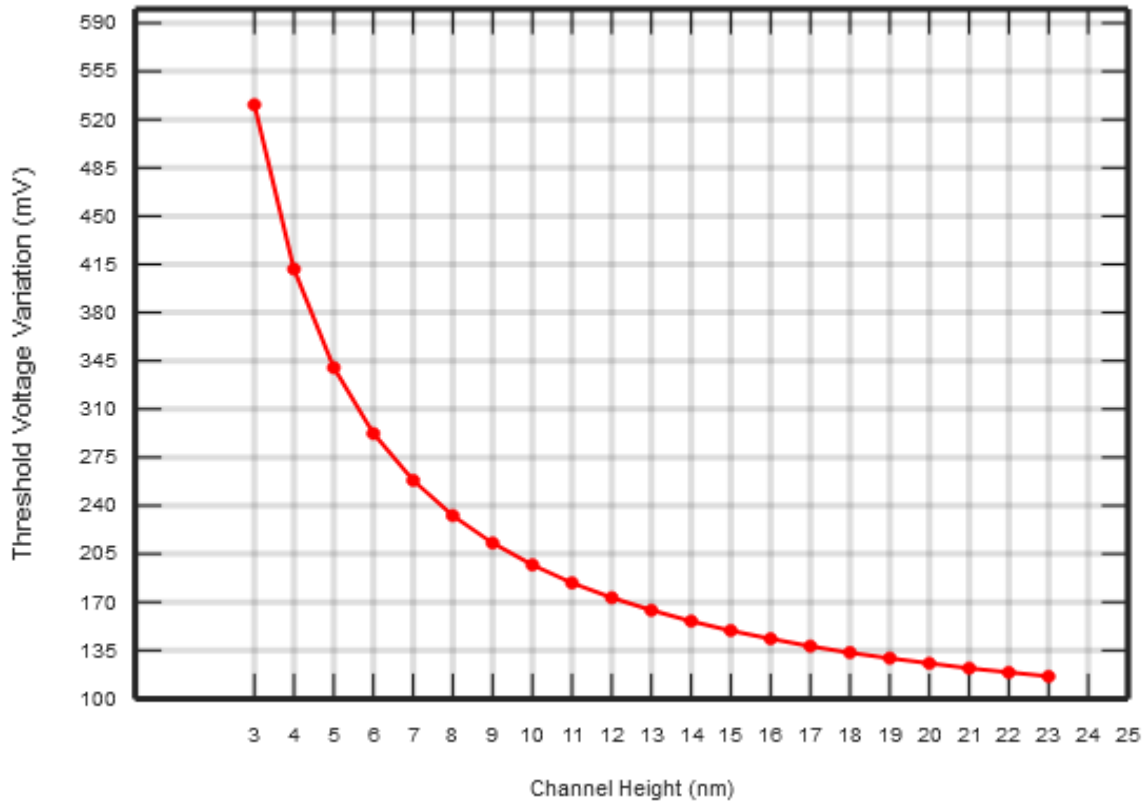


Figure 3.11 V_{th} variation with channel height for *linear doping profile*.

Fig 3.9, fig 3.10 and ***fig. 3.11*** illustrates the plot of V_{th} variation with the gate length($\boldsymbol{L_g}$), channel width($\boldsymbol{w}$) and channel height($\boldsymbol{h}$) respectively due to RDF effect. In this case, instead of considering normal dopant distribution, we have considered linear dopant distribution. Here also the V_{th} varies rapidly for smaller channel dimensions because of increasing nature of RDF effect with reduced channel size. However, the rate of increment of V_{th} in linear dopant distribution is less compared to a normal dopant distribution.

3.6 Conclusion:

This chapter deals with the performance analysis of TG JLFET under RDF effect. Here, the variation of V_{th} with various channel dimensions such as L_g, w and h are investigated. It gives the clear idea about how the TG JLFET will behave during operation under the influence of random dopant fluctuation effect.

CHAPTER 4

THRESHOLD VOLTAGE VARIATION IN CYLINDRICAL JLFET DUE TO RDF

In this chapter we will analyze the V_{th} variation in a cylindrical JLFET due to random dopant fluctuation effect. Here we will consider two doping distribution profiles; the first one will be normal doping distribution and the second one will be linear doping distribution.

It is also important to note that whenever we represent radius of cylindrical JLFET in our derived equations like ***R***(in uppercase), it represents constant value, and whenever we represent radius like ***r***(in lowercase), it is treated as a variable.

In this case we will design our proposed device i.e. the cylindrical JLFET by transforming the linear co-ordinates of TG - JLFET into cylindrical co-ordinates. The model of cylindrical JLFET which we have assumed is shown in ***fig 4.1,***

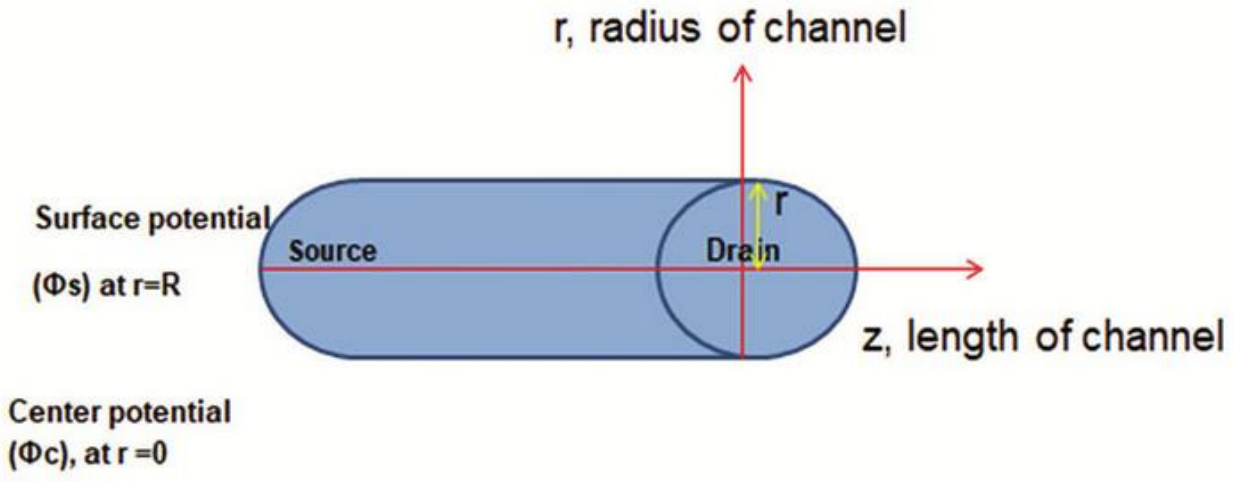


Figure 4.1 Proposed model of Cylindrical JLFET.

4.1 Analysis of Cylindrical JLFET:

From eqn. 3.1.6 , we get,

$$V_{TH} = V_{FB} - qN_d\left[\frac{WH}{Cox} + \frac{1}{\in si}\left[\frac{WH}{2H+W}\right]^2\right]$$

Writing the above eqn. in terms of area of cross section(***A***) and gate perimeter(***P***) of the device as well as constants Z_1 and Z_2 we get,

$$V_{TH} = V_{FB} - N_d\left[Z_1.A + Z_2.\left[\frac{A}{P}\right]^2\right] \qquad (4.1.1)$$

where,

$$A = W.H\ ,$$
$$P = (2H+W)$$

Again we know that in cylindrical JLFET, radius(***r***) of JLFET can be written in terms of W and H as,

$$r = \sqrt{w^2 + h^2} \qquad (4.1.2)$$

Since when we transform from linear co-ordinates into cylindrical co-ordinates we get,

$$W = r.cos\Phi \quad \text{and} \quad H = r.sin\Phi \qquad (4.1.3)$$

Using eqns. (4.1.2) and (4.1.3) , we get,

$$\Phi = cos^{-1}(W/\sqrt{W^2 + H^2}) = sin^{-1}(H/\sqrt{W^2 + H^2}) \qquad (4.1.4)$$

Also for a cylindrical JLFET, area of cross section(*A*) and gate perimeter(*P*) are given by,

$$A = \pi r^2$$
$$P = 2\pi r \qquad (4.1.5)$$

Using eqns. (4.1.4) and (4.1.5) in (4.1.1) , we get,

$$V_{TH} = V_{FB} - N_d [Z_1 . (\pi r^2) + Z_2 . [\frac{\pi r^2}{2\pi r}]^2]$$

Simplifying the above eqn. , we get,

$$V_{TH} = V_{FB} - N_d [Z_1 . (\pi r^2) + Z_2 . (\frac{r}{2})^2] \qquad (4.1.6)$$

4.1.1 : N_d is varying along the radius (*r*) of Cylindrical JLFET

So here N_d is replaced by $N_d(r)$ as it is varying with radius and we modify eqn. (4.1.6) as,

$$V_{TH} = V_{FB} - N_d(r)[Z_1 . (\pi r^2) + Z_2 . (\frac{r^2}{4})] \qquad (4.1.7)$$

Now differentiating eqn. (4.1.7) with respect to ***r*** we get,

$$\frac{dV_{TH}}{dr} = 0 - dN_d(r)[Z_1 .(2\pi r) + Z_2 . (\frac{r}{2})]$$

or,

$$\frac{dV_{TH}}{dr} = - dN_d(r)[Z_1 .(2\pi) + Z_2 . (\frac{1}{2})] . r$$

or,

$$\frac{dV_{TH}}{dr} = -dN_d(r)[Z_3 + Z_4].r \qquad (4.1.8)$$

where,

$$Z_3 = (2\pi).Z_1$$

and,

$$Z_4 = {}^{Z_2}/_{2}$$

Again from ref. **[2]** we get,

$$dN_d(r) = \frac{N_d(r)}{2\pi r.L_g}\delta(r - r_1) \qquad (4.1.9)$$

where,

r_1 **=** the value of the radius at which the rate of fluctuation doping concentration is maximum.

L_g = the gate length of the device (here we have assumed effective channel length is equal to the gate length of the device). But in our case we are much more interested in checking the magnitude of variation rather than the shape of variation so we ignore $\delta(r - r_1)$ in our usage.

A . Normal Dopant Distribution:

Refering from chapter 3.1.1(a), we get,

Using eqns. (3.1.11) and (4.1.9) in eqn. (4.1.8) we get,

$$\frac{dV_{TH}}{dr} = -\frac{N_{do}\exp(-\frac{r^2}{2})}{(2\pi r).L_g}[Z_3+ Z_4] \qquad (4.1.10)$$

Using eqn. (4.1.2) in eqn. (4.1.10) we get,

$$\frac{dV_{TH}}{dr} = -\frac{N_{do}\exp(-\frac{w^2+h^2}{2})}{(2\pi).L_g}[Z_3+ Z_4] \qquad (4.1.11)$$

The above expression i.e. eqn. (4.1.11) gives the rate of change of V_{TH} with respect to the radius(r) of the cylindrical MOSFET in terms of width(w) and height (h) of the TG JLFET. This expression is important because using it we can compare the performance analysis of the above devices under random dopant fluctuation effect for smaller dimensions by simply varying the height and width of both the junctionless transistors.

From eqn. (4.1.2), we get,

$$r = \sqrt{w^2 + h^2}$$

or,

and,

$$\frac{dr}{dw} = \frac{w}{\sqrt{w^2+H^2}}$$

$$\frac{dr}{dh} = \frac{h}{\sqrt{W^2+h^2}} \qquad (4.1.12)$$

Again from chain rule of differential calculus, we know that,

$$\frac{dV_{TH}}{dw} = \frac{dV_{TH}}{dr} \cdot \frac{dr}{dw}$$

So we get for an cylindrical JLFET as,

$$\frac{dV_{TH}}{dw} = -\frac{\mathrm{N_{do}}\exp\left(-\frac{w^2+\mathrm{H}^2}{2}\right)}{(2\pi).L_g}[Z_3+ Z_4] .\frac{w}{\sqrt{w^2+H^2}} \qquad (4.1.13)$$

Eqn. 4.1.13 represents the expression variation of threshold voltage (V_{th}) with respect to channel width(*w*) in cylindrical JLFET for normal dopant distribution.

Similarly we get,

$$\frac{dV_{TH}}{dh} = \frac{dV_{TH}}{dr} \cdot \frac{dr}{dh}$$

So we get for an cylindrical JLFET as,

$$\frac{dV_{TH}}{dh} = -\frac{\mathrm{N_{do}}\exp\left(-\frac{W^2+\mathrm{h}^2}{2}\right)}{(2\pi).L_g}[Z_3+ Z_4] .\frac{h}{\sqrt{W^2+h^2}} \qquad (4.1.14)$$

Eqn. 4.1.14 represents the expression variation of threshold voltage (V_{th}) with respect to channel height(*h*) in cylindrical JLFET for normal dopant distribution.

Using eqns. (3.1.12) , (3.1.22) , (4.1.13) and (4.1.14) we plot the graphs to show the performance analysis of TG-JLFET & Cylindrical JLFET for normal doping profile variation.

B . Linear Dopant Distribution:

From eqn. (4.1.8) and (4.1.9) we get,

$$\frac{dV_{TH}}{dr} = -dN_d(r)[Z_3 + Z_4].r \qquad (4.1.8)$$

and,

$$dN_d(r) = \frac{N_d(r)}{2\pi r.L_g}\delta(r - r_1) \qquad (4.1.9)$$

From eqn. (3.1.13), when the doping profile is varying along the radius*(r)* of the cylindrical JLFET , we get,

$$N_d(r) = \left(\frac{N_{do}}{R_{max}}\right).r - N_{do} \qquad (4.1.15)$$

Using eqn. (4.1.2), and transforming cylindrical into linear co-ordinates, we get,

$$R_{max} = \sqrt{W_{max}^{\,2} + H_{max}^{\,2}} \qquad (4.1.16)$$

where,

R_{max} = maximum possible radius of cylindrical JLFET.

Using eqn. (4.1.16), in eqn. (4.1.15) , we get,

$$N_d(r) = \left(\frac{N_{do}}{\sqrt{W_{max}^{\,2} + H_{max}^{\,2}}}\right).r - N_{do} \qquad (4.1.17)$$

Using eqn. (4.1.17), in eqn. (4.1.9) , we get,

$$dN_d(r) = \frac{(\frac{N_{do}}{\sqrt{W_{max}^2+H_{max}^2}}).r - Ndo}{2\pi r.L_g}\delta(r - r_1) \qquad (4.1.18)$$

Using eqn. (4.1.18), in eqn. (4.1.8) , we get,

$$\frac{dV_{TH}}{dr} = -[\frac{(\frac{N_{do}}{\sqrt{W_{max}^2+H_{max}^2}}).r - Ndo}{2\pi r.L_g}].[Z_3+ Z_4]r \qquad (4.1.19)$$

or,

$$\frac{dV_{TH}}{dr} = [\frac{N_{do} - (\frac{N_{do}}{\sqrt{W_{max}^2+H_{max}^2}}).r}{2\pi.L_g}].[Z_3+ Z_4]$$

or,

$$\frac{dV_{TH}}{dr} = [\frac{N_{do}}{2\pi.L_g}] [1 - (\frac{r}{\sqrt{W_{max}^2+H_{max}^2}})].[Z_3+ Z_4]$$

Using eqn. (4.1.2), in above eqn. , we get,

$$\frac{dV_{TH}}{dr} = [\frac{N_{do}}{2\pi.L_g}].[Z_3+ Z_4].[1 - (\frac{\sqrt{w^2+h^2}}{\sqrt{W_{max}^2+H_{max}^2}})] \qquad (4.1.20)$$

The above expression i.e. eqn. (4.1.20) give the rate of change of V_{TH} with respect to the radius(r) of the cylindrical JLFET in terms of width(w) and height (h) of the TG JLFET when the doping profile variation is linear.This expression is important because using it we can compare the performance analysis of the

above devices under random dopant fluctuation effect for smaller dimensions by simply varying the height and width of both the junctionless transistors.

Similarly solving like eqns. (4.1.13) and (4.1.14) , we get,

$$\frac{dV_{TH}}{dw} = \left[\frac{N_{do}}{2\pi.L_g}\right].[Z_3 + Z_4].\left[1 - \left(\frac{\sqrt{w^2+H^2}}{\sqrt{W_{max}{}^2+H_{max}{}^2}}\right)\right] . \frac{w}{\sqrt{w^2+H^2}}$$

or,

$$\boxed{\frac{dV_{TH}}{dw} = \left[\frac{N_{do}}{2\pi.L_g}\right].[Z_3 + Z_4].\left[\frac{w}{\sqrt{w^2+H^2}} - \left(\frac{w}{\sqrt{W_{max}{}^2+H_{max}{}^2}}\right)\right]} \quad (4.1.21)$$

Eqn. 4.1.21 represents the expression variation of threshold voltage (V_{th}) with respect to channel width(w) in cylindrical JLFET for normal dopant distribution.

Again we get,

$$\frac{dV_{TH}}{dh} = \left[\frac{N_{do}}{2\pi.L_g}\right].[Z_3 + Z_4].\left[1 - \left(\frac{\sqrt{W^2+h^2}}{\sqrt{W_{max}{}^2+H_{max}{}^2}}\right)\right] . \frac{h}{\sqrt{W^2+h^2}}$$

or,

$$\boxed{\frac{dV_{TH}}{dh} = \left[\frac{N_{do}}{2\pi.L_g}\right].[Z_3 + Z_4].\left[\frac{h}{\sqrt{W^2+h^2}} - \left(\frac{h}{\sqrt{W_{max}{}^2+H_{max}{}^2}}\right)\right]} \quad (4.1.22)$$

Eqn. 4.1.22 represents the expression variation of threshold voltage (V_{th}) with respect to channel height(h) in cylindrical JLFET for normal dopant distribution.

Using eqns. (4.1.13) ,(3.1.25) , (4.1.21) and (4.1.22) we plot the graphs to show the performance analysis of TG-JLFET & Cylindrical JLFET for linear doping profile variation.

4.2 Results and Discussion:

A . For Normal Dopant Distribution:

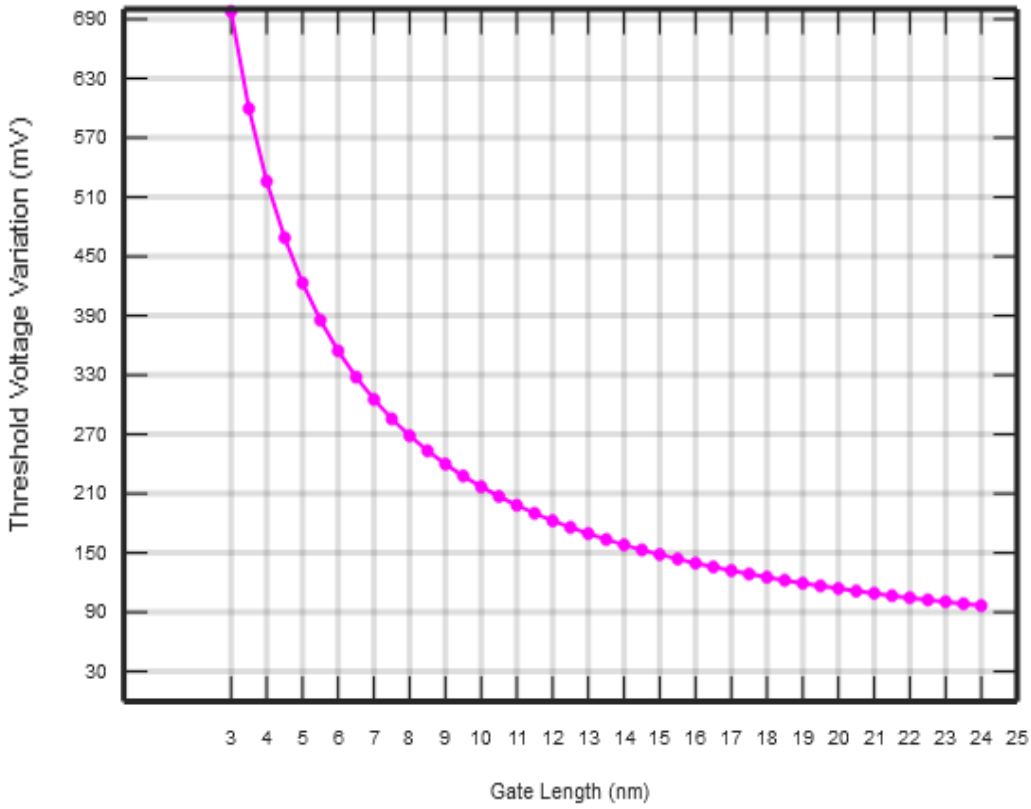


Figure 4.2 V_{th} variation with gate length for *normal doping profile*.

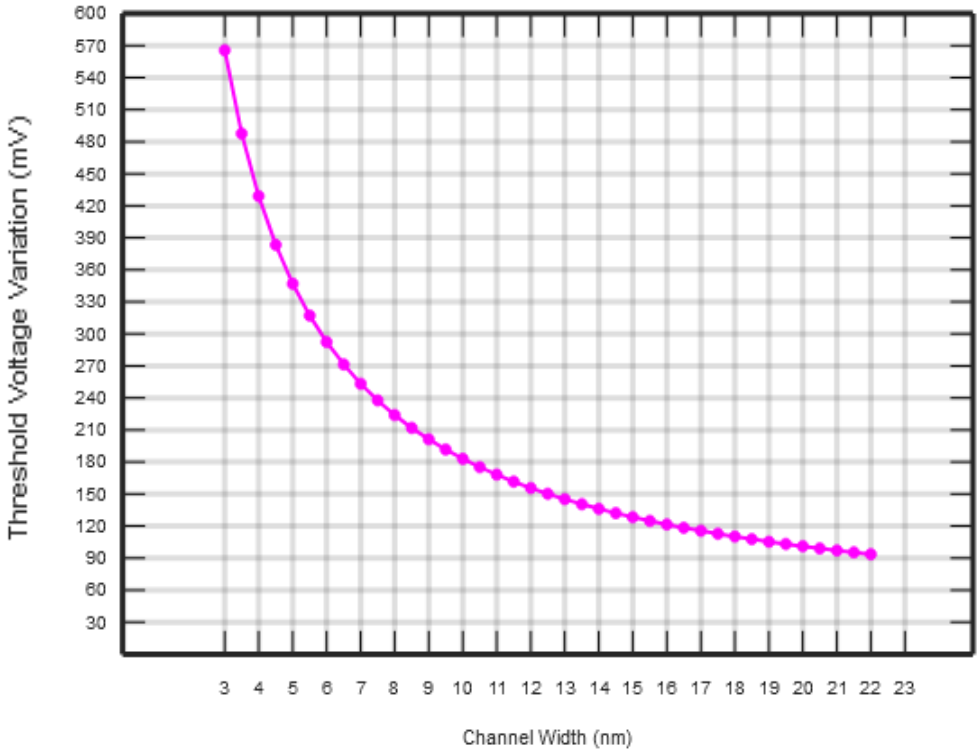


Figure 4.3 V_{th} variation with channel width for *normal doping profile.*

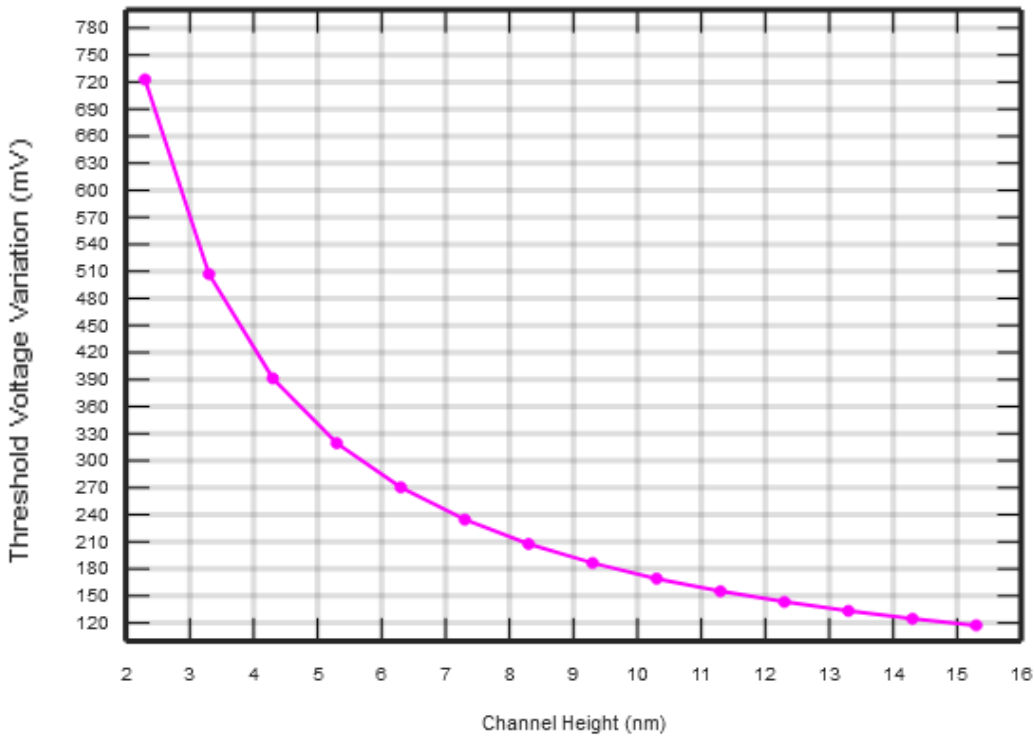


Figure 4.4 V_{th} variation with channel height for *normal doping profile*.

Fig 4.2, fig 4.3, and ***fig 4.4,*** shows the plot of V_{th} variation in cylindrical JLFET with the gate length(L_g), channel width(w) and channel height(h) respectively due to RDF effect for normal dopant distribution. It is evident from the above plot that if we are reducing L_g, w and h i.e. for a short channel the variation of V_{th} is more compared to when L_g, w and h are of larger value. If we compare the above figures with***fig. 3.6, fig. 3.7***and ***fig. 3.8*** side by side, it is clear that due to the structural modification of cylindrical JLFET over TG JLFET, the V_{th} variation is less in former compared to later device. This is due to the fact that fluctuation of dopant atoms is more in a smaller device than a larger device.

B . For Linear Dopant Distribution:

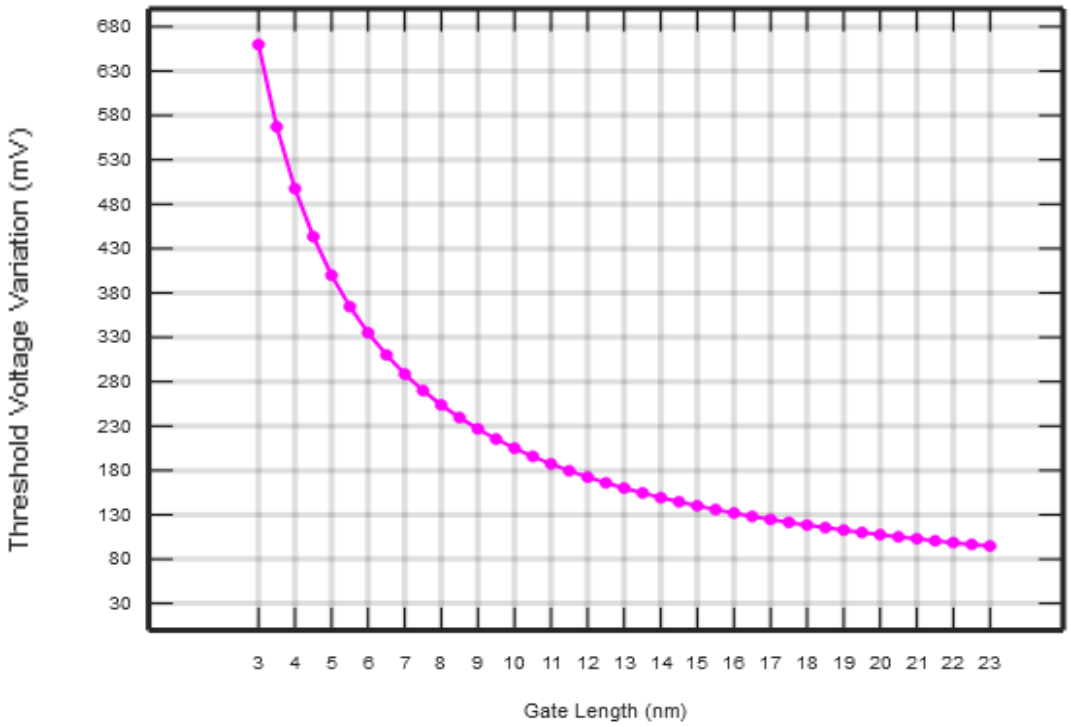


Figure 4.5 V_{th} variation with gate length for *linear doping profile*.

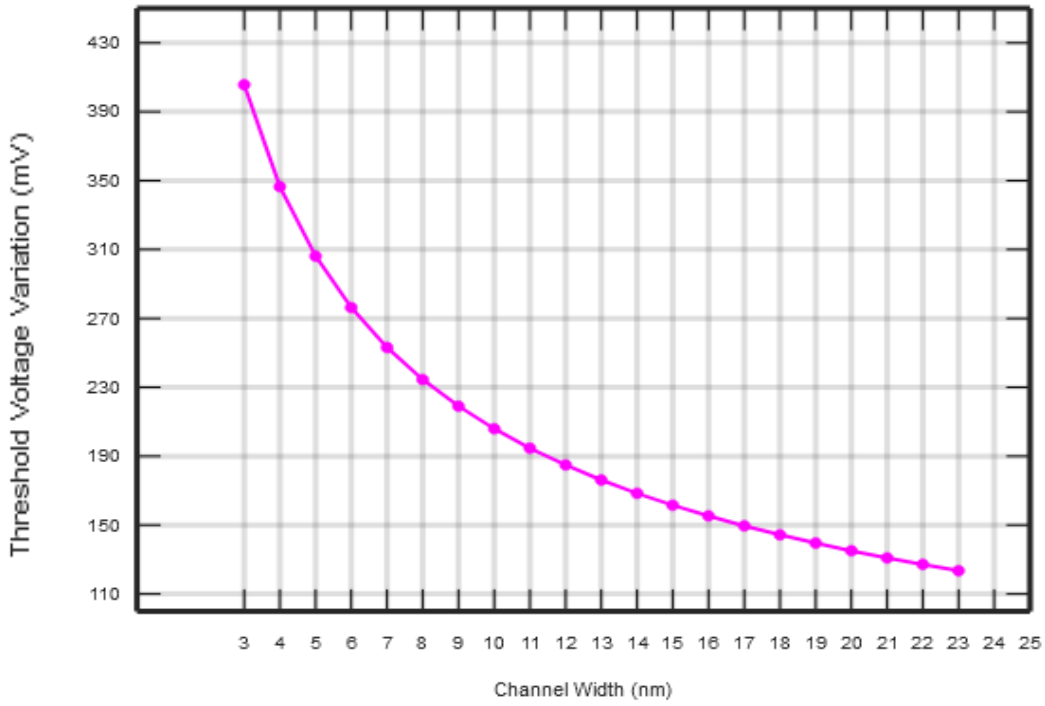


Figure 4.6 V_{th} variation with channel width for *linear doping profile*.

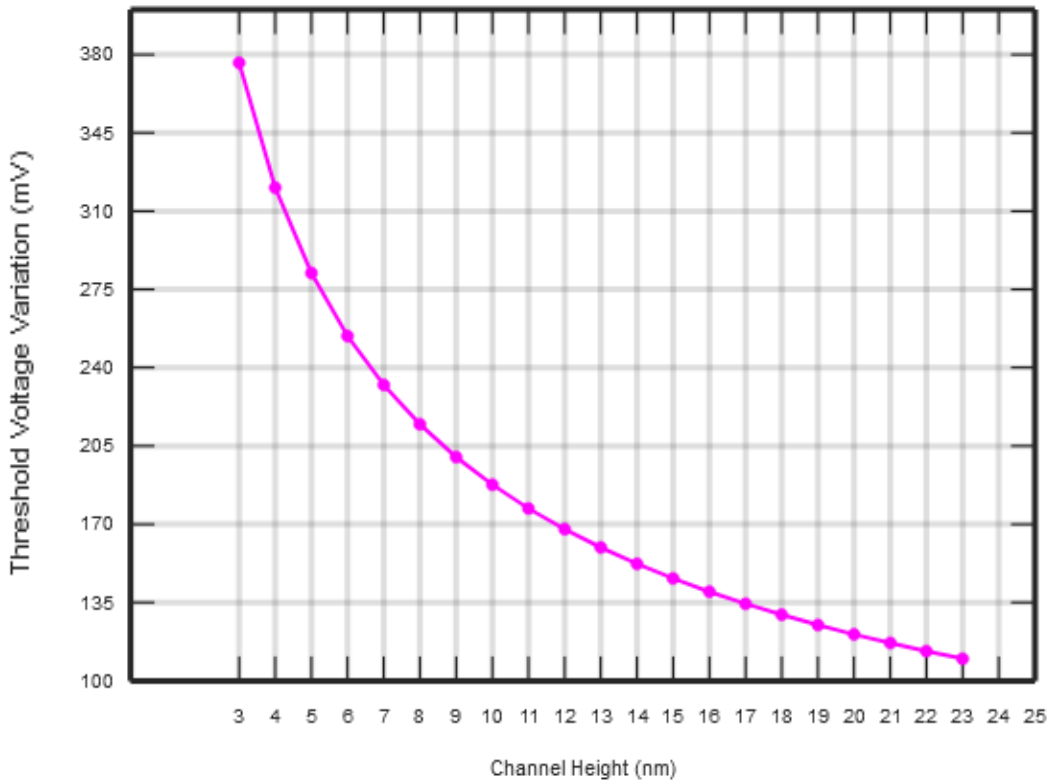


Figure 4.7 V_{th} variation with channel height for *linear doping profile*.

Fig 4.2, fig 4.3, and ***fig 4.4,*** shows the plot of V_{th} variation in cylindrical JLFET with the gate length (***L***$_{g}$), channel width(***w***) and channel height(***h***) respectively due to RDF effect but, instead of normal dopant distribution, here we have used linear dopant distribution. Similar to that of TG JLFET, cylindrical JLFET also produces less magnitude in V_{th} variation with linear dopant distribution compared to that with normal dopant distribution.

4.3 Conclusion:

This chapter deals with the performance analysis of cylindrical JLFET under RDF effect. As done in case of TG JLFET, variation of V_{th} with various channel dimensions such as L_g, w and h are investigated. However, it became evident from this chapter, that the radial channel in cylindrical JLFET provides it an advantage to combat RDF in a more efficient way compared to TG JLFET.

CHAPTER 5

THRESHOLD VOLTAGE VARIATION IN TGJLFET AND CYLINDRICAL JLFET DUE TO RDF IN PRESENCE OF QUANTUM CONFINEMENT

In this chapter, we will study about the additional influence of quantum confinement of carriers on the threshold voltage variation of both TG JLFET and cylindrical JLFET when we shrink the transistor size below ***20nm***.

5.1 Quantum Confinement and its Significance:

Quantum confinement of carriers gives rise to the Quantum Size Effect(QSE). It basically arises when one dimension of a system is reduced to a scale comparable to electron wavelength. The carriers confined in such structures lose their degree of freedom along the reduced dimension; their motion and thereby their momentum get restricted. In order to study the influence of QSE on the behaviour of carriers in a JLFET the channel cross section must be appropriately reduced. In those cases, we can treat the channel as a quantum wire with rectangular cross section in case of TG JLFET and with circular cross section in case of cylindrical JLFET.

When the dimensions of the transistor i.e. the gate length(L_g), height (h) and width(w) are reduced below 10 nm or lower then the electronic property of the semiconductor bulk changes. The most

common problem, the carriers of the transistor(electrons for NMOS and holes for PMOS) suffers from is the quantum confinement effect.

Quantum confinement is defined as the change of electronic as well as the optical properties of the semiconductor crystal when its dimensions are reduced below 10 nm. It is because this effect is observed when the size of the device is too small to be comparable with the wavelength of electron *(= $10^{-11}m$*). For cylindrical JLFET, this quantum confinement effect occurs when the radius of the JLFET becomes comparable to ***Bohr's radius*** (= *$5.291x10^{-11}m$*).

As a result of quantum confinement for a small nano-dimensional mos-transistor, the energy levels inside the bulk are not continuous. These discrete energy states in the bulk is to the occurrence of the finite density of state. The discrete structure of the energy states results in discrete absorption spectrum of nano transistors.

In a quantum confined structure, the carriers are confined in one or more than one directions by the potential barriers. More numbers of discrete levels will arise if more number of directions are confined. So we can also say that because of this effect, the degrees of freedom of the carrier particles reduces.

This effect has no relation with the variation in doping concentration so one may argue that that why we have considered this effect on our thesis. It is because quantum confinement effect has a serious impact on threshold voltage variation for smaller dimensional devices. This causes an exponential rate of change in threshold voltage with reduction in dimensions of the device. In

present day as we are more interested to shrink down the transistor size, this effect plays a great role in our thesis.

The energy level in the conduction band (E_{mn}) due to quantum confinement of carriers is given by,

$$E_{mn} = \frac{\hbar^2 {k_x}^2}{2m_n^*} + \frac{\hbar^2}{2m_n^*}\left[\frac{m^2\pi^2}{a^2} + \frac{n^2\pi^2}{b^2}\right]$$

For ground state energy level ($\mathbf{E_1}$) in the conduction band ***(m=n =1)***, so we get,

$$E_1 = \frac{\hbar^2 {k_x}^2}{2m_n^*} + \frac{\hbar^2}{2m_n^*}\left[\frac{\pi^2}{a^2} + \frac{\pi^2}{b^2}\right]$$

or,

$$\boxed{E_1 = \frac{\hbar^2 k_x}{2m_n^*} + \frac{\hbar^2\pi^2}{2m_n^*}\left[\frac{1}{a^2} + \frac{1}{b^2}\right]}$$

where,

$\frac{\hbar^2 {k_x}^2}{2m_n^*}$ = stationary component of ground state energy level.

$\frac{\hbar^2\pi^2}{2m_n^*}\left[\frac{1}{a^2} + \frac{1}{b^2}\right]$ = varying component of ground state energy level.

k_x = wave number along the channel length.

m,n = 1,2,3,..... are the size quantum numbers.

a,b = dimensions of the semiconductor.

5.2 Normal Dopant Distribution with Quantum Confinement:

5.2.1 Quantum Confinement in TG – JLFET:

In presence of quantum confinement, the variation in the ground energy level in the conduction band (ΔE_o) for an electron by referring the equation as mentioned above is given by,

$$\Delta E_o = \frac{\pi^2 \hbar^2}{2m_n^*}\left[\frac{1}{h^2} + \frac{1}{w^2}\right] \qquad (5.1)$$

where,

$\hbar$ = normalized planck's constant,

m_n^* = effective mass of electron = $1.1m_o$,

m_o = free electron mass,

w , h = width and height of TG – JLFET respectively.

Also it is important to note from the above expression that the energy level variation in the conduction band (ΔE_o) is independent of the gate length (L_g) of the device.

A . Dopant distribution is along the channel width in TG – JLFET:

From eqn. (3.1.8) , we get the expression of threshold voltage as,

$$V_{TH} = V_{FB} - N_d(w)\left[Z_1(wH) + Z_2\left[\frac{wH}{2H+w}\right]^2\right]$$

The above eqn. will be modified as we add one extra term due to quantum confinement as,

$$V_{TH} = V_{FB} - N_d(w)[\, Z_1(wH) + Z_2[\frac{wH}{2H+w}]^2] + \frac{\pi^2\hbar^2}{2qm_n^*}\,[\frac{1}{H^2} + \frac{1}{w^2}]$$

(5.2)

The term arises due to minimum energy level variation in conduction band because of quantum confinement of carriers. We used a term **q** in denominator because to convert energy variation from electron-volts to volts.

Now determining the rate of change of threshold voltage variation with width(***w***) of the TG JLFET under the confiment of carriers, we get,

Using eqn. (3.1.12) we simplify eqn. (5.2) as,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}\exp(-\frac{w^2}{2})}{w.Lg}\,[Z_1.H + Z_2.\{(\frac{4wH^3}{(2H+w)^3})\}] + \frac{d}{dw}[\frac{\pi^2\hbar^2}{2qm_n^*}\,[\frac{1}{H^2} + \frac{1}{w^2}]]$$

or,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}\exp(-\frac{w^2}{2})}{w.Lg}\,[Z_1.H + Z_2.\{(\frac{4wH^3}{(2H+w)^3})\}] + \frac{\pi^2\hbar^2}{\cancel{2}qm_n^*}\,[-\frac{\cancel{2}}{w^3}]$$

or,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}\exp(-\frac{w^2}{2})}{w.Lg}\,[Z_1.H + Z_2.\{(\frac{4wH^3}{(2H+w)^3})\}] - \frac{\pi^2\hbar^2}{qm_n^*w^3}$$

or,

$$\frac{dV_{TH}}{dw} = -[\frac{N_{do}\exp(-\frac{w^2}{2})}{w.Lg}\,[Z_1.H + Z_2.\{(\frac{4wH^3}{(2H+w)^3})\}] + \frac{\pi^2\hbar^2}{qm_n^*w^3}]$$

or,

$$\frac{dV_{TH}}{dw} = -\left[\frac{N_{do}\exp\left(-\frac{w^2}{2}\right)}{w.Lg}\left[Z_1.H + Z_2.\left\{\left(\frac{4wH^3}{(2H+w)^3}\right)\right\}\right] + \frac{Z_5}{w^3}\right] \quad (5.3)$$

where, $Z_5 = \pi^2\hbar^2/qm_n^*$

Eqn. (5.3) gives the rate of change of threshold voltage V_{TH} with channel width(*w*) for TGJLFET, under *normal dopant distribution* when the carriers suffers from quantum confinement.

As dV_{TH}/dw is inversely proportional to ***w³*** so we can say that the quantum confinement effect plays a very significant role in threshold voltage fluctuation when the width of the transistor is shrinked to a very small size.

B . Dopant distribution is along the channel height in TG – JLFET:

From eqn. (3.1.18) , we get the expression of threshold voltage as,

$$V_{TH} = V_{FB} - N_d(h)\left[Z_1(W.h) + Z_2.\left[\frac{Wh}{2h+W}\right]^2\right]$$

The above eqn. will be modified as we add one extra term due to quantum confinement as,

$$V_{TH} = V_{FB} - N_d(h)\left[Z_1(W.h) + Z_2.\left[\frac{Wh}{2h+W}\right]^2\right] + \frac{\pi^2 {h_p}^2}{2qm_n^*}\left[\frac{1}{h^2} + \frac{1}{W^2}\right] \quad (5.4)$$

Now determining the rate of change of threshold voltage variation with height(***h***) for the TG JLFET under the confinement of carriers, we get,

Using eqn. (3.1.22) we simplify eqn. (5.4) as,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{d}{dh}\left[\frac{\pi^2 {h_p}^2}{2qm_n^*}\left[\frac{1}{h^2}+\frac{1}{W^2}\right]\right]$$

or,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{\pi^2 {h_p}^2}{\cancel{2}qm_n^*}\left[-\frac{\cancel{2}}{h^3}\right]$$

or,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] - \frac{\pi^2 {h_p}^2}{qm_n^* h^3}$$

or,

$$\frac{dV_{TH}}{dh} = -\left[\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{\pi^2 {h_p}^2}{qm_n^* h^3}\right]$$

or,

$$\frac{dV_{TH}}{dh} = -\left[\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{\pi^2 {h_p}^2}{qm_n^* h^3}\right]$$

or,

$$\boxed{\frac{dV_{TH}}{dh} = -\left[\frac{N_{do}\exp(-\frac{h^2}{2})}{Lg}\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{Z_5}{h^3}\right]} \quad (5.5)$$

Eqn. (5.5) gives the rate of change of threshold voltage V_{TH} with channel height(*h*) for TGJLFET, under *normal dopant distribution* when the carriers suffers from quantum confinement.

As $^{dV_{TH}}/_{dh}$ is inversely proportional to h^3 so we can say that the quantum confinement effect plays a very significant role in threshold voltage fluctuation when the height of the transistor is shrinked to a very small value.

Important Note:

Here we have not considered $^{dV_{TH}}/_{dL_g}$ i.e. rate of change of threshold voltage with gate length, because neither V_{TH} nor ΔE_o is directly proportional to L_g so their derivatives with respect to L_g will give result as 0. However, $^{dV_{TH}}/_{dw}$ as well as $^{dV_{TH}}/_{dh}$ are both proportional to $^{1}/_{L_g}$ thereby, we plot dV_{TH} with respect to w and h with L_g as a parameter.

5.2.2 Quantum Confinement in Cylindrical JLFET:

C . Dopant distribution is along the channel radius in Cylindrical JLFET:

In presence of quantum confinement, the variation in the ground energy level in the conduction band (ΔE_o) for an electron in cylindrical JLFET can be written as,

$$\Delta E_o = \frac{\pi^2\hbar^2}{2m_n^*}\left[\frac{1}{(r.\sin\Phi)^2} + \frac{1}{(r.\cos\Phi)^2}\right]$$

or,

$$\Delta E_o = \frac{\pi^2\hbar^2}{2m_n^*}\left[\frac{(r.\sin\Phi)^2+(r.\cos\Phi)^2}{(r.\sin\Phi)^2.(r.\cos\Phi)^2}\right]$$

or,

$$\Delta E_o = \frac{\pi^2\hbar^2}{2m_n^*}\left[\frac{(r^2\{(\sin\Phi)^2+(\cos\Phi)^2\}}{(r.\sin\Phi)^2.(r.\cos\Phi)^2}\right]$$

or,

$$\Delta E_o = \frac{\pi^2\hbar^2}{2m_n^*}\left[\frac{r^2}{r^4.(\sin\Phi)^2.(\cos\Phi)^2}\right]$$

$$\left[\because (\sin\Phi)^2 + (\cos\Phi)^2 = 1\right]$$

or,

$$\boxed{\Delta E_o = \frac{\pi^2\hbar^2}{2m_n^*}\left[\frac{1}{r^2.(\sin\Phi)^2.(\cos\Phi)^2}\right]} \qquad (5.6)$$

Now differentiating eqn. (5.6) with respect to ***r*** **,** we get,

$$\frac{d(\Delta Eo)}{dr} = \frac{\pi^2\hbar^2}{\cancel{2}m_n^*}\left[-\frac{\cancel{2}}{r^3.(\sin\Phi)^2.(\cos\Phi)^2}\right]$$

or,

$$\frac{d(\Delta Eo)}{dr} = - \frac{\pi^2 \hbar^2}{m_n^*} \left[\frac{1}{r^3.(\sin\Phi)^2.(\cos\Phi)^2}\right] \qquad (5.7)$$

Now transforming cylindrical co-ordinates into linear co-ordinates to ease the comparison between performance of TG JLFET and cylindrical JLFET , we get,

Using eqns. (4.1.2) and (4.1.4) in eqn (5.7) , we get,

$$\frac{d(\Delta Eo)}{dr} = - \frac{\pi^2 \hbar^2}{m_n^*} \left[\frac{1}{(\sqrt{w^2+h^2})^3.(h/\sqrt{w^2+h^2})^2.(w/\sqrt{w^2+h^2})^2}\right]$$

or,

$$\frac{d(\Delta Eo)}{dr} = - \frac{\pi^2 \hbar^2}{m_n^*} \left[\frac{(\sqrt{w^2+h^2})^4}{(\sqrt{w^2+h^2})^3.(w.h)^2}\right]$$

or,

$$\boxed{\frac{d(\Delta Eo)}{dr} = - \frac{\pi^2 \hbar^2}{m_n^*} \left[\frac{\sqrt{w^2+h^2}}{(w.h)^2}\right]} \qquad (5.8)$$

Again from eqn. (4.1.11) , we get the expression of variation of threshold voltage with radius for a cylindrical JLFET as,

$$\frac{dV_{TH}}{dr} = - \frac{N_{do}\exp(-\frac{w^2+h^2}{2})}{(2\pi).L_g} [Z_3 + Z_4]$$

Adding eqn. (5.8) to the above eqn. because of quantum confinement effect, we get,

$$\frac{dV_{TH}}{dr} = - \frac{N_{do}\exp(-\frac{w^2+h^2}{2})}{(2\pi).L_g} [Z_3 + Z_4] - \frac{\pi^2 {h_p}^2}{q m_n^*} \left[\frac{\sqrt{w^2+h^2}}{(w.h)^2}\right]$$

or,

$$\frac{dV_{TH}}{dr} = -\frac{N_{do}\exp(-\frac{w^2+h^2}{2})}{(2\pi).L_g}[Z_3+Z_4] - Z_5.[\frac{\sqrt{w^2+h^2}}{(w.h)^2}]$$

or,

$$\boxed{\frac{dV_{TH}}{dr} = -[\frac{N_{do}\exp(-\frac{w^2+h^2}{2})}{(2\pi).L_g}[Z_3+Z_4] + Z_5.[\frac{\sqrt{w^2+h^2}}{(w.h)^2}]]} \quad (5.9)$$

Eqn. (5.9) gives the rate of change of threshold voltage V_{TH} with channel radius(*r*) of cylindrical JLFET, under *normal dopant distribution* when the carriers suffers from quantum confinement.

As $dV_{TH}/_{dr}$ is inversely proportional to r^3 so we can say that the quantum confinement effect plays a very significant role in threshold voltage fluctuation when the radius of the transistor is reduced to a very small value.

Again from eqn. (4.1.12) , we get,

$$\frac{dr}{dw} = \frac{w}{\sqrt{w^2+H^2}}$$

and, $$\frac{dr}{dh} = \frac{h}{\sqrt{W^2+h^2}}$$

Again from chain rule of differential calculus, we know that,

$$\frac{dV_{TH}}{dw} = \frac{dV_{TH}}{dr} \cdot \frac{dr}{dw}$$

So we get for an cylindrical JLFET as,

$$\frac{dV_{TH}}{dw} = -\left[\frac{N_{do}\exp\left(-\frac{w^2+H^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] + Z_5.\left[\frac{\sqrt{w^2+H^2}}{(w.H)^2}\right]\right] . \frac{w}{\sqrt{w^2+H^2}}$$

or,

$$\frac{dV_{TH}}{dw} = -\frac{N_{do}\exp\left(-\frac{w^2+H^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] . \frac{w}{\cancel{\sqrt{w^2+H^2}}} - Z_5.\left[\frac{\cancel{\sqrt{w^2+H^2}}}{(w.H)^2}\right] . \frac{w}{\sqrt{w^2+H^2}}$$

or,

$$\boxed{\frac{dV_{TH}}{dw} = -\left[\frac{N_{do}\exp\left(-\frac{w^2+H^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] . \frac{w}{\sqrt{w^2+H^2}}\right] - Z_5.\left[\frac{1}{w.H^2}\right]} \quad (5.10)$$

Similarly we get,

$$\frac{dV_{TH}}{dh} = \frac{dV_{TH}}{dr} . \frac{dr}{dh}$$

So we get for an cylindrical JLFET as,

$$\frac{dV_{TH}}{dr} = -\left[\frac{N_{do}\exp\left(-\frac{W^2+h^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] + Z_5.\left[\frac{\sqrt{W^2+h^2}}{(W.h)^2}\right]\right] . \frac{h}{\sqrt{W^2+h^2}}$$

or,

$$\frac{dV_{TH}}{dh} = -\frac{N_{do}\exp\left(-\frac{W^2+h^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] . \frac{h}{\sqrt{W^2+h^2}} - Z_5.\left[\frac{\cancel{\sqrt{W^2+h^2}}}{(W.h)^2}\right] . \frac{h}{\cancel{\sqrt{W^2+h^2}}}$$

or,

$$\boxed{\frac{dV_{TH}}{dh} = -\left[\frac{N_{do}\exp\left(-\frac{W^2+h^2}{2}\right)}{(2\pi).L_g}\left[Z_3+Z_4\right] . \frac{h}{\sqrt{W^2+h^2}}\right] - Z_5.\left[\frac{\mathbf{1}}{h.W^2}\right]}$$

(5.11)

The *eqns. (5.10) & (5.11)* gives the rate of change of threshold voltage V_{TH} in terms of channel width(*w*) and channel height(*h*) respectively for a cylindrical JLFET, under *normal dopant distribution* when the carriers suffers from quantum confinement.

Using eqns. (5.3) , (5.5) , (5.10) and (5.11) we plot the graphs to show the performance analysis of TG-JLFET & Cylindrical JLFET for normal doping profile variation with quantum confinement effect of carriers inside semiconductor bulk.

5.3 Linear Dopant Distribution with Quantum Confinement:

As quantum confinement of carriers is only dependent on the dimensions of the transistors and not on the doping profile variation so can directly write as,

Using eqns. (3.1.16), (3.1.22), (4.1.21), (4.1.22) and also using eqns. (5.3) , (5.5) , (5.10), (5.11) , we get,

A . For TG – JLFET*:*

$$\frac{dV_{TH}}{dw} = -\left[\frac{N_{do}}{L_g}.\left[\frac{1}{w} - \frac{1}{W_{max}}\right].\left[Z_1.H + Z_2\left\{\left(\frac{4wH^3}{(2H+w)^3}\right)\right\}\right] + \frac{Z_5}{w^3}\right] \quad (5.12)$$

Eqn. (5.12) gives the rate of change of threshold voltage V_{TH} with channel width(*w*) for TG-JLFET, under *linear dopant distribution* when the carriers suffers from quantum confinement.

and,

$$\frac{dV_{TH}}{dh} = -\left[\frac{N_{do}}{L_g}.\left[1 - \frac{h}{H_{max}}\right].\left[Z_1 + Z_2.\left\{\frac{2hW^2}{(2h+W)^3}\right\}\right] + \frac{Z_5}{h^3}\right] \quad (5.13)$$

Eqn. (5.13) gives the rate of change of threshold voltage V_{TH} with channel height(*h*) for TG-JLFET, under *linear dopant distribution* when the carriers suffers from quantum confinement.

B . For Cylindrical JLFET*:*

$$\frac{dV_{TH}}{dr} = \left[\frac{N_{do}}{2\pi.L_g}\right].\left[Z_3 + Z_4\right].\left[1 - \left(\frac{\sqrt{\boldsymbol{w^2+h^2}}}{\sqrt{\boldsymbol{W_{max}}^2+\boldsymbol{H_{max}}^2}}\right)\right] - Z_5.\left[\frac{\sqrt{w^2+h^2}}{(w.h)^2}\right] \quad (5.14)$$

Eqn. (5.14) gives the rate of change of threshold voltage V_{TH} with channel radius(*r*) of cylindrical JLFET, under *linear dopant distribution* when the carriers suffers from quantum confinement.

$$\frac{dV_{TH}}{dw} = \left[\frac{N_{do}}{2\pi.L_g}\right].\left[Z_3 + Z_4\right].\left[\frac{w}{\sqrt{w^2+H^2}} - \left(\frac{\boldsymbol{w}}{\sqrt{\boldsymbol{W_{max}}^2+\boldsymbol{H_{max}}^2}}\right)\right] - Z_5.\left[\frac{1}{w.H^2}\right] \quad (5.15)$$

$$\frac{dV_{TH}}{dh} = \left[\frac{N_{do}}{2\pi.L_g}\right].\left[Z_3 + Z_4\right].\left[\frac{h}{\sqrt{W^2+h^2}} - \left(\frac{\boldsymbol{h}}{\sqrt{\boldsymbol{W_{max}}^2+\boldsymbol{H_{max}}^2}}\right)\right] - Z_5.\left[\frac{\mathbf{1}}{h.W^2}\right] \quad (5.16)$$

The *eqns. (5.15) & (5.16)* gives the rate of change of threshold voltage V_{TH} in terms of channel width(*w*) and channel height(*h*) respectively for a cylindrical JLFET, under *linear dopant distribution* when the carriers undergo quantum confinement.

Using eqns. (5.12) , (5.13) , (5.15) and (5.16) we plot the graphs to show the performance of TG-JLFET & Cylindrical JLFET for linear doping profile variation in presence of quantum confinement of carriers.

5.4 Results and Discussion:

A . For Normal Dopant Distribution:

Considering TG JLFET:

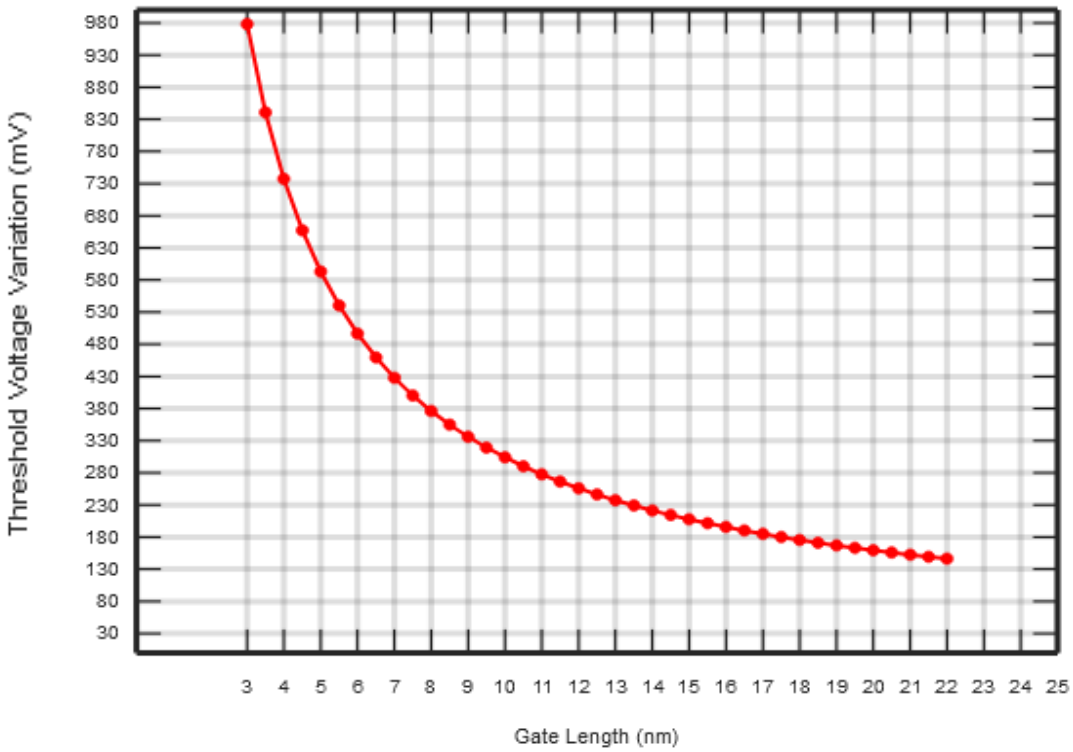


Figure 5.1 V_{th} variation with gate length for *normal doping profile and quantum confinement*.

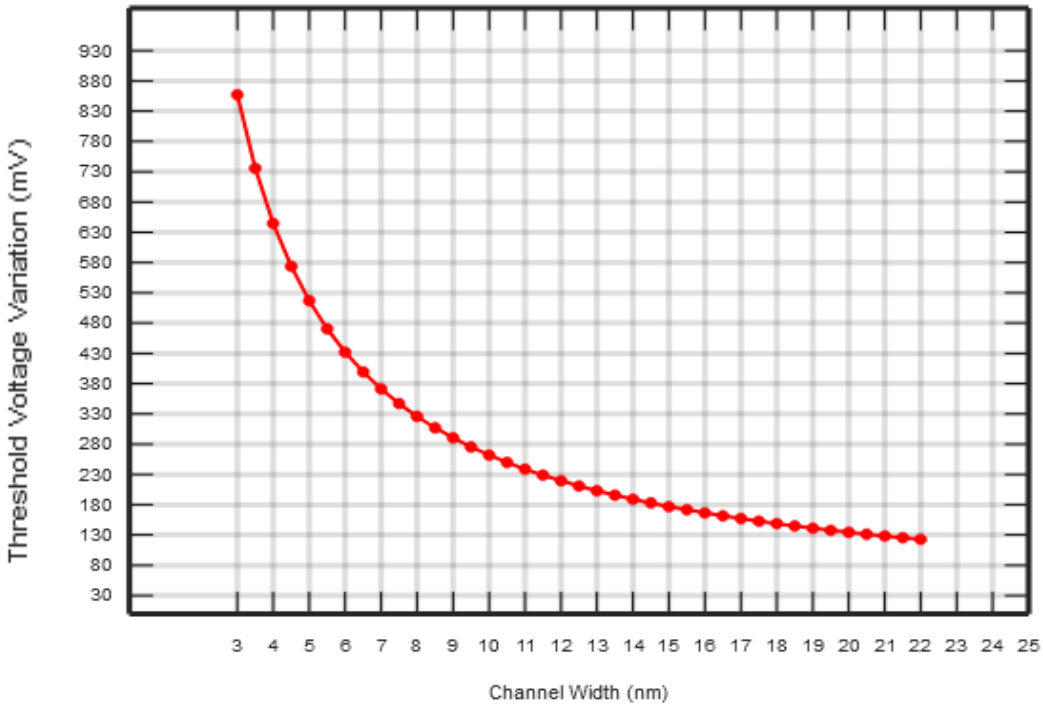


Figure 5.2 V_{th} variation with channel width for *normal doping profile and quantum confinement*.

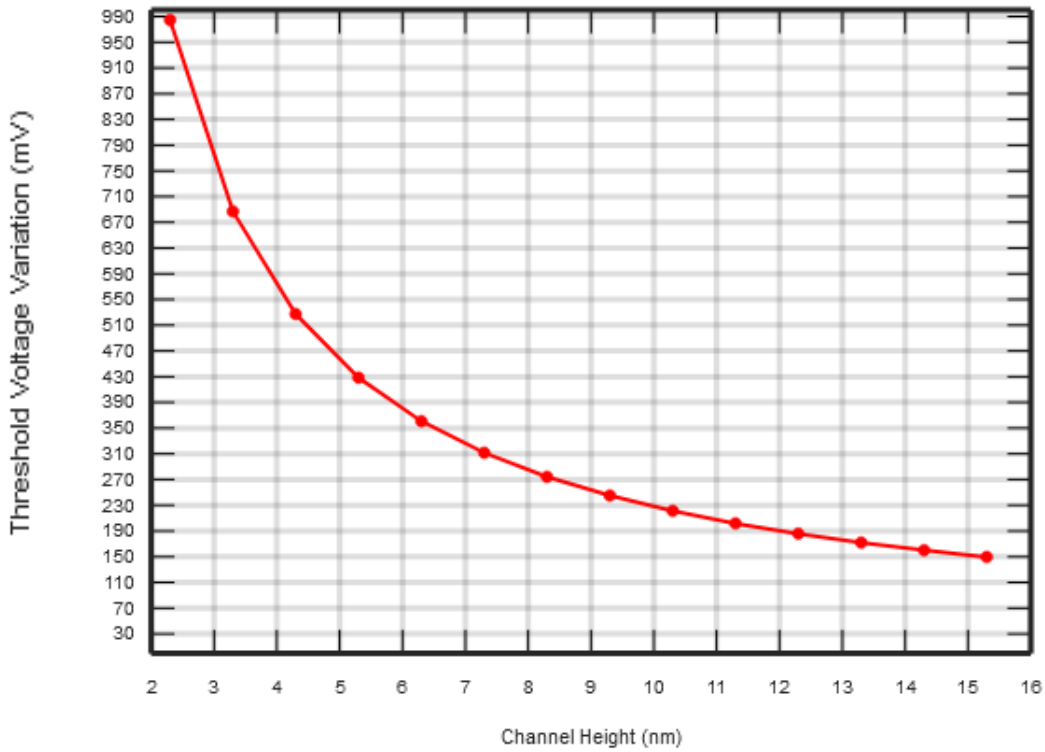


Figure 5.3 V_{th} variation with channel height for *normal doping profile and quantum confinement*.

Fig 5.1, ***fig 5.2*** and ***fig 5.3*** illustrates the plot of V_{th} variation with the gate length(L_g), channel width(w), and channel height(h) respectively for a TG JLFET due to RDF effect and quantum confinement with normal dopant distribution. It is evident from the above figures that the quantum confinement effect doesnot changes the shape of the graphs as it is independent of the dopant distribution. The QSE only depends upon the dimensions of the channel so the magnitude of variation of V_{th} with QSE is superimposed on the magnitude of variation of V_{th} due to RDF effect so, the overall variation of V_{th} increases more rapidly with reduced dimensions.

Considering Cylindrical JLFET:

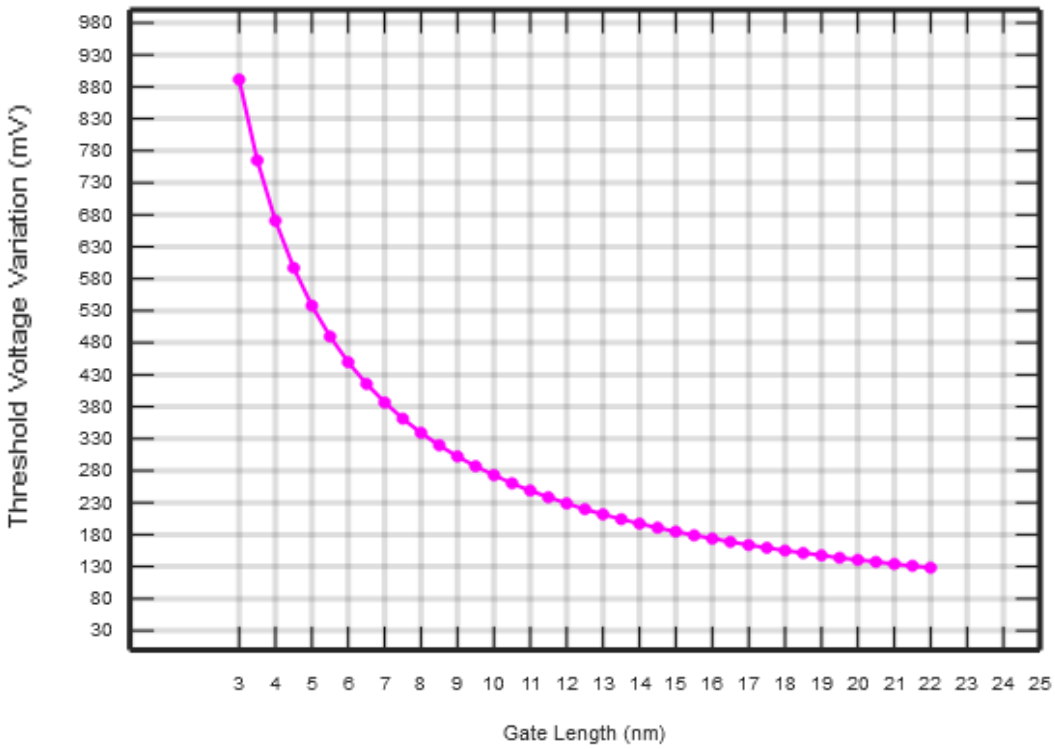


Figure 5.4 V_{th} variation with gate length for *normal doping profile and quantum confinement*.

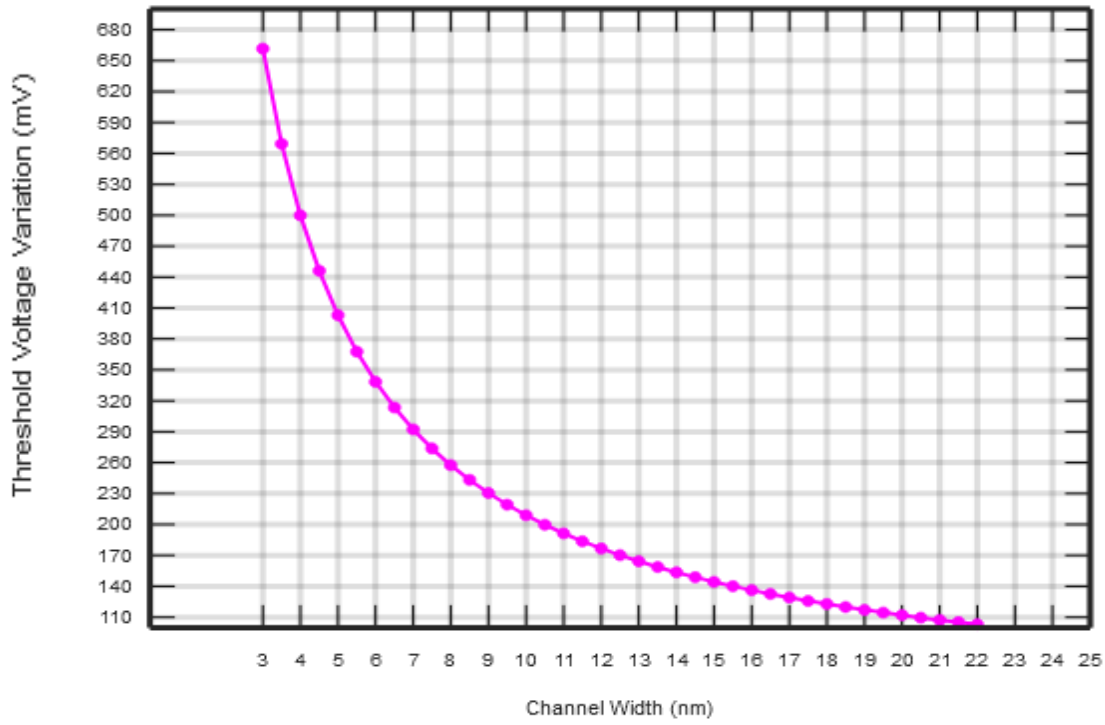


Figure 5.5 V_{th} variation with channel width for *normal doping profile and quantum confinement*.

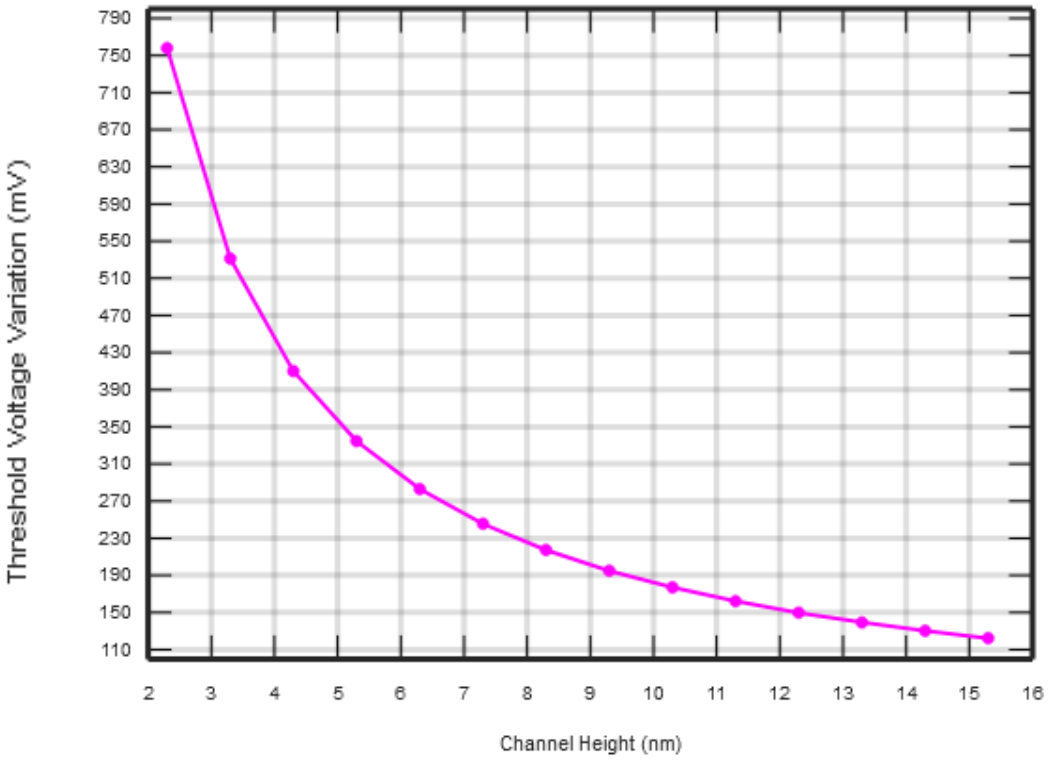


Figure 5.6 V_{th} variation with channel height for *normal doping profile and quantum confinement*.

Fig 5.4, ***fig 5.5*** and ***fig 5.6*** illustrates the plot of V_{th} variation with the gate length(L_g), channel width(w), and channel height(h) respectively for a cylindrical JLFET due to RDF effect and quantum confinement with normal dopant distribution. It is clear from the plot that the radial structure of cylindrical JLFET gives it an edge over TG JLFET to provide better performance in presence of RDF and QSE, as it provides less V_{th} variation comapred to its linear counterpart.

B . For Linear Dopant Distribution:

Considering TG JLFET:

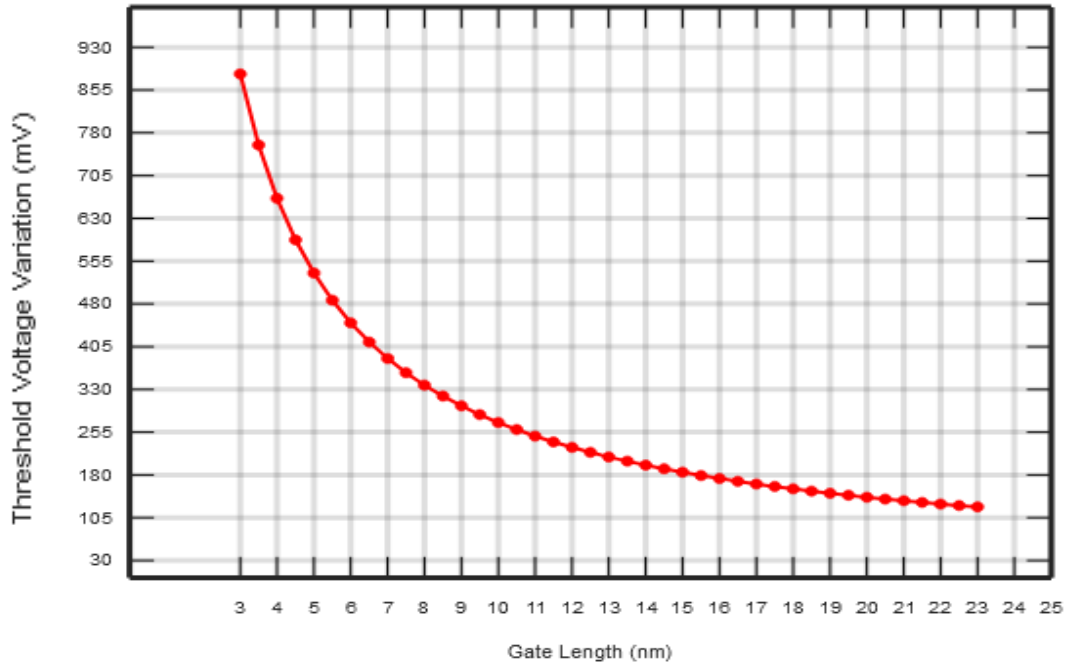


Figure 5.7 V_{th} variation with gate length for *linear doping profile and quantum confinement*.

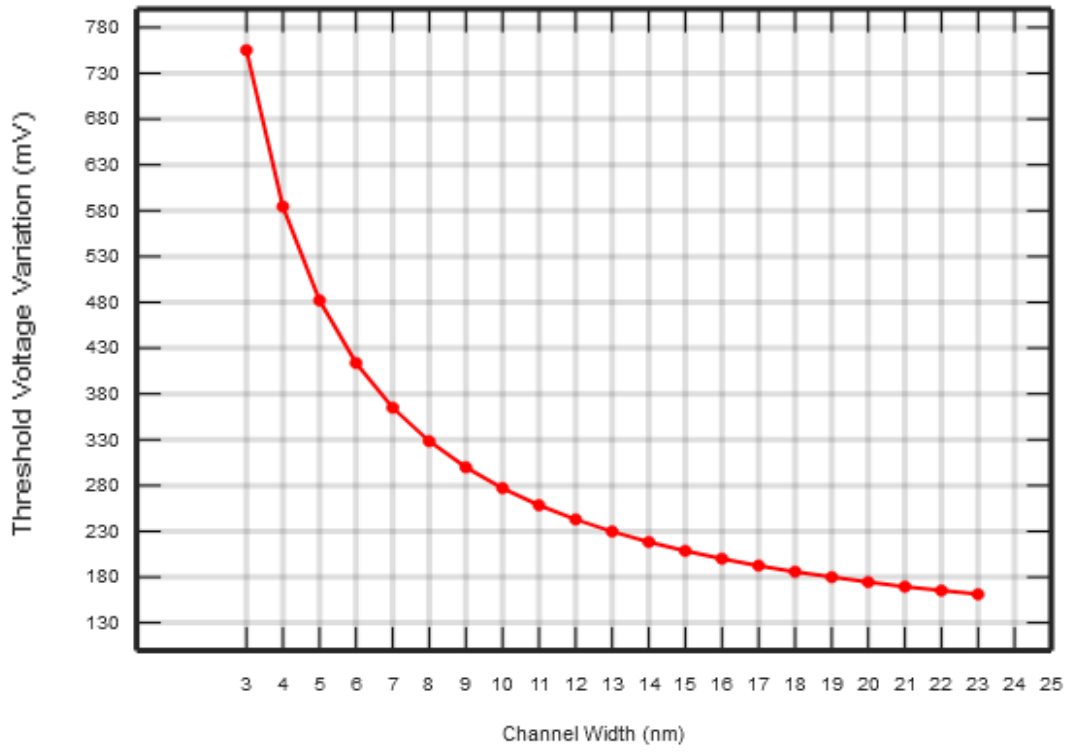


Figure 5.8 V_{th} variation with channel width for *linear doping profile and quantum confinement*.

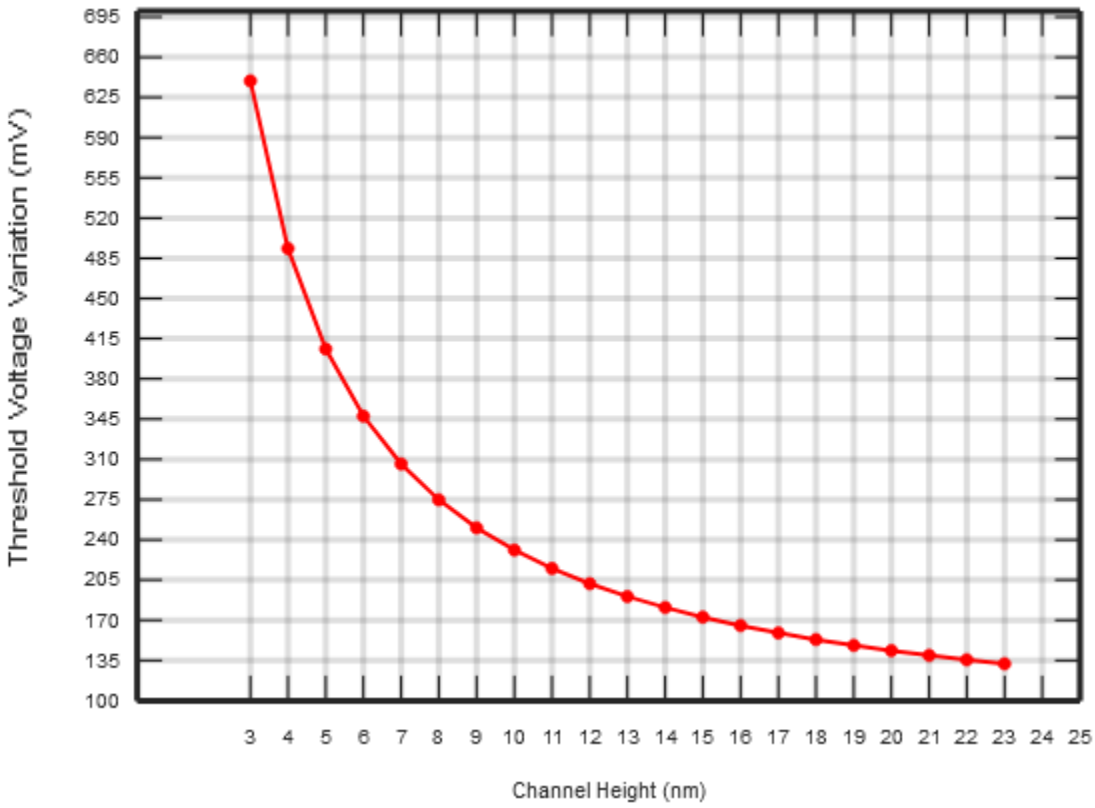


Figure 5.9 V_{th} variation with channel height for *linear doping profile and quantum confinement*.

Fig 5.7, ***fig 5.8*** and ***fig 5.9*** illustrates the plot of V_{th} variation with the gate length(L_g), channel width(w), and channel height(h) respectively for a TG JLFET due to RDF effect and quantum confinement with linear dopant distribution. The explanation of the figures is same as that with normal dopant distribution and has already been done above. The effect of QSE on magnitude of V_{th} variation remains same as normal dopant distribution as QSE is independent of type of dopant distribution. However, the overall magnitude of V_{th} variation in linear dopant distribution is less compared to normal dopant distribution because the effect of RDF is minimal in former compared to latter.

Considering Cylindrical JLFET:

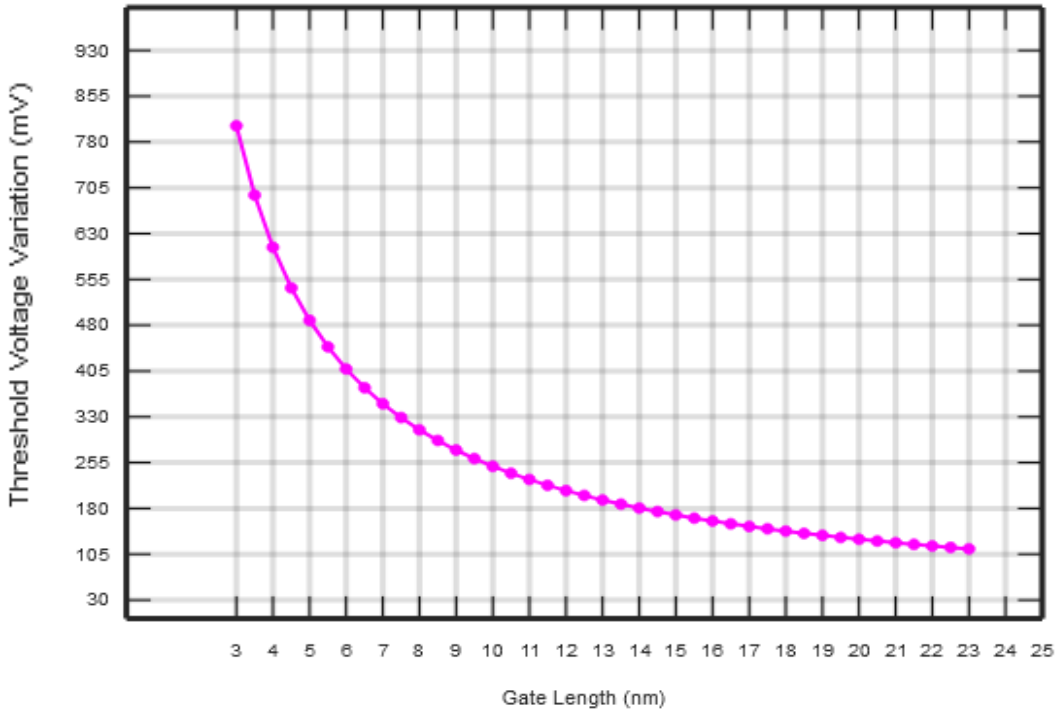


Figure 5.10 V_{th} variation with gate length for *linear doping profile and quantum confinement*.

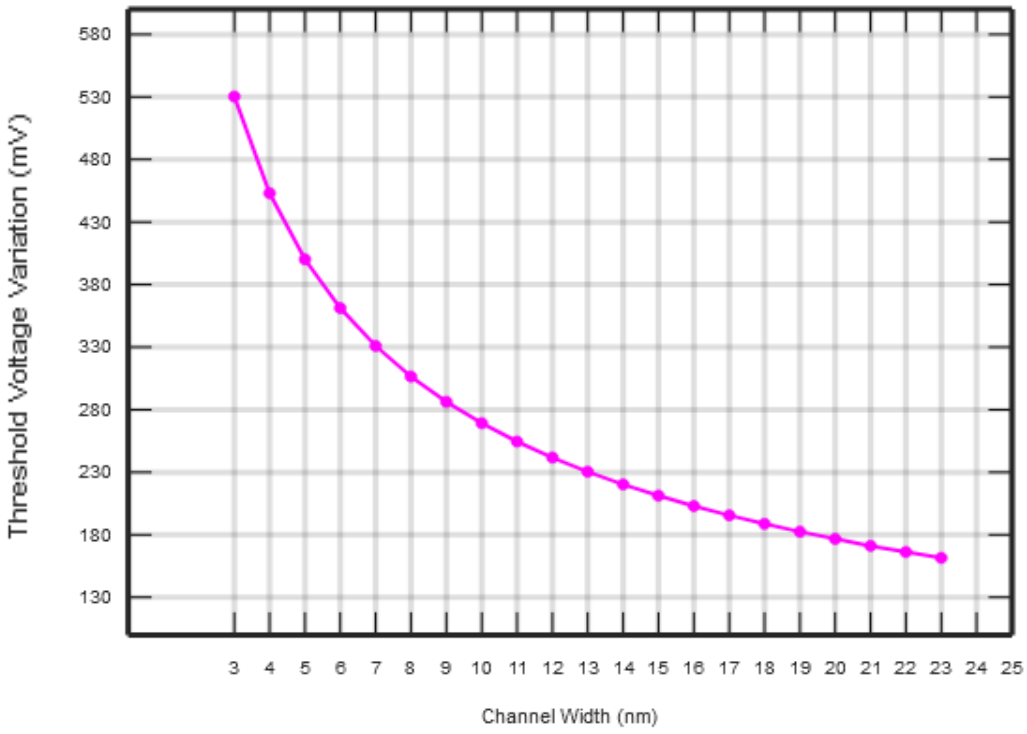


Figure 5.11 V_{th} variation with channel width for *linear doping profile and quantum confinement*.

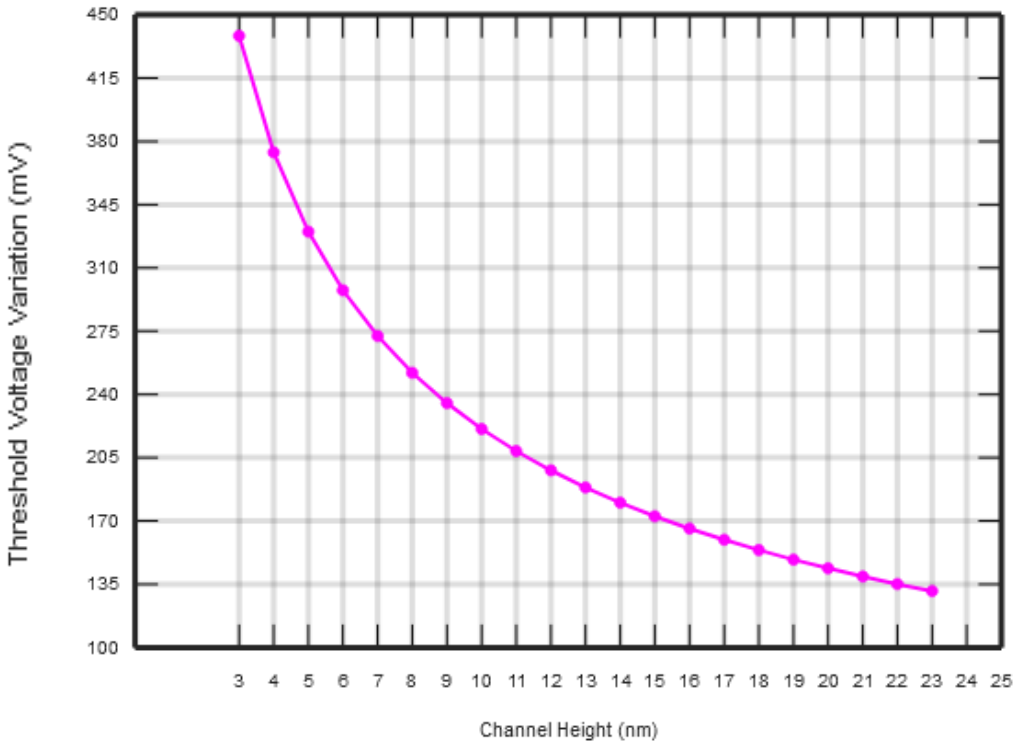


Figure 5.12 V_{th} variation with channel height for *linear doping profile and quantum confinement*.

Fig 5.10, ***fig 5.11*** and ***fig 5.12*** illustrates the plot of V_{th} variation with the gate length($\boldsymbol{L_g}$), channel width($\boldsymbol{w}$), and channel height($\boldsymbol{h}$) respectively for a cylindrical JLFET due to effect of RDF and quantum confinement respectively with linear dopant distribution. The explanation of the figures is same as that with normal dopant distribution and has already been done above. The cylindrical JLFET always provides less V_{th} variation along all the channel dimensions under the influence of RDF and QSE because of its radial structure which provides better electrostatic control compared to TG JLFET.

5.5 Conclusion:

In this chapter, another phenomenon along with RDF named as Quantum Size Effect(QSE) is introduced, which causes quantum confinement of carriers. The effect arises due to drastic reduction of channel dimensions as a result of device scaling. It gives the clear idea about the choice of device architecture in ICs which requires aggressive scaling for providing better performance.

CHAPTER 6

COMPARISON OF THRESHOLD VOLTAGE VARIATION IN TG JLFET AND CYLINDRICAL JLFET DUE TO RDF

In this chapter, the results obtained in chapter 3 to 5 related to the threshold voltage variations due to RDF in a TG JLFET (FINFET) and a Cylindrical (GAA) JLFET are compared. It is important to note that in the entire analysis all the devices are considered to have n- type channel, and so the donor used as dopants with a value $N_{do} = 1.125x10^{19}\ cm^{-3}$. We are much more interested to analyze short channel devices and the impact of RDF on their V_{th} variation in the quantum regime.

JLFETs investigated in the present thesis can be used as the basic building block of CMOS used in industry. The fundamental operation of CMOS is to work as an inverter, and we know that to operate as an inverter the (W/L) ratio of the transistor should be unity. Therefore we have considered, the variation range of L_g = variation range of *w.* Here both L_g and *w* are varied from 3 to 22nm. The channel height is varied in the range of 2.3 to 16 nm. Again it is important to note that we have considered an assymetric TG JLFET with (***w>h***). Further, as we have radius of cylindrical JLFET $\boldsymbol{r = \sqrt{w^2 + h^2}}$, the range of *h* is chosen by concept of pythagoras triplets making ***h ≈ 0.75w,*** so that value of *r* remains uniform for all values of *h* and *w*.

6.1 V_{th} Variation with Normal Dopant Distribution:

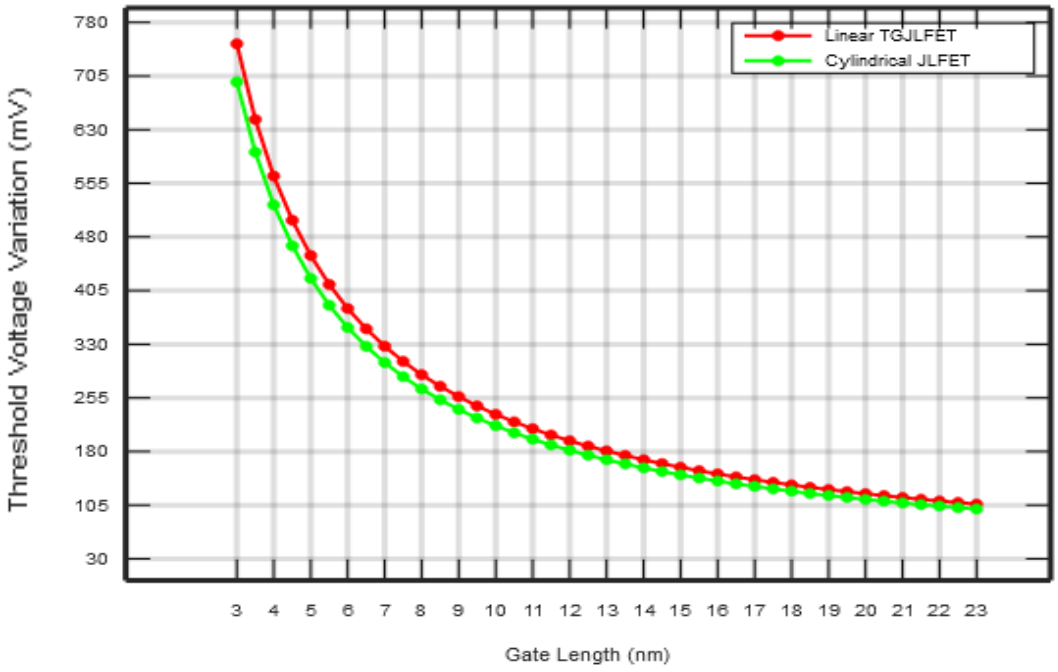


Figure 6.1 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with gate length for *normal dopant distribution*.

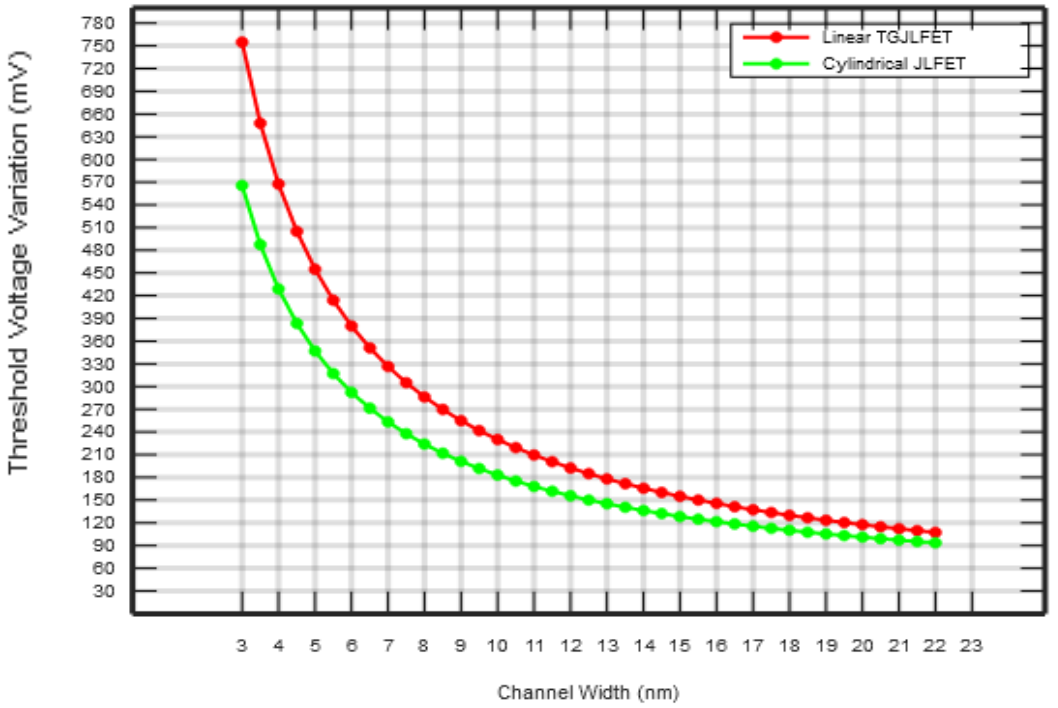


Figure 6.2 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel width for *normal dopant distribution*.

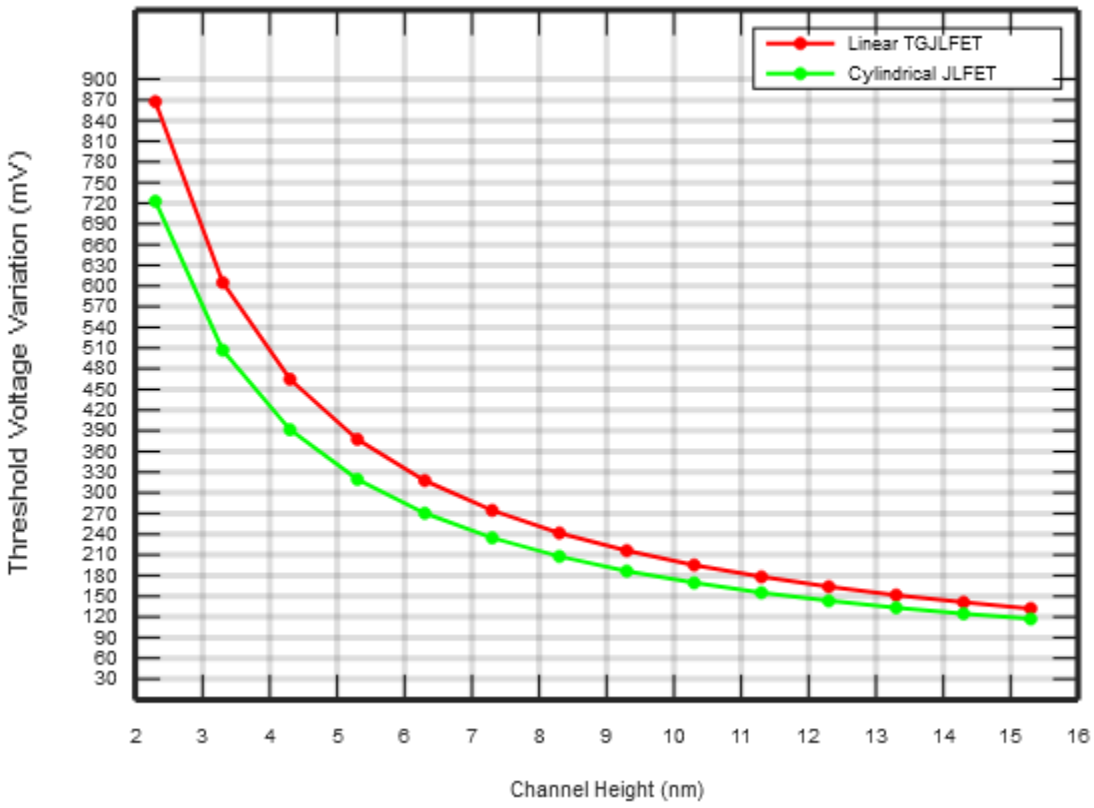


Figure 6.3 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel height for *normal dopant distribution*.

Fig. 6.1 presents the comaparison of variation of V_{th} with gate length($\boldsymbol{L_g}$) in TG JLFET and cylindrical JLFET. The range of L_g is considered to be from *3nm to 22nm*. It is evident from the graph that the variation of V_{th} with $\boldsymbol{L_g}$ is larger in case of TG JLFET. It is because of the structural improvement in cylindrical JLFET over a TG JLFET, since the latter has its gate wrapped fraom three sides of the channel, whereas in the former a single gate wraps the channel all around, thus providing better electrostatic control and reduced V_{th} variation. Such difference in V_{th} variation becomes more and more prominent with shrinkage of device dimension, showing roughly *6%* less variation of V_{th} in cylindrical JLFET at the smallest gate length of *3nm*. In this case we have

considered *w, h* and *r* of both JLFETS to be constants, and value of *w = 20nm, h = 16nm and r = 25nm*.

The comaparison for variation of V_{th} with channel width (***w***) and channel height(***h***) between a TG JLFET and cylindrical JLFET with normal dopant distribution is illustrated in ***fig. 6.2*** and ***fig. 6.3***. It is evident from the graph that when the dopant concentration N_d varies along the ***w*** and ***h*** of the JLFETs following the normal distribution, then the rate of variation of V_{th} is much lower in a cylindrical JLFET when compared to a TG JLFET.

For ***fig. 6.2***, we have considered L_g and h of both JLFETS to be constants. Here value of *Lg = 22nm, h = 16nm.* Here value of *r* for a cylindrical JLFET will not be a constant as it depends on *w* which is a variable. In case of shrinking channel width, there is roughly *24%* less variation of V_{th} in cylindrical JLFET at the smallest channel length of *3nm*.

For ***fig. 6.3***, we have considered L_g and *w* of both JLFETS to be constants. Here value of *Lg = 22nm, w = 20nm.* Similarly, value of *r* for a cylindrical JLFET will not be a constant as it depends on *h* in this case which is a variable. The V_{th} variation becomes nearly *17%* less in cylindrical JLFET when compared to a TG JLFET at the smallest value of the channel height at *h = 2.3nm*.

6.2 V_{th} Variation with Linear Dopant Distribution:

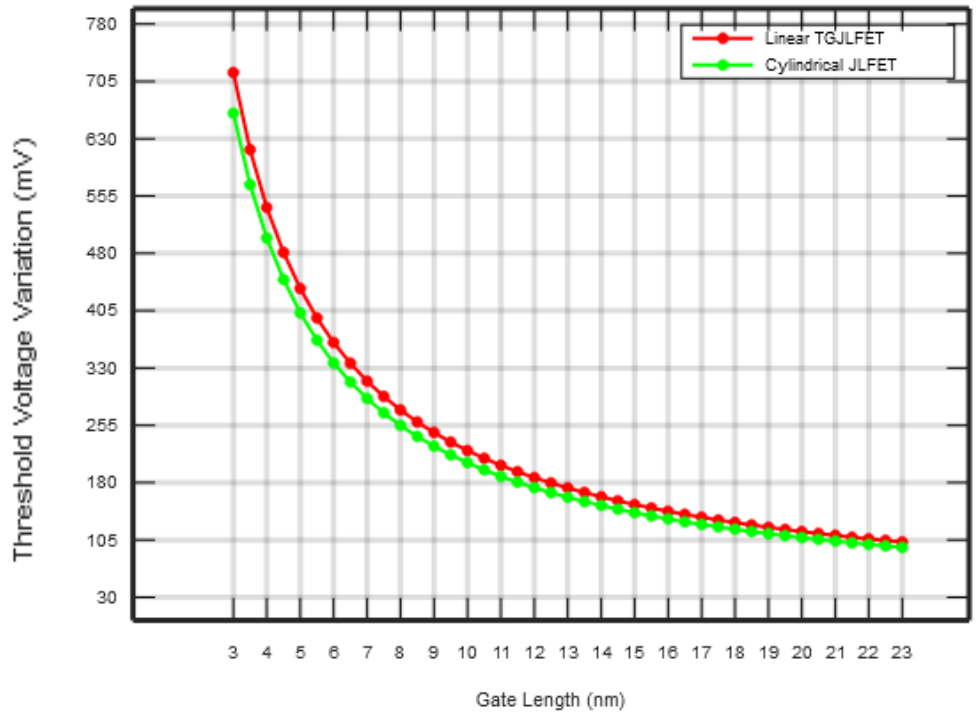


Figure 6.4 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with gate length for *linear dopant distribution*.

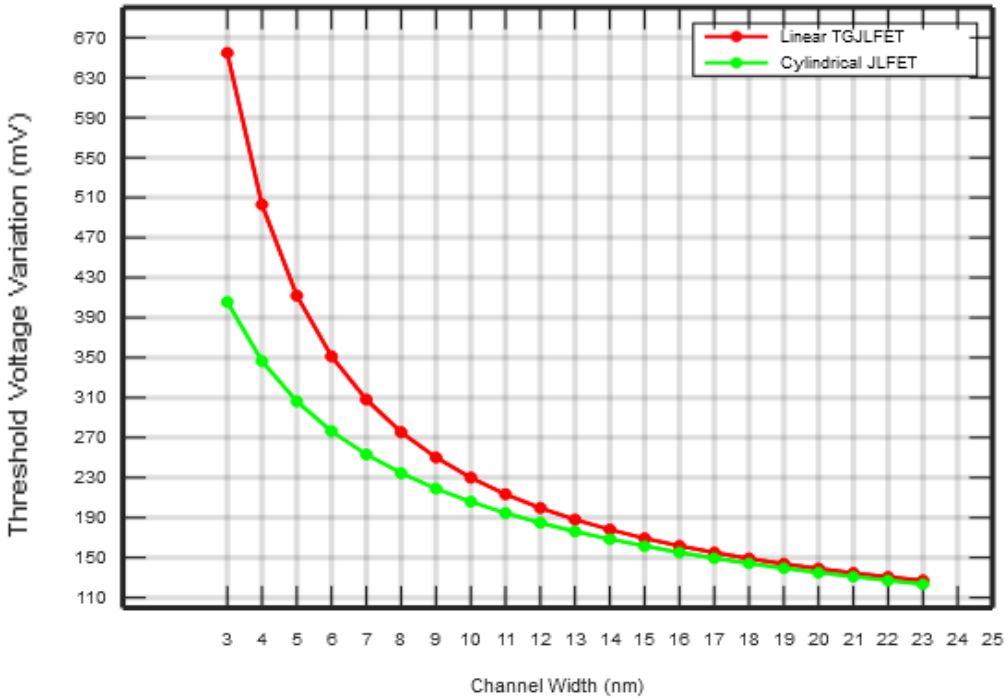


Figure 6.5 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel width for *linear dopant distribution*.

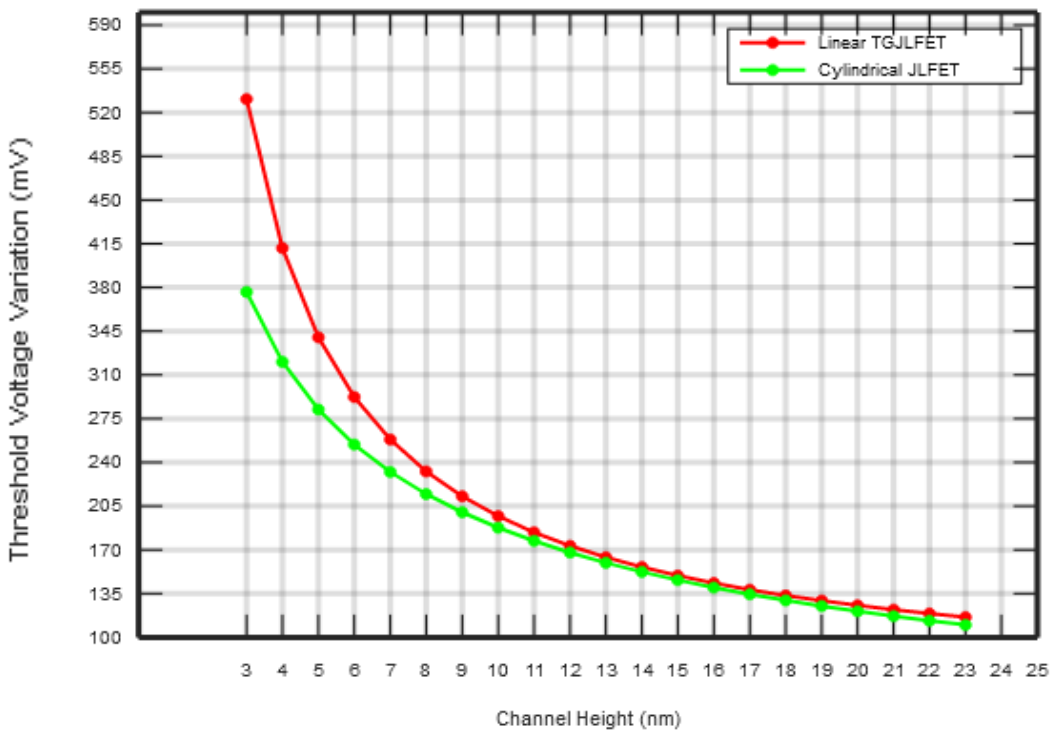


Figure 6.6 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel height for *linear dopant distribution*.

Fig. 6.4, fig. 6.5, and ***fig 6.6*** illustrates the plots of comaparison of variation of V_{th} with L_g, ***w*** and ***h*** by changing the dopant distribution to vary linearly. Here the figures shows that the overall magnitude of variation of V_{th} for both the JLFETs is lower compared to normal dopant distribution because in linear dopant distribution the rate of fluctuation of dopant atoms are comparitively slower than normal dopant distribution. So, the effect of RDF in linear dopant distribution is small compared to normal dopant distribution.

From the above figures, it is evident that that the TG JLFET provides an extra variation of *5.56%, 37.88%* and *28.3%* respectively at smallest value of L_g, *w* and *h* with linear dopant distribution.

6.3 V_{th} Variation with Normal Dopant Distribution & Quantum Confinement :

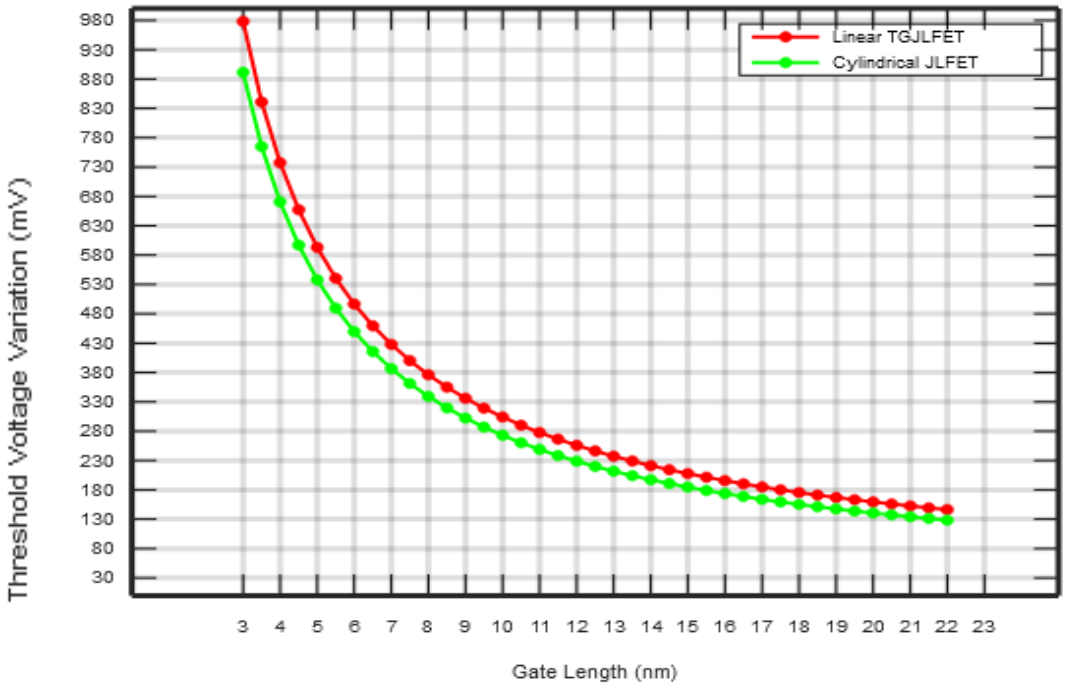


Figure 6.7 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with gate length for *normal dopant distribution* and *quantum confinement*.

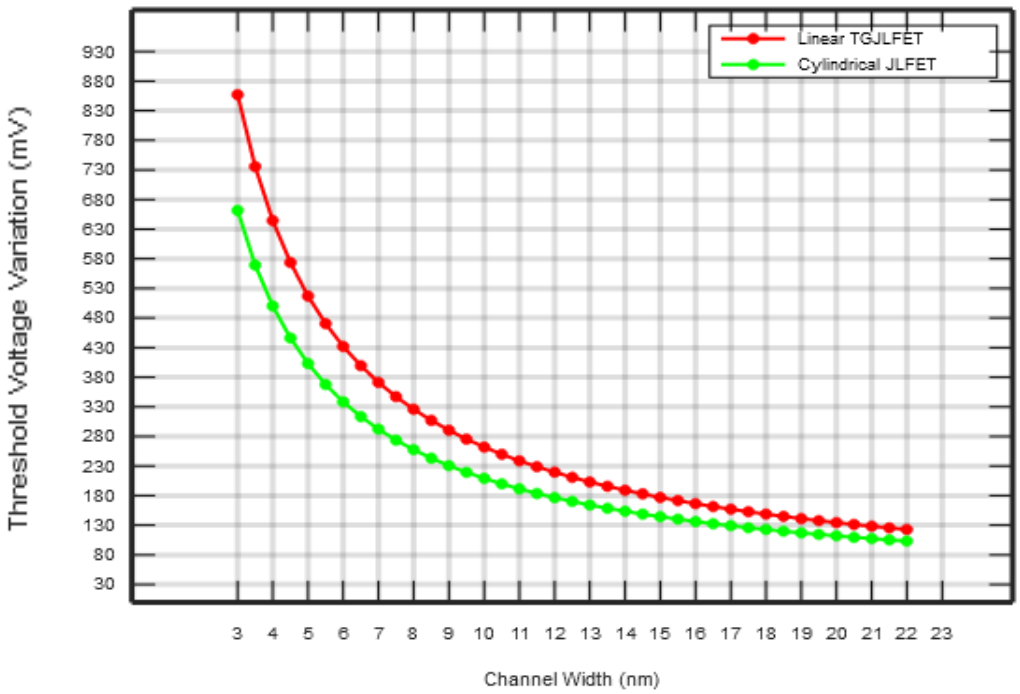


Figure 6.8 . Comparing V_{th} variation in linear TG JLFET and cylindrical JLFET with channel width for *normal dopant distribution* and *quantum confinement*.

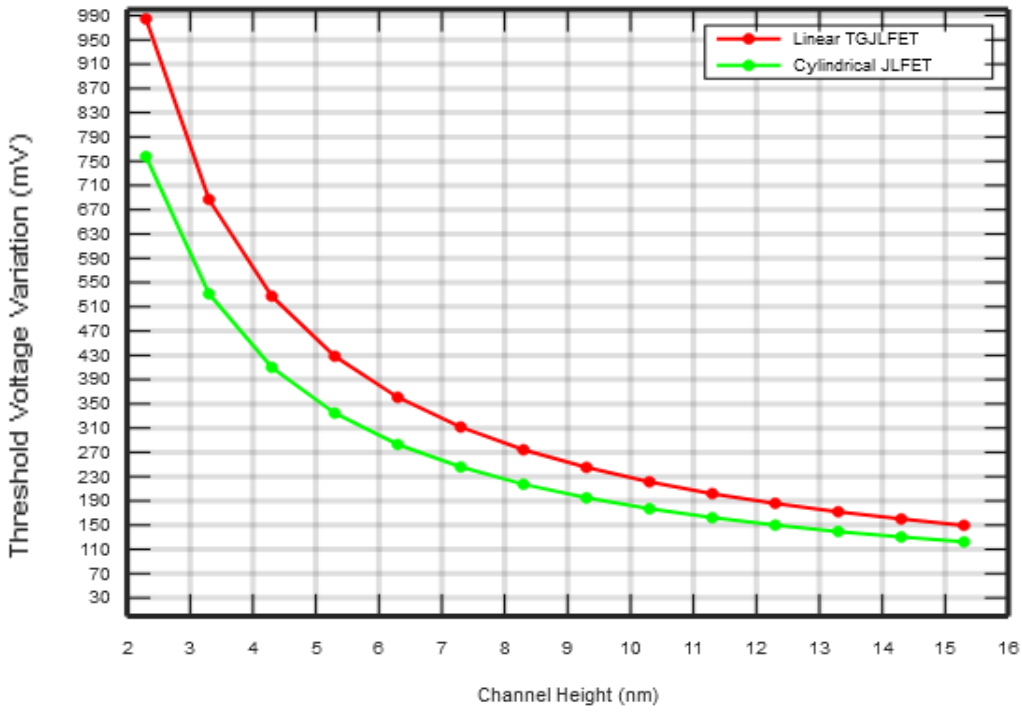


Figure 6.9 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel height for *normal dopant distribution* and *quantum confinement*.

Fig. 6.7, fig. 6.8, and ***fig 6.9*** shows the plot of comaparison of variation of V_{th} with with L_g, ***w*** and ***h*** in presence of both RDF and quantum confinement. The quantum confinement is an additional effect which is arising due to the quantum sizing of the transistors which further increses the V_{th} variation. As described in the earlier chapters, unlike RDF this effect is only dependent on the dimensions and doesnot depends on the type of dopant distributionso, it can be inferred that for a particular device the V_{th} variation due to QSE will remain same even though same device have different dopant distributions. As a result the additional variation of V_{th}, due to this effect is superimposed on the magnitude of V_{th} of ***fig. 6.1, fig. 6.2,*** and ***fig 6.3*** without any change in shape.

6.4 V_{th} Variation with Linear Dopant Distribution & Quantum Confinement:

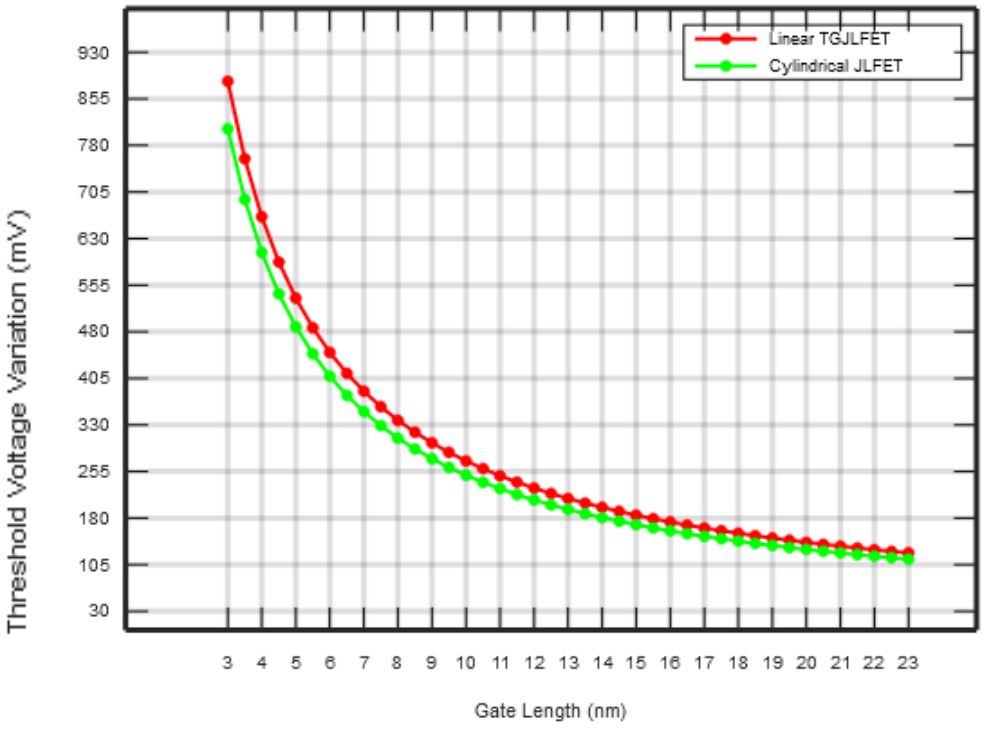


Figure 6.10 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with gate length for *linear dopant distribution* and *quantum confinement*.

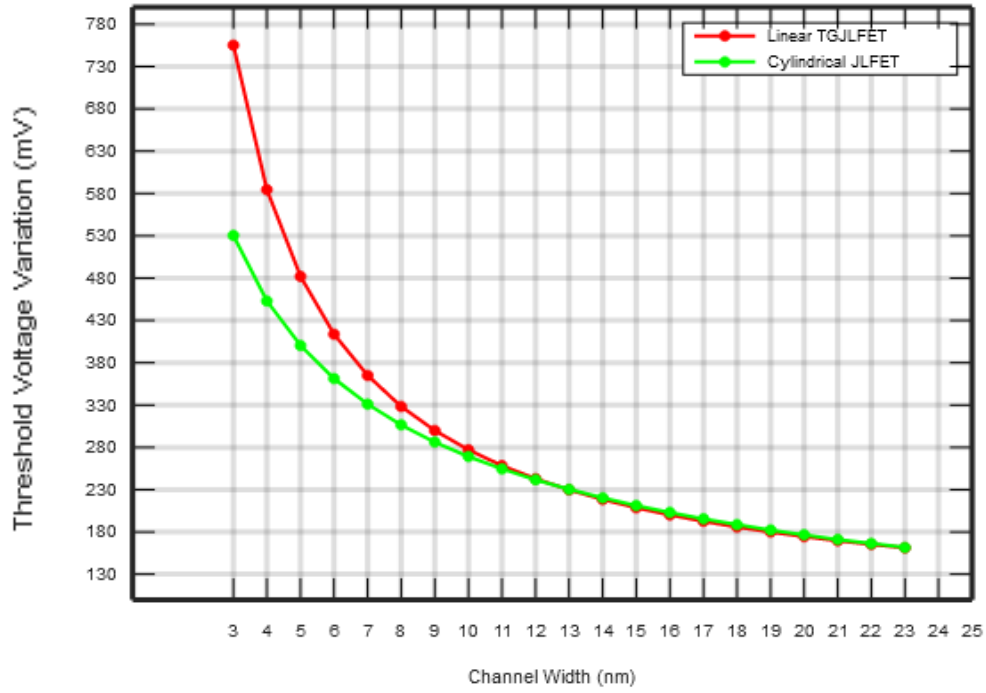


Figure 6.11 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel width for *linear dopant distribution* and *quantum confinement*.

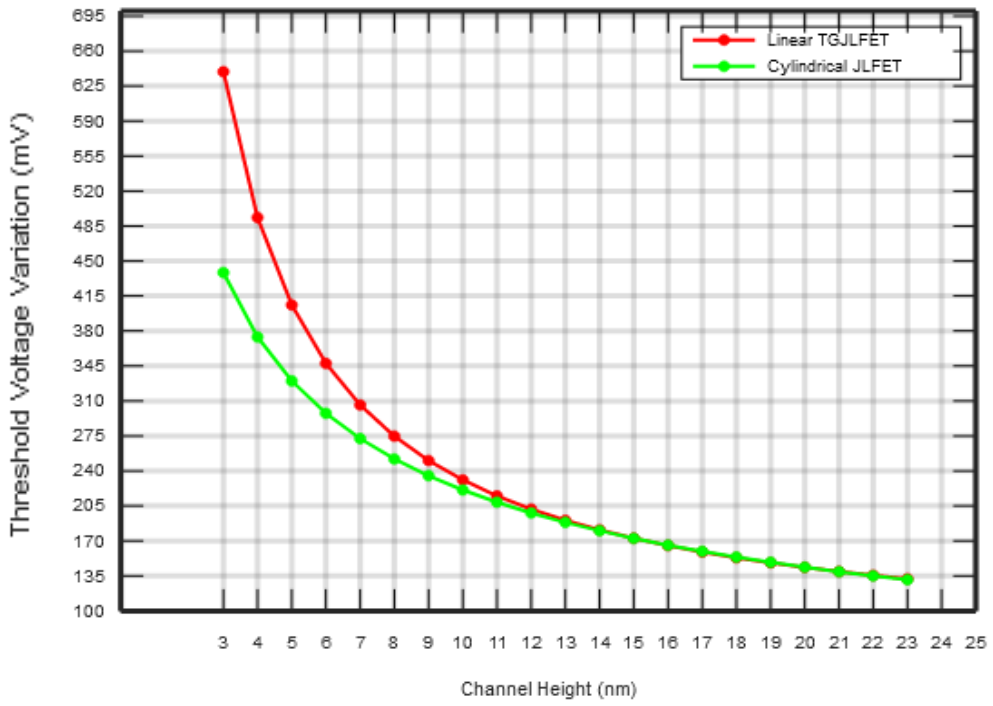


Figure 6.12 . Comparing V_{th} variation in TG JLFET and cylindrical JLFET with channel height for *linear dopant distribution* and *quantum confinement*.

Fig. 6.7, fig. 6.8, and ***fig 6.9*** shows the plot of comaparison of variation of V_{th} with with L_g, ***w*** and ***h*** in presence of both RDF and quantum confinement with linear dopant distribution. The explanation for these plots matches with the same for normal dopant distribution which has been clearly described in previous sections.

6.5 Comparison of V_{th} variation by varying two dimensions of JLFET simultaneously :

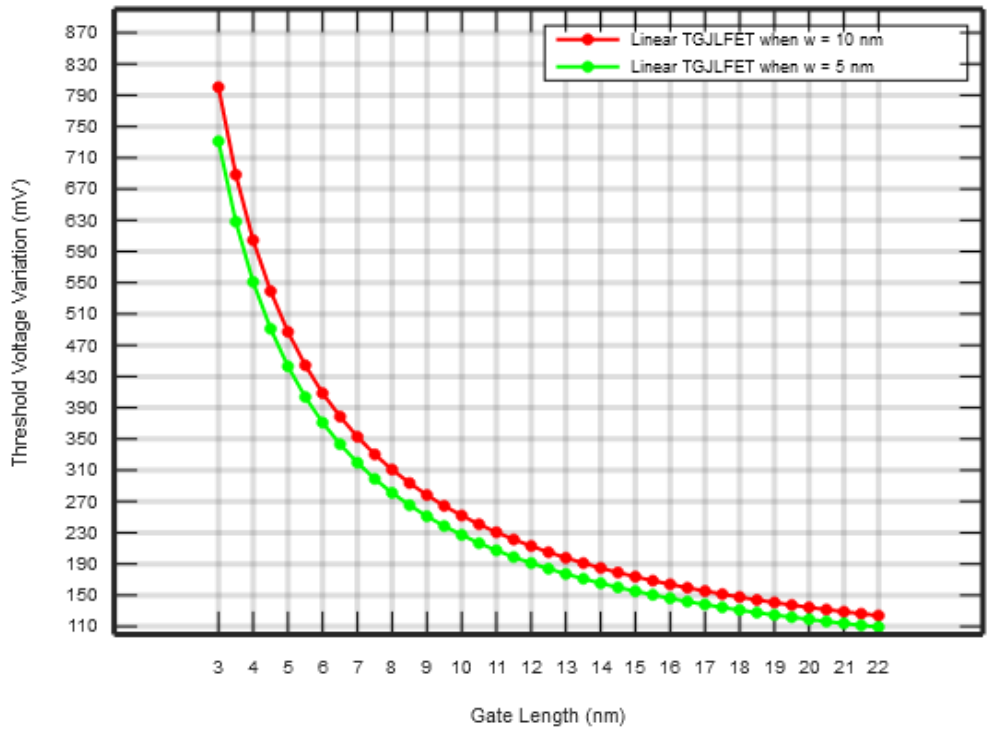


Figure 6.13 . Comparing V_{th} variation in two TG JLFETs with gate length for *two different channel widths*.

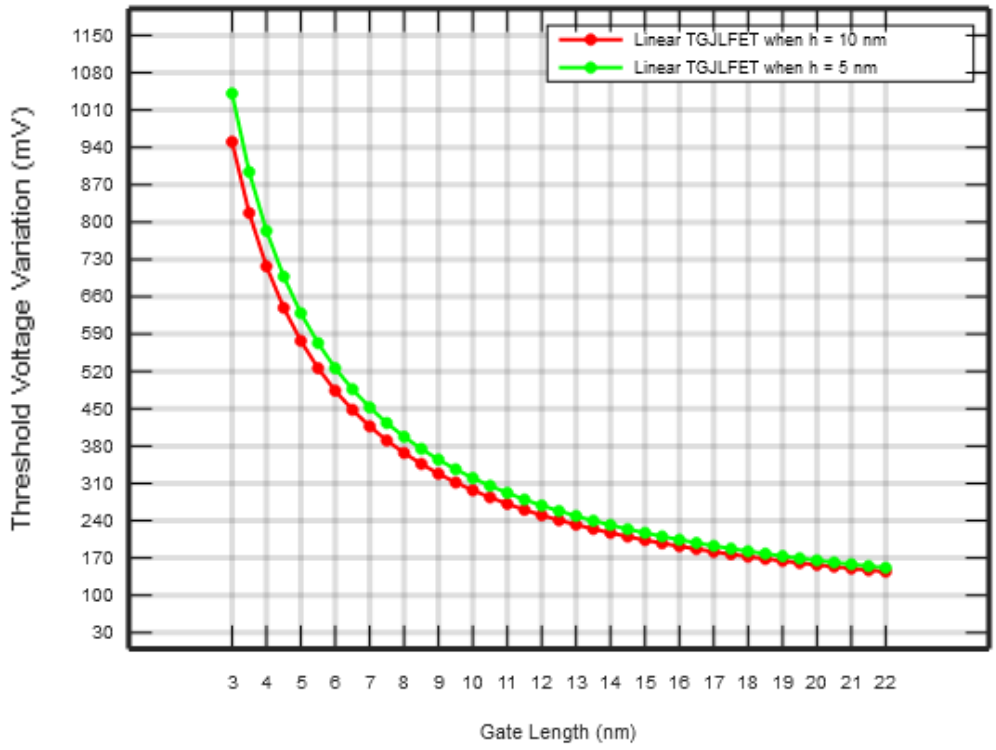


Figure 6.14 . Comparing V_{th} variation in two TG JLFETs with gate length for *two different channel heights.*

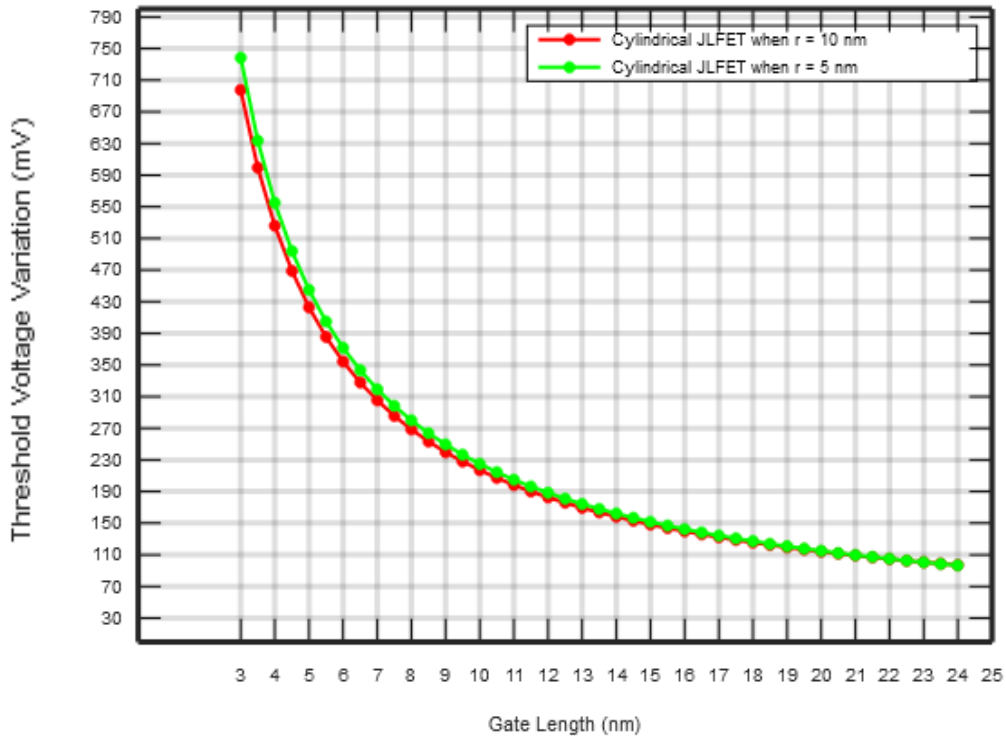


Figure 6.15 . Comparing V_{th} variation in two cylindrical JLFETs with gate length for *two different channel radius.*

Fig. 6.13 and ***fig. 6.14*** shows the plots of variation of threshold voltage with gate length L_g for two linear TG JLFETs with different channel widths and channel heights respectively. In this analysis, the effect of quantum confinement of carriers is ignored because our main analysis is to study effect of RDF only and quantaum confinment effect has no impact on RDF.

In ***fig. 6.13***, the variation of V_{th} is slightly more in TG JLFET with width(w) = *5nm* compared to a TG JLFET with *w=10nm*. The variation of V_{th} is nearly *8.64%* more in the device with smaller width since, as we are reducing ***w*** RDF will increase as we know that it is difficuilt to properly dope a device with smaller dimensions and effect of RDF is more dominant in that case.

In ***fig. 6.14***, the variation of V_{th} is around *9.52%* more in TG JLFET with height(*h*) = *5nm* compared to a TG JLFET with *h=10nm*. The reason for this is same as explained in case of ***fig 6.13***.

Fig. 6.15 illustrates the plot of variation of threshold voltage with gate length $\boldsymbol{L_g}$ for two cylindrical JLFETs with different radius. In this analysis, the effect of quantum confinement of carriers is ignored. The variation of V_{th} is *6.71%* more in cylindrical JLFET with radius(*r*) = *5nm* compared to a cylindical JLFET with *r =10nm*. The variation of V_{th} is more in the device with smaller radius since, we know that, $\boldsymbol{r = \sqrt{w^2 + h^2}}$ so as we are reducing *r*, the *w* and *h* component inside *r* will also reduce and, because of that RDF will increase as we know that it is difficuilt to properly dope a device with smaller dimensions.

6.6 Conclusion:

This chapter describes the results of performance comparison for a linear TG JLFET and a cylindrical JLFET. It is clearly evident from the results presented in this chapter that a cylindrical JLFET provides a better control over threshold voltage than a TG JLFET for a channel with smaller dimensions because of its structural advantage.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION:

The study in this thesis deals with analyzing the performance of different JLFET structures under RDF for smaller channel dimensions. The JLFETs have been evolved to combat the SCEs arising in MOSFETs because of aggresive scaling primarily to serve the increasing demand of modern day complex VLSI chips. Thus in the present study, JLFETs with smaller channel dimensions, are mainly focussed.

The two devices that are proposed and analyzed in our work are TG JLFET and cylindrical JLFET. The device performance has been investigated by varying the channel dimensions, viz. length, width and height, and studying the variation of V_{th} with them. The close agreement between the results obtained from the analytical model and the results present in our reference paper validates our proposed model. It was quite evident from our results that cylindrical JLFET provides less V_{th} variation compared to a TG JLFET, and thus acheiving better performance. The reason behind better performance in cylindrical JLFET is its greater elctrostatic control over the channel because of its structural modification, thereby minimizing the effect of RDF.

The effect of quantum confinement of carriers is also considered in this study. The V_{th} variation becomes more and more significant with the reduction in the channel dimensions, and thus degrades the performance of our proposed models.

The detailed investigations presented in the thesis reveal that the appropriate optimization of the proposed architecture may yield high performance device which minimizes the effect of RDF for short channel devices.

TABLE SHOWING V_{TH} VARIATION DUE TO EFFECT OF RDF WITHOUT QUANTUM CONFINEMENT:

		TG-JLFET			CYLINDRICAL JLFET		
		GATE LENGTH (L_g)	CHANNEL WIDTH (w)	CHANNEL HEIGHT (h)	GATE LENGTH (L_g)	CHANNEL WIDTH (w)	CHANNEL HEIGHT (h)
SMALLEST VALUE OF PARAMETER CONSIDERED IN THE STUDY (nm)		3	3	2.3	3	3	2.3
ΔV_{TH} AT SMALLEST VALUE OF PARAMETER	WITH NORMAL DOPING PROFILE (mV)	770	755	870	705	570	725
	WITH LINEAR DOPING PROFILE (mV)	710	660	535	650	415	380

The V_{TH} variation at the smallest value of L_g, w and h is shown in ***Table 7.1. Table 7.2*** ilustrates the data obtained from the results implying how much performance is improved using a cylindrical JLFET compared to a TG JLFET under the effect of RDF only, when the device has a very small channel dimensions.

TABLE FOR SHOWING BETTER PERFORMANCE IN CYLINDRICAL JLFET COMPARED TO TG-JLFET:

	WITH GATE LENGTH (L_g)	WITH CHANNEL WIDTH (w)	WITH CHANNEL HEIGHT (h)
% OF ADDITIONAL VARIATION IN TG-JLFET COMPARED TO CYLINDRICAL JLFET WITH NORMAL DOPING PROFILE	6%	24%	17%
% OF ADDITIONAL VARIATION IN TG-JLFET COMPARED TO CYLINDRICAL JLFET WITH LINEAR DOPING PROFILE	5.56%	37.88%	28.3%

TABLE 7.2

7.2 SCOPE FOR FUTURE WORK:

The present thesis deals with the comparison of performance for modern short channel devices such as TG JLFET (FINFET) and cylindrical JLFET (GAAFET) under the effect of RDF. However, here the parameter considered for analyzing the performance of the above devices is only by the variation in threshold voltage(V_{th}). The future studies could thus be extended to find the variation of I_{ON}/I_{OFF} ratio with the device dimensions for the above devices.

The GAAFET is structured in such a way so that it can provide better performance than a FINFET when the device channel dimension is extremely small. The future study can thus be extended where other short channel effects

like DIBL, velocity saturation, hot carrier effect, mobility degradation can be considered and study whether GAAFET is providing better results over FINFET or not.

The present thesis considers the GAAFET with of single material single gate only. The study can be generalised for multiple material multi gate GAAFET. If the material across the two gates of GAAFET are interchanged , the performance of the device can further be investigated.

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