Junctionless Field Effect Transistor (JLFET):

Performance Evaluation and Applications

Thesis submitted for partially fulfilling the requirements of the Master degree of Electronics and Telecommunication Engineering

Submitted by

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CERTIFICATE

This is to certify that the thesis entitled, "**Junctionless Field Effect Transistor(JLFET): Performance Evaluation and Applications**" submitted by Chayan Dutta (Roll No.: 002010702005) of Jadavpur University, Kolkata is a record of bonafide thesis work under my guidance and can be accepted for partially fulfilling the requirement of the degree of Master of Engineering in Electronics and Tele-communication Engineering. The results shown in this thesis are not included in any other paper submitted for the degree to any other University or Institute.

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DECLARATION OF ORIGINALITY AND COMPLIANCE OF AN ACADEMIC THESIS

I hereby certify that this thesis entitled, **"Junctionless Field Effect Transistor (JLFET): Performance Evaluation and Applications"**

-None has submitted this work to any other institute for achieving any degree

-All the results have been obtained and represented according to academic rules and regulations and the ethical Code of Conduct of the institute

I also undertake that, as specified by the code of conduct, wherever I have used materials which are not original to this work, I have given proper credit by citing them in the references of the thesis.

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Contents

Chapter 1
Introduction

1.1 Introduction

In Field Effect Transistor or simply FET, voltage is applied to the Gate input to control the channel conductivity and thereby, the output current. As its operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, it is called a voltage controlled device. The Field Effect Transistor is a three terminal semiconductor device that has very similar characteristics to those of Bipolar Transistor. FET is more useful in most electronic circuit applications than Bipolar Junction Transistors (BJT) for the benefits as follows-

- Input – output isolation
- Planar structure resulting in high integrability
- Low noise as majority carrier device
- High efficiency
- Faster operation
- Robustness
- High thermal stability

FETs can be made much smaller in size than an equivalent BJT. In addition to that, low power consumption of FET makes it ideal for use in integrated circuits. Passive components i.e. resistor & capacitor and active source i.e voltage controlled current source can be realized using

MOSFET. The I-V relation of MOSFET involves *W/L* ratio. If channel width and length are reduced by same factor, its performance would remain unaltered. This introduces concept of MOS scaling and makes large no of MOSFETs feasible in single chip. The integration limit is provided by Sir Gordon Moore. As of now on an average, each IC consists of 2 trillion MOSFETs.

Moore's First law:

Following the downscaling in size of MOS as proposed by Gordon Moore and demand in the count of devices accommodated in integrated circuit(IC) was increasing continuously. Moore observed that the size of transistors was reducing continiously for the continuous innovation. In 1965 Moore predicted that the count of devices in a chip would be doubled each year for the upcoming decade. Gordon Moore's prediction held true for 10 years. He then revised his prediction and stated that the number of transistors would double every two years from that time onwards. This is Moore's First law, which became the main industry driver. Over the last few years, the growth of the number of transistors on each IC is declining due to saturation reached by practical limitations of manufacturing processes.

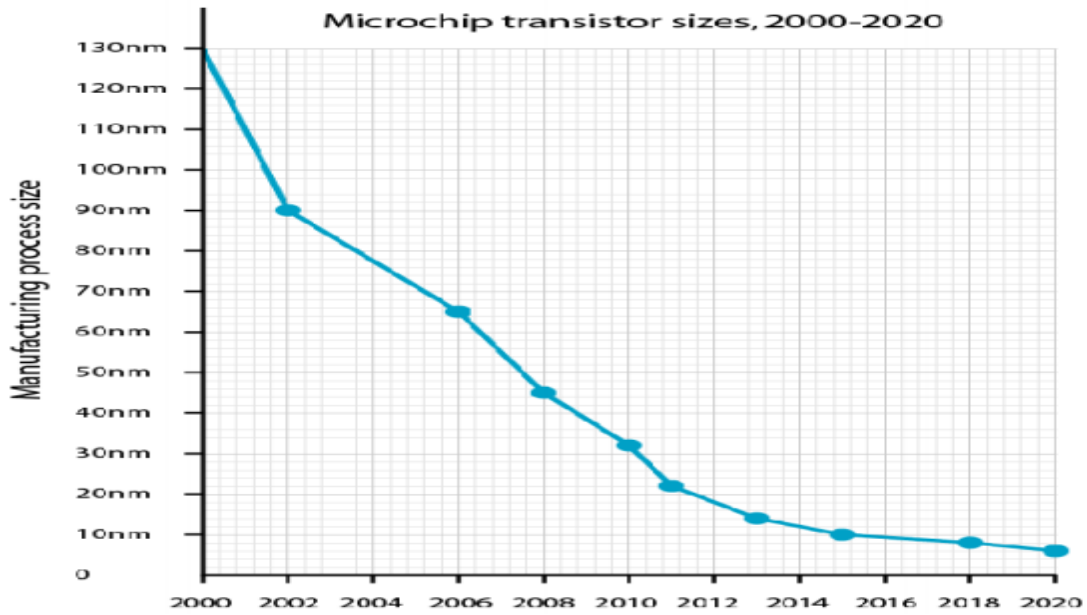

Fig 1.1 Feature Size Reduction with Time [17]

Moore's Second Law:

Moore also stated that the capital cost of manufacturing ICs would increase exponentially over time. In other words, the cost of R&D, manufacturing, and testing are rising exponentially with each new generation of chips. An important role is played by Moore's Second Law for the sustainability of Moore's First Law. As the cost of innovation and manufacturing are increasing, companies are likely to reduce the rate at which they advance technologically, and the number of transistors is likely to be lower than what was predicted by Moore's First Law.

To meet goals as stated by Moore, device level as well as circuit level modifications are made. Thus, Double Gate MOSFET, Triple Gate MOSFET, Gate-All-Around FET and FinFET have evolved to provide better gate control and suppress various short channel effects.

The drain and source in devices with junctions are formed to affect the device as well as circuit performance. Also scaling of MOSFET without performance degradation requires costly and

complex fabrications. Hence concept of no junction i.e. JLFET evolves. No metallurgical junction is present in JLFET. So these are simpler and less expensive to manufacture. JLFET utilizes a gated semiconductor film to control its resistance and the current flowing through it. These added benefits influence me to conduct research on performance and various applications of JLFET.

1.2 Organisation of the Thesis:

The work presented in the thesis is organized as below:

Chapter 1 gives brief introduction of JLFET and its advantages over other structures.

Chapter 2 throws some light on JLFET fundamentals and related works done so far.

Chapter 3 describes quantum effect in JLFET.

Chapter 4 tells about power consumption and propagation delay of various applications of JLFET.

Chapter 5 gives the conclusion of the same.

Chapter 2

Review of JLFET: Fundamentals and Related Works

In this chapter, some fundamental aspects of JLFETs will be described.

2.1 JLFET Fundamentals

2.1.1 Structure of Junctionless FET:

Julius Lilienfeld discovered FET devices similar to MOS devices. It is made of a thin film of semiconductor material deposited on insulator, which is deposited on an electrode formed using metal [20-23]. The electrode works as the gate. In practical, the current flows through the resistance between two contact electrodes as the current through drain flows in between the drain and source in a conventional MOSFET[24-30]. The device invented by Lilienfield is a voltage controlled resistor. The application of voltage at the gate forces the semiconductor film to be depleted of charge carriers, thereby modifying its conductivity. Theoretically, it must be possible to entirely deplete the film of carrier when the resistance of the device turns to be quasi-infinite [35-41]. A transistor is an active device that checks flow of current dynamically, and the word 'transistor' is a combination of 'trans' and 'resistor'. FET is a resistor in which a gate controls the carrier density and therefore, the current flow. Lilienfield's transistor was never able to yield a good working device.

The Lilienfield transistor, unlike all other types of transistors, does not contain any junction. In recent days devices are of such small dimensions that very sharp gradients of dopant concentration are needed: typically the dopant must change from donor concentration as 2×10^{19} cm^{-3} to acceptor concentration as 2×10^{18} cm^{-3} within a few nanometers[45-52]. These impose restrictions on the thermal budget and need the deployment of expensive fast annealing. Having no junction presents a great advantage. In a junctionless FET the channel dopant concentration is same as the source and drain dopant concentration. As the dopant concentration gradient in source-channel and drain-channel is zero, diffusion cannot occur. It removes the need for expensive superfast annealing setup and enables one to make shorter channel devices.

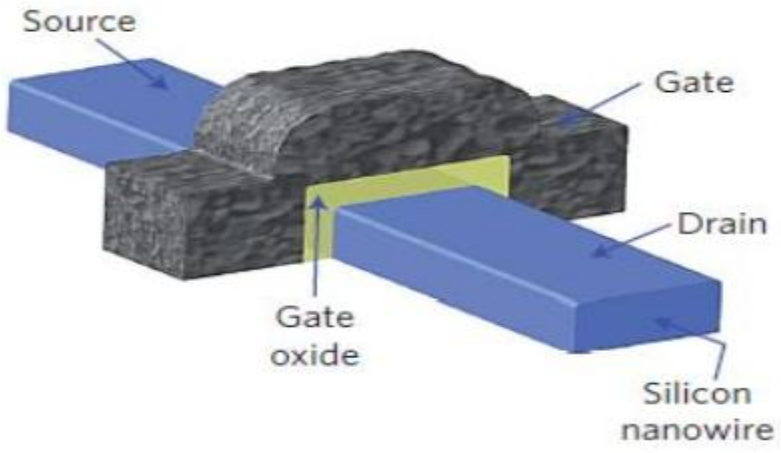

Fig 2.1 Structure of JLFET [16]

2.1.2 Fabrication of Junctionless FET:

The key step to fabricate a junctionless transistor is forming a layer of semiconductor material. It must be very thin and narrow so that charge carriers can be fully depleted during the OFF state of the device [58-66]. The semiconductor sample must be doped heavily so that a sufficient current

can flow during the ON state. These two conditions together necessitate the requirement of nano-scale dimensions and very high dopant concentrations.

We fabricate the devices on standard Silicon-On-Insulator (SOI). We thin down SOI layer to 10 *nm* and pattern into nano-ribbons by electron beam lithography [71-78]. Gate oxidation is performed and after that ion implantation is used so that devices are doped uniformly to make N^+ or P^+ having a dopant density as $(3\text{-}4)\times10^{19}\ cm^{-3}$, which is Lightly Doped Drain(LDD) for N and P channel devices. Gate is made using comparatively thick layer (50 *nm*) of amorphous Si at a temperature about 560 ^oC in a ultra-low pressure chemical vapor deposition (LPCVD) chamber [81-87]. The N-channel and the P-channel devices have a P^+ and N^+ polysilicon gate respectively which eliminate poly depletion effects and yield required threshold voltage. No other source and drain implant is used. Oxide deposition is done and later it is etched to produce contact holes and TiW + Al metallization complete the process [92-98]. Nano-ribbons are formed with thickness in the range of 6 to 9 *nm* and width in the range from 25 to 35 *nm*. The thickness of oxide is about 9 *nm*.

The Junctionless gated silicon nano-wire transistor is made by Atomic Force Microscopy (AFM) and wet etching process applied to SOI wafer of p-type. The electronic design of nanometer scale is formed on <100> SOI wafer by the usage of Scanning Probe Microscopy (SPM) through Atomic Force Microscope (AFM) nanolithography [102-108]. Let us take the example fabrication process of nano-electric device based on potassium hydroxide etch applied to materials made by AFM nanolithography. The samples having a surface area (1.1-1.6) cm^2 are cut to from p-type SOI <111> wafers which are doped with phosphorous having resistivity about 5-10 Ω-*m*, diameter (90±0.25) *mm*, thickness (500 ± 20) μm. The samples are cleaned by using ammonium hydroxide and hydrogen peroxide heated at 80^oC for 15 minutes followed by rinsing

with De Ionized Water (DIW) to remove the organic components [31-34]. Solution of hydrochloric acid and hydrogen peroxide were used to clean the ion metal on surface. Diluted hydrofluoric acid (1:20) was used to eliminate the stray oxide layer. All samples are rinsed with hydrofluoric acid to give them same initial conditions [42-44]. After the operation, the samples are placed in the container, containing the aqueous potassium hydroxide varying in concentrations from 10 percent wt. to 40 percent wt. We etch the samples in the solution for 10 *sec* in 50°*C* with an accuracy of ±0.5°*C*. The nano electronic form of the transistor is made by using the nanolithography. The pattern is created on SOI <100>. Before growing oxide as a mask, the SOI is undergone through cleaning method as mentioned earlier.

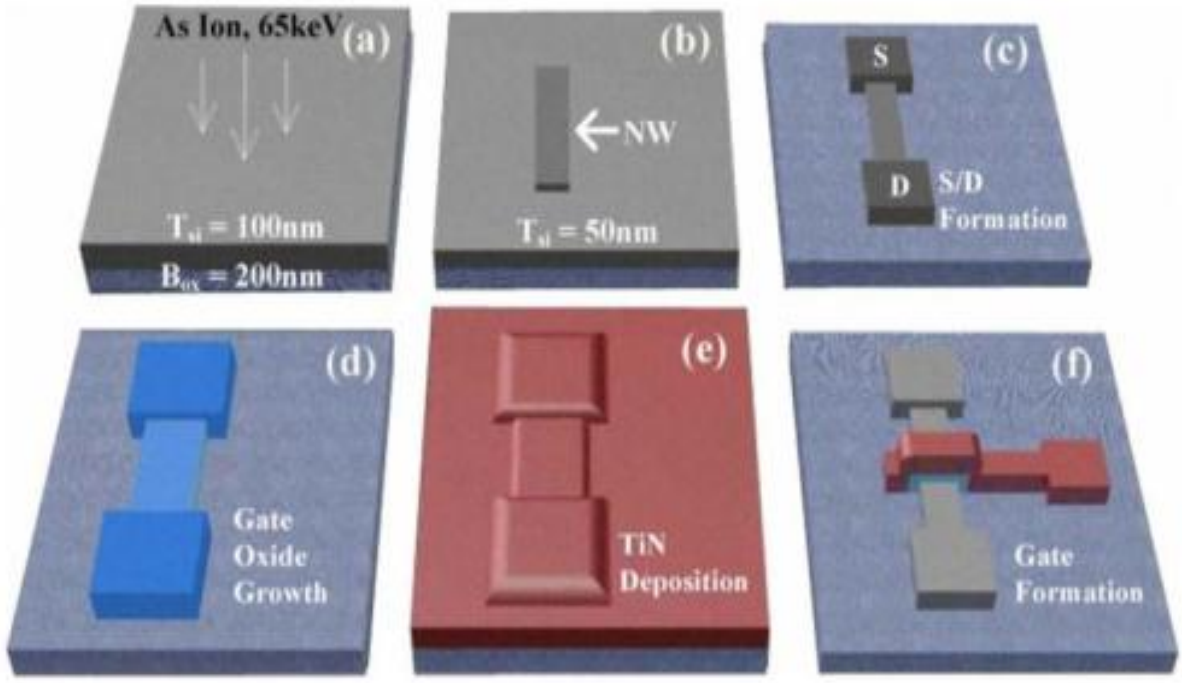

Fig 2.2 Fabrication by E-Beam Lithography[16]

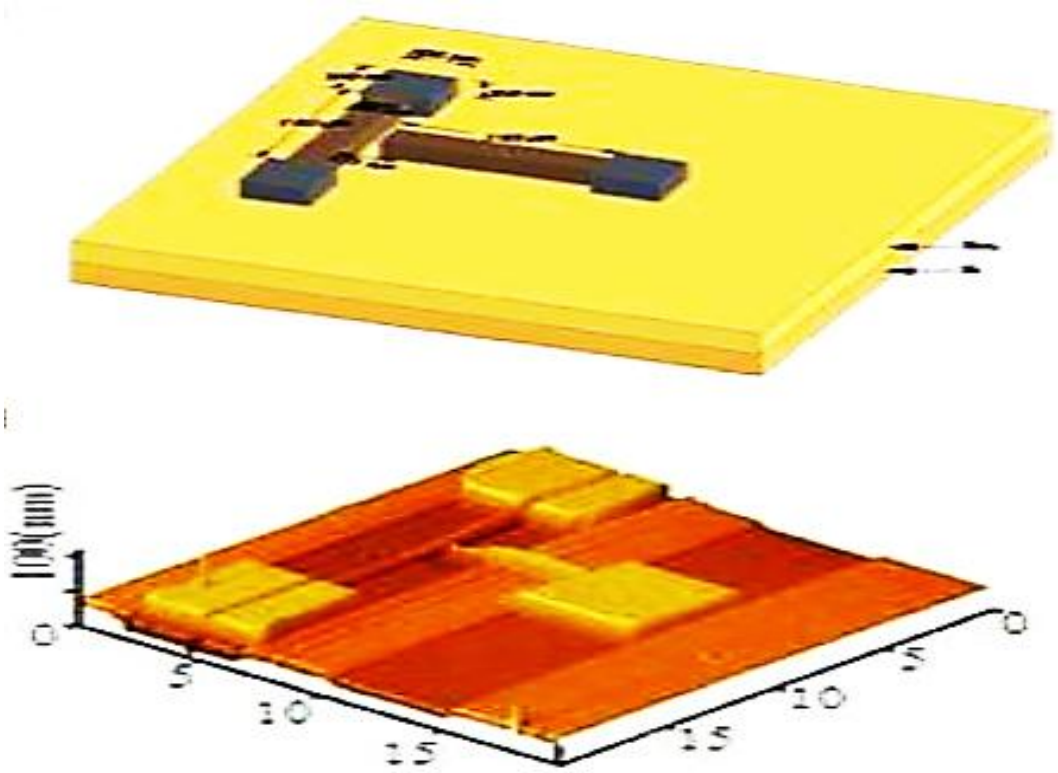

Fig 2.3 Fabrication by Atomic Force Microscopy[16]

2.1.3 Various Modes of Operation:

In nanowire centre channel region of gated resistor is neutral. Since the charge carriers are gathered in neutral Si, a null electric field is observed in the perpendicular direction to the flow of current [53-57]. During the ON state, considering a very low voltage at drain, the entire channel is uncharged and in flatband state. The channel thus behaves as a resistor having conductivity $\sigma = q\mu N_D$. Here q, μ and N_D are electronic charge, mobility and donor concentration respectively. The electron mobility in highly doped n-type silicon is nearly 100 $cm^2\ V^{-1}s^{-1}$[67-70]; it changes very little for donor concentration in the range of $1x10^{19}$ to $1x10^{20}\ cm^{-3}$ [79-80]. Hole mobility roams around 40 $cm^2\ V^{-1}s^{-1}$ in p-type sample with the same acceptor

concentration. In case of unstrained Si, the mobility of bulk MOSFETs drop from 390 $cm^2 V^{-1} s^{-1}$ for the 0.78 μm node to 90 $cm^2 V^{-1} s^{-1}$ for the 0.15 μm node [88-91].

A fall of the highest mobility from 295 to 135 $cm^2 V^{-1} s^{-1}$ is observed in FinFETs when the length of the gate is lowered from 0.89 to 0.13 μm. If it is for unstraining techniques, the mobility of electron for the 42 *nm* node could be far below 90 $cm^2 V^{-1} s^{-1}$. We can use straining techniques to both gated resistors and inversion-mode transistors [99-101]. In case of a MOSFET, charge carriers are bounded in an inversion mode channel for which scattering highly increases in frequency with gate terminal voltage. So transconductance and current are reduced. In the highly doped FET, the current in drain flows through the whole nanoribbon, instead of being restricted in channel surface. Figure 2.4 presents the concentration of carrier in an n-type junctionless FET for various values of voltage at the gate in the range from device pinch-off to flatband condition. The conduction path is visibly located at the centre of the nanowire. Thus electrons move through the silicon with bulk mobility. It is also possible to make accumulation channels at surface by increasing the voltage of the gate beyond the flatband condition, if transconductance degrades more slowly when voltage at the gate is increased. As a result, current and speed performance of higher value can be achieved. The change of the threshold voltage of a gated resistor is approximately -1.5 mV^oC^{-1} [109-110]. The degradation of mobility with increase in temperature is lower for the gated resistors than in FETs with triple gate. In case of a FET with low dopant density, the mobility is affected by phonon scattering, so it presents strong dependence on temperature. But in the heavily doped gated resistor mobility is affected by ionized impurity scattering and its fluctuation with temperature is much smaller.

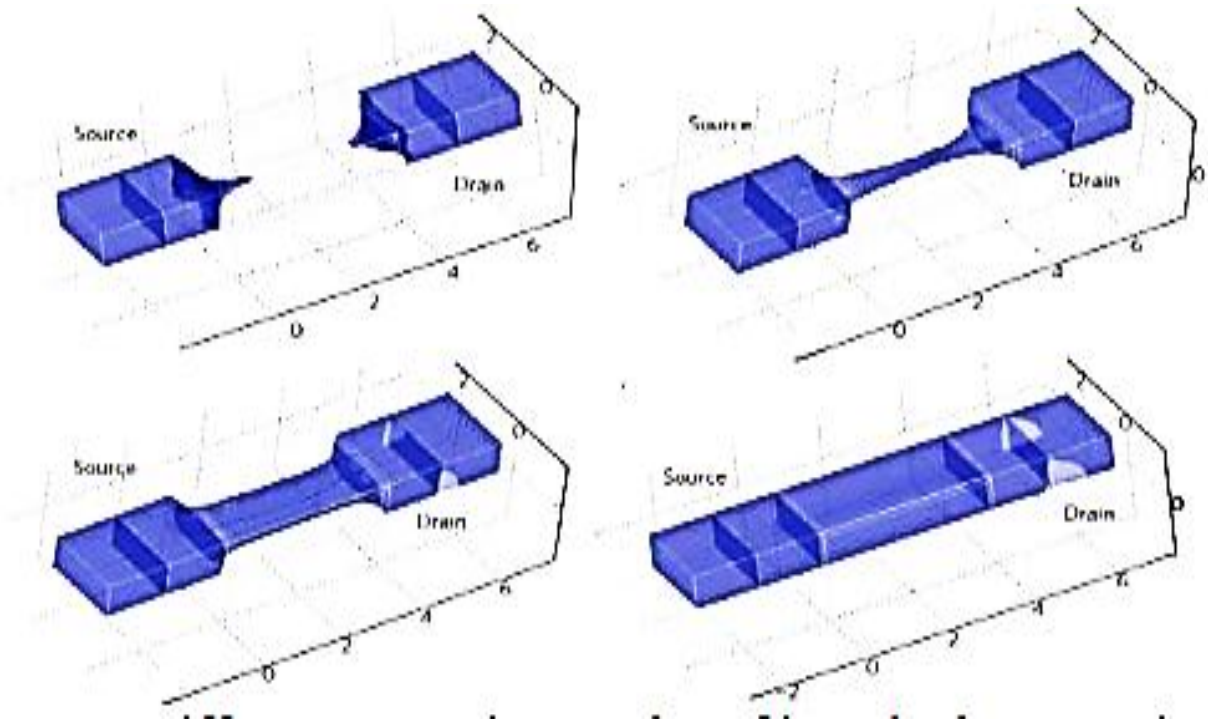

Fig 2.4 Different Operating Modes of Junctionless Transistor[16]

2.1.4 Types of Junctionless Transistor

1. Junctionless Multi-Gate FET (JLMuGFET):

This device does not have any junction. So a simpler process of fabrication is required [16]. Lesser variability and better electrical property can be achieved than in case of standard inversion mode.

2. Junctionless Transistor with Bulk Planar Structure:

The junctionless transistor (BPJLT) having planar structure is highly scalable field-effect transistor with no junction. So source, channel and drain are of same dopant density. But it still necessitates a junction vertically for purpose of isolation.

3. Junctionless MOSFET with Vertical Channel(JLVMOS):

The junctionless VMOS is made on bulk-silicon wafer. The channel in the vertical direction is obtained by the spacer along the gate, and thus the making cost can be made smaller. The dual-gate structure of a VMOS helps in increasing the controllability of the gate over the channel[18].

2.1.5 Comparison between Junction-based and Junctionless Transistor

MOSFET is normally in OFF state and does not allow any flow of current if there is no conductive path established between source-drain. For turning the device ON, the voltage of the gate is enhanced so that an inversion channel is formed. The current through drain in such a device is given by

$$I_D = \mu C_{ox}(W_{Si}/L)(V_{DD} - V_{TH})^2 \ldots\ldots\ldots(2.1)$$

where W_{Si} represents the device wideth, L represents the length of the gate, V_{DD} represents the supply voltage and C_{ox} represents the capacitance of the gate oxide.

On the other hand the gated resistor is normally in ON state. So the work function difference of the silicon nanowire and the gate changes the flatband and the threshold voltages to values greater than zero. When the device is in ON state and under flatband conditions it acts as a resistor and the current through drain is expressed by

$$I_D = q\mu N_D (T_{Si}W_{Si}/L)V_{DD} \ldots\ldots\ldots\ldots(2.2)$$

where T_{Si} is the silicon thickness and N_D is the donor concentration. The current is not dependent on the capacitance of gate oxide and can be enhanced simply by increasing the dopant concentration [16] . The fluctuation of the threshold voltage is higher in FET than in ultrathin-film, inversion-mode SOI transistors. The charge carrier mobility in gated resistors is smaller than the nanowire FETs for large value of V_{GS}. But in the "weak inversion" i.e, in the subthreshold region gated resistors possess same carrier mobility as in the conventional nanowires. The JLFET gives better subthreshold slope (SS) and drain induced barrier lowering (DIBL) characteristics as compared with the MOSFETs in case of very low power logic. The short-channel effects are suppressed in JLFET by greater extent.

State	**Inversion NWT**	**Accumulation NWT**	**JLFET**
ON	Main current through inversion channels in surface	Surface Accumulation channels & low current through body	Surface Accumulation channels & high Current through body
OFF	Surface subthreshold current	Body subthreshold current	Body subthreshold current

Depleting condition of the highly doped nanowire makes electric field of a large value in the direction which is perpendicular to flow of current below threshold. But above threshold the electric field becomes zero. This is the opposite as in case of inversion-mode (IM) or accumulation mode (AM) devices, where the field is the highest during ON state of the device.

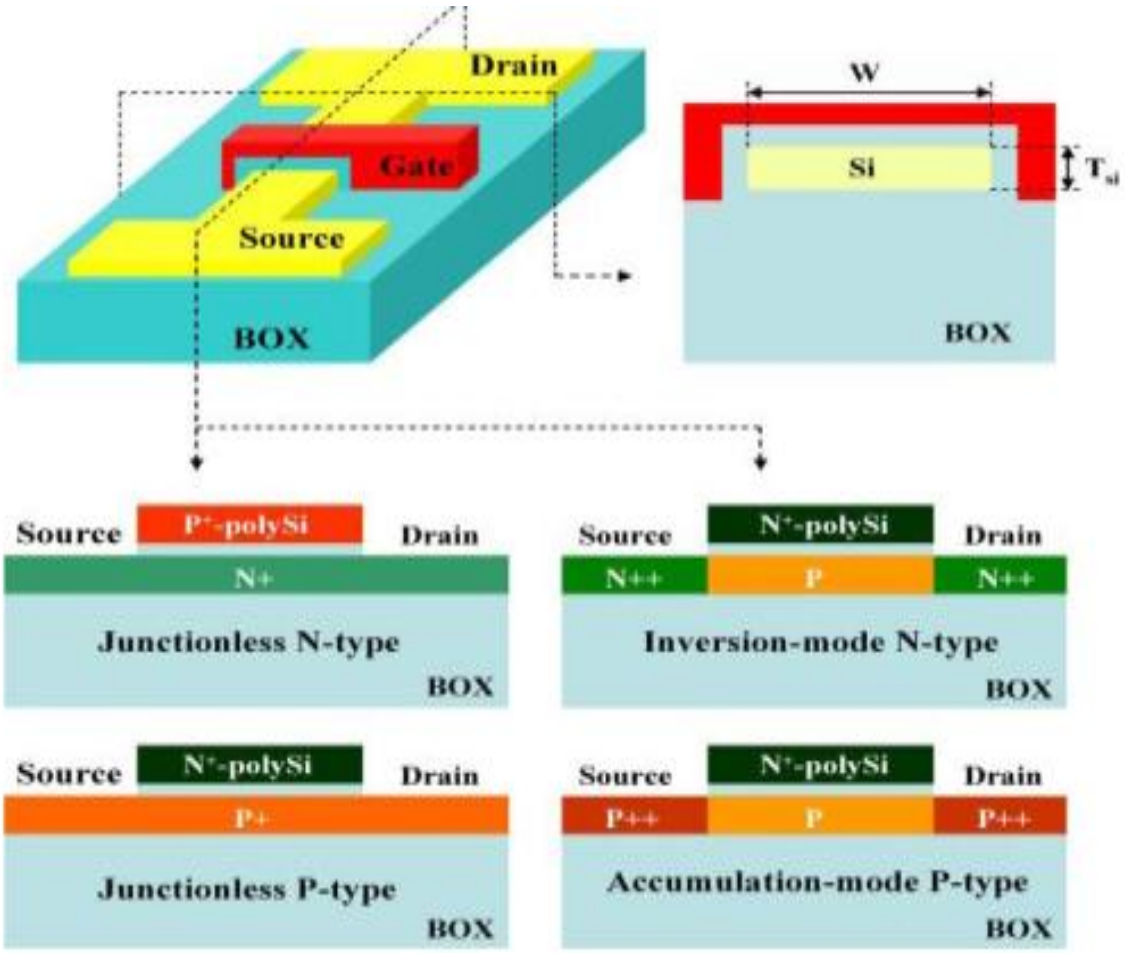

Fig 2.5 Comparison between Junctionless and Junction-Based Transistors[16]

2.2 Review of Earlier Works:

Few of existing literature on JLFET are reviewed here. The problems addressed and the findings reported in those publications are briefly compiled below:

The heavily doped n-type silicon nanowires (SiNWs) JLFETs are made by the usage of the process of self-alignment to check the direction and position of SiNWs [1]. SiNWs are produced across the drain and source which is pre-patterned under the help of the electric field applied

externally, which helps the subsequent steps of device fabrication. The JLFET shows mobility of electron ~ 90 cm^2 */Vsec*, I_{ON}/I_{OFF} ratio ~ 10^6 and subthreshold slope ~ 90 *mV/dec*. Additionally, the fluctuation of current under stress is checked. It is presented that current under stressed condition reaches maximum when the JLFET is at pinch-off state. At last, improvement in I_{OFF} by 97% and subthreshold slope by 16% using 100 *MPa* compressive stress in the n-JLFET is obtained.

The realization of $In_{0.53}Ga_{0.47}As$ JLFET is achieved for the shortest length of channel L_{CH} (7 *nm*) for any group III-V semiconductors [2]. The JLFET is made of a 1 *nm* very-thin channel which is sandwiched between a 1 *nm* indium phosphide cap and the substrate, and a highly doped raised source-drain structure. Peak value of transconductance = 1480 $\mu S/\mu m$ at V_{DS} = 0.6 *V* for an equivalent oxide thickness = 2.5 *nm* and source-drain resistance R_{SD} of 170 $\Omega.\mu m$ were achieved. Also for the first time the ballistic behavior of sub-7 *nm* group III-V semiconductors was practically investigated with the usage of a novel approach. The $In_{0.53}Ga_{0.47}As$ JLFET with L_{CH} having value 7 *nm* was observed to have a mean free path of 26 *nm* and ballistic efficiency B of 0.79.

An explicit compact model for the double-gate (DG) JLFET is presented here [3]. The expressions for the mobile channel charge density in depletion and accumulation mode are presented and the current through drain is estimated as a function of the structural parameters and voltages applied at the terminal. Validations are performed by comparison with the 2D numerical simulations.

A tri-gate $In_{0.53}Ga_{0.47}As$-on-insulator (InGaAs-OI) JLFET architecture is demonstrated [4]. The device has a 20 *nm* n-type $In_{0.53}Ga_{0.47}As$ channel with dopant density 10^{18} /cm^3 achieved by

direct wafer bonding and 3.5 *nm* Al_2O_3 gate dielectric deposited using Plasma Enhanced Atomic Layer Deposition. The impact of the width of the fin (W_{fin}) and length of gate (L_g) scaling at constant dopant density of channel (N_d) and equivalent thickness of oxide (EOT) on the performance of the devices are also discussed.

A simulation based study of Vertical Gaussian type of Doping profile is presented [5]. The said structure improves the ON - OFF current through drain ratio (by 10^5), roll off of threshold voltage (by 35 mV), Drain Induced Barrier Leakage (by 27 mV/V) and Subthreshold Slope (by 5 mV/dec for straggle parameter σ = 3.75 nm) in comparison to uniformly doped channel DG-JLFETs.

N-channel JLFETs with patch antennas have been manufactured using SOI wafers [6]. The sensor exhibits 30μv DC photo response to 0.34THz EM radiation. Measurements of their I-V characteristics and sub THz response characteristics are obtained. An ability to influence the substrate biasing has been studied.

A two-dimensional analytical model of single material symmetric Double Gate Stack-Oxide (DGS) JLFET in subthreshold region is presented. [7] This model has been studied and expected to give better subthreshold characteristics and optimize Short Channel Effects. The DGS-JLFET characteristics are compared with characteristics of the symmetric DG-JLFET made of the single material. Here said DGS-JLFET shows improved I_{ON} to I_{OFF} ratio, less Subthreshold Slope and less impact of Drain Induced Barrier Leakage when comparing with DG-JLFET.

Comparison of cylindrical double gate junctionless (CDGJLFETs) and cylindrical single gate junctionless FETs (CSGJLFETs) is presented using TCAD simulation [8]. The CDGJLFETs gives improved output than CSGJLFETs in subthreshold current, voltage of the channel, roll off

in threshold voltage, subthreshold region voltage swings due to more stringent controllability of gates on the channel.

Thermal noise in trigate junctionless field effect transistors (TG-JLFET) is presented by 3-D TCAD simulation [9]. Thermal noise enhances with conductivity of the channel. So, it is important to check the noise during maintaining good conductivity. Here fluctuation in parameters may be used to decrease thermal noise and also optimize the design of the device.Thermal noise for drain current, induced noise of gate and cross-correlation noise in TG-JLFET are investigated by TCAD.

A SiGe source-drain n-type hetero nanotube (HNT) JLFET is proposed with its enhanced performance for the sub-20 nm regime [10]. The paper demonstrates that the interface at source and channel and drain produces the discontinuity in HNT JLFET valence band which removes the impact of lateral band to band tunneling (L-BTBT) of electrons during OFF condition. Further, high-k spacers improve the performance by higher I_{ON} to I_{OFF} ratio of ~10^{11} for 6 *nm* gate length. But core gate enlarges the OFF current in NT JLFET. In HNT JLFET OFF current decreases due to DIBL and sub-threshold slope having values 3.5*mV/V* and 60*mV/decade* respectively. Further use of the HNT JLFET in analog/RF appliances has been described with the help of TCAD showing a significant gain–bandwidth product of 3.9 THz and an intrinsic gain of 31.76 dB.

Capacitance-Voltage (C-V) characteristics and the threshold voltage fluctuation of p-type Rectangular Gate Junctionless Field Effect Transistor (RG-JLFET) and Double Gate Junctionless Field Effect Transistor (DG-JLFET) is presented by employing self-consistent solver [11]. It solves Schrodinger-Poisson equations with proper boundary conditions, and considers

penetration of wave function and other quantum mechanical effects. The effect of variation of device parameter (such as thickness of channel, thickness of oxide and dopant concentration) on threshold voltage check for both structures is compared. Physical explanations are also shown.

An undoped Double gate Junctionless field effect transistor (UnDGJLFET) is characterized [12]. The device body is intrinsic. A comparative simulation on electronic performance of the undoped DGJLFET and a DGJLFET having dopant density of $10^{19}/cm^3$ have been performed in TCAD. It exhibits that the UnDGJLFET shows much lower subthreshold region swing and larger threshold voltage than the doped. For the less number of charge carrier, the ON current is much smaller for the UnDGJLFET compared to doped JLFET.

A multi gate MOSFET with high k-spacers is designed in [13]. The spacers are placed on the two gates. The characteristics of the device is studied with the high dielectric constant (k_{sp}) spacers formed from hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3) taken into consideration. The paper represents the analysis of short channel effects (SCEs) such as threshold voltage roll off, DIBL and I_{ON}/I_{OFF} ratio.

A detailed model to estimate the dc electronic behavior in very thin surrounding gate junctionless (JL) nanowire field-effect transistors is constructed in [14]. The said model takes into account 2-D geometrical and electrical carrier charge density confinement within discrete sub-bands. Mixing a parabolic approximation of the Poisson equation and the first-order perturbation theory for the Schrodinger sub-band energy eigenvalues and the Fermi–Dirac statistics for the confined charge density, solution for the dc characteristics in very thin JL devices is obtained. Validity of the model has been verified with TCAD simulations. The result is valid for all regions of operation. This shows the crucial step for circuit analysis based on JL nanowire.

A generalization for charge-based model for ultrathin DG-JLFET by including quantum electron density is presented [15]. The derivation relies on the first order correction for the infinite quantum well. For first and second quantized states, the free charge carrier distribution and current through a very thin body JLDG FET are in agreement with TCAD solution for all regions of operations.

A compact model of quantum electronic charge density at the subthreshold region is derived for junctionless (JL) double-gate (DG) FETs [19]. The proposed model is achieved for two different quantum confinement conditions. One is for a case of a thick channel and a heavily doped channel, where quantum confinement effects (QCEs) are modeled by a 1-D quantum harmonic oscillator. The other is for a case of a thin channel, where QCEs are modeled by the use of a 1-D quantum well surrounded by high potential barriers and an energy correction term coming from the depletion charge. It is shown that, regardless of the channel thickness, the quantum confinement is higher in JL than in inversion-mode (IM) DG FETs. However, for a thin channel, the quantum threshold voltage shift is less severe in JL than in IM DG FETs. The proposed model gives an analytical expression for the threshold voltage shift due to QCEs, which can be used as a quantum correction term for compact modeling.

A highly scalable and CMOS compatible double-gate junctionless field-effect transistor (DG-JLFET)-based leaky integrate-and-fire (LIF) neuron is presented for the sub-20 nm gate length[21]. DG-JLFET LIF is able to mimic biological neuronal behavior. The DG-JLFET LIF neuron shows a low threshold voltage (−0.31 V) for firing a spike and requires 1.14 pJ of energy per spike which is ∼32 times less than partially depleted silicon-on-insulator(PD-SOI) MOSFET LIF neuron.

A 2-D analytical model of a dielectric modulated trench double gate junctionless FET (DM-TDGJLFET) is developed for label-free detection of biomolecules [22]. The channel potential is obtained by solving the 2-D Poisson's equation using the parabolic approximation with appropriate boundary conditions. The drain current and threshold voltage are obtained from the minimum channel potential. The proposed DM-TDGJLFET structure has two gates which are vertically placed in separate trenches. The two cavities for biomolecules immobilization are carved in the gate oxide region.

The concept of junction-free transistor to propose and simulate the ultrathin dielectric modulated (DM) bulk-planar junctionless field-effect transistor (BP-JLFET) as a biosensor device is proposed [23]. The proposed device is incorporated with a label-free detection of neutral (proteins, enzymes, streptavidin, and APTES) and charged [deoxyribonucleic acid (DNA)] biomolecules in terms of dielectric constant (K) and charge densities (ρ). For the detection of the biomolecules, the nanocavity is formed by etching out the oxide underneath the gate dielectric at source end. The presence/absence of biomolecules has been detected by the factor of sensitivity with the immobilization of dielectric constant (K) and the charge density (ρ) in the formed nanocavity.

The electrical properties of the Double-Gate MOSFET(DG-MOSFET) which turn out to be very promising for device miniaturization below 0.1μm is investigated[25]. A compact model which accounts for charge quantization within the channel, Fermi statistics, and nonstatic effects in the transport model is worked out. The main results of this investigation are: the ideality factor in subthreshold is equal to unity, i.e., the slope of the turn-on characteristic is 60 mV/decade at room temperature; the drain-induced barrier lowering is minimized by the shielding effect of the double gate, which allows us to reduce the channel length below 30 nm; and the device

transconductance per unit width is maximized by the combination of the double gate and by a strong velocity overshoot which occurs in response to the sudden variation of the electric field at the source end of the channel, and which can be further strengthened near the drain in view of the short device length.

A closed-form solution for transcapacitances in long-channel junctionless double-gate (JL DG) MOSFET is achieved [26]. This approach, which is derived from a coherent charge-based model, was fully validated with technology computer-aided design simulations.

The technological constrains and design limitations of ultrathin body junctionless double gate MOSFET (JL DG MOSFET) are investigated [27]. Relationships between the silicon thickness and the doping concentration compatible with design requirements in terms of OFF-state-current and voltages are obtained and validated with TCAD simulations. This set of analytical expressions can be used as a guideline for technology optimization of JL DG MOSFETS.

An analytical model for the junctionless double-gate metal–oxide–semiconductor field-effect transistor (DG MOSFET) device is presented [28]. Despite some similarities with classical junction-based DG MOSFETs, the charge–potential relationships are quite different and cannot be merely mapped on existing multigate formalisms. This is particularly true for the technological parameters of interest where reported doping densitiesexceed 10^{19} cm^{-3} for 10nm and 20nm silicon channel thicknesses. Assessment of the model with numerical simulations confirms its validity for all regions of operation, i.e., from deep depletion to accumulation and from linear to saturation.

The analog properties of nMOS junctionless (JL) multigate transistors are evaluated and their performance is compared with those exhibited by inversion-mode (IM) trigate devices of similar

dimensions [30]. The study has been performed for devices operating in saturation as single-transistor amplifiers. Furthermore, this article aims at providing a physical insight into the analog parameters of JL transistors. For that, in addition to device characterization, 3-D device simulations were performed. It is shown that, depending on gate voltage, JL devices can present both larger Early voltage V_{EA} and larger intrinsic voltage gain A_V than IM devices of similar dimensions. In addition, V_{EA} and A_V are always improved in JL devices when the temperature is increased, whereas they present a maximum value around room temperature for IM transistors.

Chapter 3

Quantum Effect in JLFET

3.1 Introduction

For thin and heavily doped semiconductor short channel effect is more prominent than thick or lightly doped semiconductor. Moreover quantum mechanical effect plays crucial role for highly scaled device especially when channel thickness is beyond 10 *nm*. Length of the gate plays a crucial role as potential in longitudinal direction corresponding to the length of the gate and the wave function along the channel direction describe the the carrier transport. For large length of the gate, potential in longitudinal direction varies slowly. For this inter-valley carrier mixing, tunneling and other quantum mechanical effects can be neglected easily without any change in performance. If the gate length reduces, the variation of the longitudinal potential becomes significant. Quantum tunneling within the source- drain region dominates. So for very small length of the gate the quantum mechanical transport model is significantly different from the classical one. The gate oxide thickness also plays critical role for consideration of quantum effect. The ultrathin oxide layer lowers the thickness of the energy barrier separating the gate and the channel, making it easier for carriers to tunnel within the insulator layer. When the thickness of gate oxide reduces to 3 *nm* or less, direct mode of tunneling prevails through the layers of the oxide and circuit performance degrades significantly, eventually making the device unstable.

3.2 Concept of Quantum Effect

When the device dimension is very small i.e. comparable with the wavelength of electron motion of electron is restricted along this dimension and this is called quantum size effect.

According to wave mechanics a particle in a system is described by a wave function. Wave function contains all knowable information about the system. The function and its space derivative must be finite, continuous and single valued.

Here we are going to consider infinite quantum well.

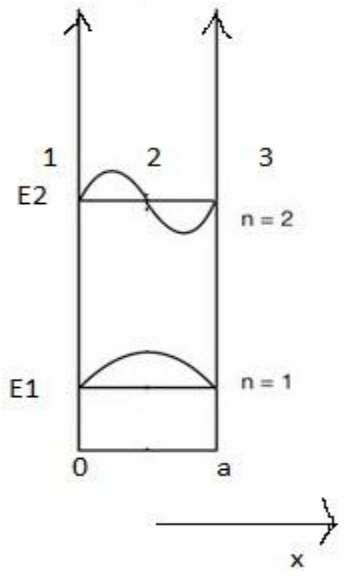

Fig 3.1 Infinite Quantum Well

The potential for the regions can be expressed as –

$V(x) = 0,\ 0<x<a$

$V(x) =$ infinite, otherwise.

Time independent Schrodinger Wave Equation is expressed as-

$$-\left(\frac{h^2}{8m\pi^2}\right)\frac{d^2\varphi(x)}{dx^2} + V(x)\,\varphi(x) = E\,\varphi(x) \text{.....(3.1)}$$

where, h = Planck's constant

E = Energy of the particle

m = Effective mass of carrier

For region 2:

$$\varphi(x) = A_1 \sin kx + B_1 \cos kx \text{.....(3.2)}$$

Considering continuity of wave function and finite product of $V(x)$ and $\varphi(x)$, $\varphi(x) = 0$ for region 1 and 3.

So, $\varphi(x) = 0$ for x = 0 and x = a.

Hence, B_1 must be zero.

So, $\varphi(x) = A_1 \sin kx$ for region 2.

Also, $A_1 \sin ka = 0$

$i.e.\ \sin ka = 0$

$i.e.\ ka = n\pi$

$i.e.\ k = n\pi/a$ *for* $n=1,2,3\ldots\ldots$

Hence $\varphi(x) = A_1 \sin(n\pi x/a)$ .....(3.3)

Eigen Energy value, $E_n = \left(\frac{h^2}{8m\pi^2}\right)\left(\frac{n\pi}{a}\right)^2$…….(3.4)

Density of States for Quantum Well:

$N_{2D}(E) = \left(\frac{4\pi m}{h^2}\right)\sum_{n=1}^{n_{max}} H(E - E_n)$……..(3.5)

Here H(E- E_n) = 1 for E≥ E_n

= 0 for E<E_n

The average no. of electrons that occupy each state per unit volume,

$n_0 = \left(\frac{4\pi m k_B T}{h^2 d_z}\right)\sum_{n=1}^{n_{max}} F_0(\eta_n)$……(3.6)

where, $F_0(\eta_n)$ = Fermi Integral of order zero with argument η_n,

k_B = Boltzman's Constant,

T = Absolute Temperature,

d_z = Dimension along z-direction

$\eta_n = (E_F - E_n)/k_BT$,

E_F = Fermi Energy Level

General form of Fermi Integral of order j with argument η is –

$$F_j(\eta) = \int_0^{\infty} \frac{(\varepsilon^j d\varepsilon)}{\{1 + \exp(\varepsilon - \eta)\}} = \left(\frac{1}{\Gamma(j+1)}\right)$$

where, $\eta = (E_F - E_C)/k_BT$,

$\varepsilon = (E-E_C)/k_BT$

3.3 Influence of Quantum Effect on Charge Density in JLFET

As already discussed, the modes of operation of the JLFET may be of three types – depletion, accumulation and hybrid.

- When the channel is in depletion mode, the voltage at gate-source satisfies $V_{GS} < V_{FB,S}$ where $V_{FB,S}$ refers to the flat-band voltage in the source. This is given by [15]

$$V_{FB,S} = \varphi_{ms} + U_T \ln(N_D/n_i) \text{.....(3.7)}$$

where φ_{ms} = Metal-semiconductor work function difference, U_T = Thermal potential = k_BT/q, k_B = Boltzman's constant, T = Absolute temperature, q = Electronic charge, N_D = Channel doping, n_i = Intrinsic carrier concentration

- When the whole channel is in accumulation, $V_{GS} > V_{FB,D,}$ where $V_{FB,D}$ refers to the flat-band voltage in the drain. It is given by

$$V_{FB,D} = V_{DS} + \varphi_{ms} + U_T \ln(N_D/n_i) \text{.....(3.8)}$$

- Within these two distinct states there lies a hybrid state.

Figure below shows the structure of n-type DG JLFET. Here we assume the channel quantization along the channel thickness i.e. in x-direction.

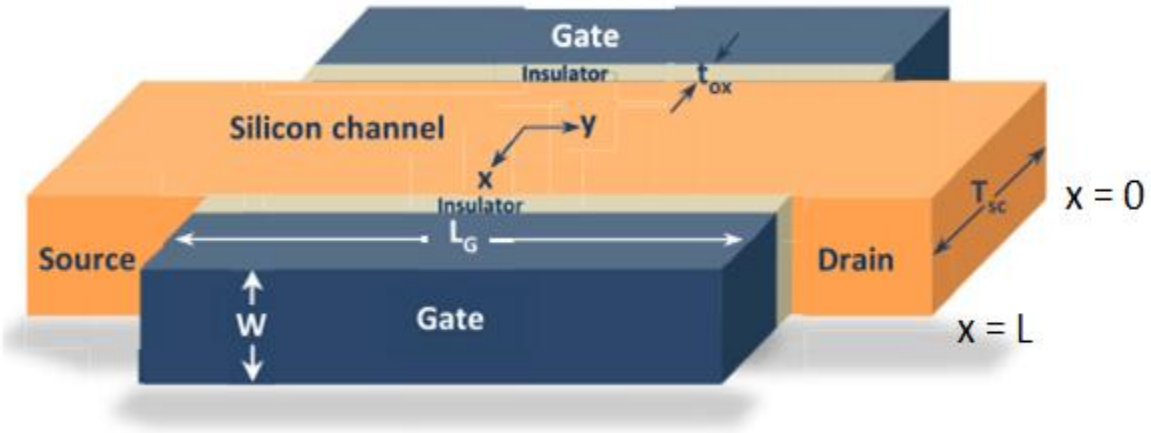

Fig 3.2 Schematic of an n-type DG Junctionless FET[15]

3.3.1 Modelling

According to Baccarani and Reggiani, for very thin channels, subband energy states which are discrete can be determined by a first-order correction which is based on the time independent perturbation.

Quantized subband energies = $E_{c0} + \{ (nh)^2/(8m^*_{c,k} T_{sc}^2)\}$….(3.9)

First order correction term = $(Qq_{sc}T_{sc}/24\varepsilon_{Si})[1-\{6/(n\pi)^2\}]$…(3.10)

Using equation (3.9) and (3.10) The final subband energy states can be expressed as:

$E_{n,k}=E_{c0}+\{(nh)^2/(8m^*_{c,k}T_{sc}^2)\}+(Qq_{sc}T_{sc}/24\varepsilon_{Si})[1-\{6/(n\pi)^2\}]$….(.3.11)

where E_{c0} stands for the conduction band edge energy at x = 0, ψ_0 refers to the central potential of the channel, n is the subband number and k is the valley number, ε_{Si} is the permittivity of Si.

As we consider quantization in (100) orientataion, quantization occurs in only two conduction band valleys in Si and remaining four valleys are not quantized.

The lowest valley (k = 1) is twofold degenerate ($g_1 = 2$) with $m^*_{c,1} = 0.92m_0$, where m_0 is considered the free electron mass.

The higher valley (k = 2) is fourfold degenerate ($g_2 = 4$) with $m^*_{c,2} = 0.19m_0$.

The total semiconductor charge density per unit area, Q_{sc} is given as –

$$Q_{sc} = Q_{fix} + Q_{QM} \quad \text{.....(3.12)}$$

where Q_{QM} and Q_{fix} ($Q_{fix} = q\ N_D T_{sc}$.....(3.12a)) correspond to respectively the mobile charge density and the fixed charge density per unit area.

The quantized mobile charge density per unit area, Q_{QM}, is the sum of charges in quantized subbands. According to equation (3.5), (3.6), (3.11), (3.12) and (3.12a) , it becomes

$$Q_{QM} = - q\sum_n\sum_k g_k N_k ln\ [1+exp\{(-E_{n,k}+E_{f,n})/k_BT\}]$$

$$=-q\sum_n\sum_k g_k N_k ln[1+exp\{(-E_{n,k}+E_{c0}-E_{c0}+E_{f,n})/k_BT\}] \quad \text{.....(3.13)}$$

Here $N_k = 4\pi m^*_{d,k} k_BT/h^2$ is the 2-D effective density of states of the subband of energy $E_{n,k}$. $m^*_{d,1} = 0.19m_0$ and $m^*_{d,2} = 0.417m_0$ are Densitiey of States(DOS) effective masses for valleys 1 and 2 respectively.

E_{fn} stands for the quasi-Fermi energy of electron. It is related to potential at the channel(V_{ch}) as –

$$E_{fn} - E_{c0} = q\ \psi_0 - qV_{ch} + k_BT\ ln(n_i/N_c) \quad \text{.....(3.14)}$$

where N_c stands for the conduction band effective density of states. Here we are considering that almost all charges are distributed in only subbands 1 and 2.

Using equations (3.11) and (3.14) in equation (3.13) we get-

$$Q_{QM} = - q\sum_n\sum_k g_k N_k ln\ [1+exp\{(\ q\ \psi_0 - qV_{ch} + k_BT\ ln(n_i/N_c))/k_BT\}$$

$$exp\{-(nh)^2/(8m^*_{c,k}\ T_{sc}^2 U_T) - (Q_{sc}/24C_{sc}\ U_T)\ [1-\{6/(n\pi)^2\}]\}$$

$$= - q\sum_n\sum_k g_k N_k ln\ \{1+(\ n_i/N_c)exp(-(nh)^2/(8qm^*_{c,k}\ T_{sc}^2 U_T)$$

$$-(Q_{sc}/24C_{sc}\ U_T\ )[1-\{6/(n\pi)^2\}] + (\psi_0 - V_{ch})/U_T)\} \ldots\ldots (3.15)$$

Here C_{sc} = Channel Capacitance Per Unit Area = ε_{Si}/T_{sc}.

Putting the value of Q_{QM} of equation (3.15) in equation (3.12) we get –

$$Q_{sc} = qN_DT_{sc} - q\sum_n\sum_k g_k N_k ln\ \{1+(\ n_i/N_c)exp(-(nh)^2/(8qm^*_{c,k}\ T_{sc}^2 U_T)$$

$$-(Q_{sc}/24C_{sc}U_T)[1-\{6/(n\pi)^2\}]+(\psi_0-V_{ch})/U_T)\} \ldots\ldots\ldots (3.16)$$

The boundary condition achieved from the continiuity of displacement vector at Si-SiO_2 interface runs as –

$$V_{GS} - \Delta\ \varphi_{ms} - \psi_s = - Q_{sc}/2C_{ox} \ldots\ldots\ldots\ldots\ldots (3.17)$$

where ψ_s is the potential at the surface of the channel,

$C_{ox} = \varepsilon_{ox}/T_{ox}$ = oxide capacitance per unit area where ε_{ox} is oxide permittivity,

$\psi_s - \psi_0 = - (Q_{sc}\ /8C_{sc}) - Q_{b1}/2\pi^2\ C_{sc} \ldots\ldots\ldots\ldots\ldots\ldots$(3.18), with ψ_0 as central potential

Q_{b1} corresponds to contribution of the first subband towards mobile charge density.

$Q_{b1} = \beta(Q_{sc} - Q_{fix})$……..(3.19)

Here β represents the fraction of the first subband mobile charge density to the total mobile charge density.

Adding equations (3.17) & (3.18) and using equation (3.19), we get –

$$V_{GS} - \Delta\varphi_{ms} - \psi_0 = -(Q_{sc}/8C_{sc}) - (\beta Q_{sc}/2\pi^2 C_{sc}) - (Q_{sc}/2C_{ox}) + (\beta Q_{fix}/2\pi^2 C_{sc})$$……..(3.20)

Now combining the equations (3.16) and (3.20) and considering $V_{ch} = 0$ we get –

$$Q_{sc} = qN_D T_{sc} - q\sum_n\sum_k g_k N_k ln\{1+(n_i/N_c)exp(-(nh)^2/(8qm^*_{c,k} T_{sc}^2 U_T) - (Q_{sc}/24C_{sc} U_T)[1-\{6/(n\pi)^2\}] + [V_{GS}-\Delta\varphi_{ms}+(Q_{sc}/8C_{sc})+(\beta Q_{sc}/2\pi^2 C_{sc})+(Q_{sc}/2C_{ox}) -(\beta Q_{fix}/2\pi^2 C_{sc})]/U_T)$$ ……(3.21)

3.3.2 Simulation

The prime focus of this chapter is to investigate the influence of variations in channel thickness (T_{sc}) and channel doping (N_d) on the fixed and total charge density in the channel, and thereby, on the variation of the threshold voltage of the JLFET.

Values of various parameters considered for simulation are given below:

q, Electronic charge = $1.6*10^{-19}$ C,

n_i,Intrinsic carrier concentration in Si at T = 200K = $1.5*10^{16} m^{-3}$,

N_c, Conduction band Density of states = $2.81*10^{25} m^{-3}$,

h, Planck constant = $6.63*10^{-34}$ J/Hz,

U_T, Thermal potential = 0.026 V,

t_{ox}, Oxide thickness = 2 nm,

ε_{Si} , Permittivity of Si = $1.03368 * 10^{-10}$ F/m,

ε_{ox} , Permittivity of oxide = $3.4515 * 10^{-11}$F/m,

$V_{GS} - \Delta \varphi_{ms}$, Difference between gate source potential difference and metal-semiconductor work function difference = 0.4 V,

g_1 , No. of valley quantized = 2,

g_2 , No. of valley not quantized = 4,

N_1 , Two dimensional effective DOS for the first subband = $2.0463*10^{16} m^{-3}$,

N_2 , Two dimensional effective DOS for the second subband = $4.4912*10^{16} m^{-3}$,

$m^*_{c,1}$, Lower valley carrier effective mass = $0.92m_0 = 8.372*10^{-31}$ kg,

$m^*_{c,2}$, Upper valley carrier effective mass = $0.19\ m_0 = 1.729*10^{-31}$ kg,

m_0 = Free electron mass = $9.1*10^{-31}$ kg.

A. Variation of Charge Density with Channel Thickness in Absence and Presence of the Quantum Effect:

Here channel thickness(T_{sc}) is varied from 4*nm* to 8*nm* for three different channel doping(N_d) i.e. $10^{21}m^{-3}$, $10^{22}m^{-3}$ and $10^{23}m^{-3}$. The variation of fixed charge density in absence of quantum effect and total charge density in presence of quantum effect are presented as function of channel thickness using equation (3.12a) and (3.21).

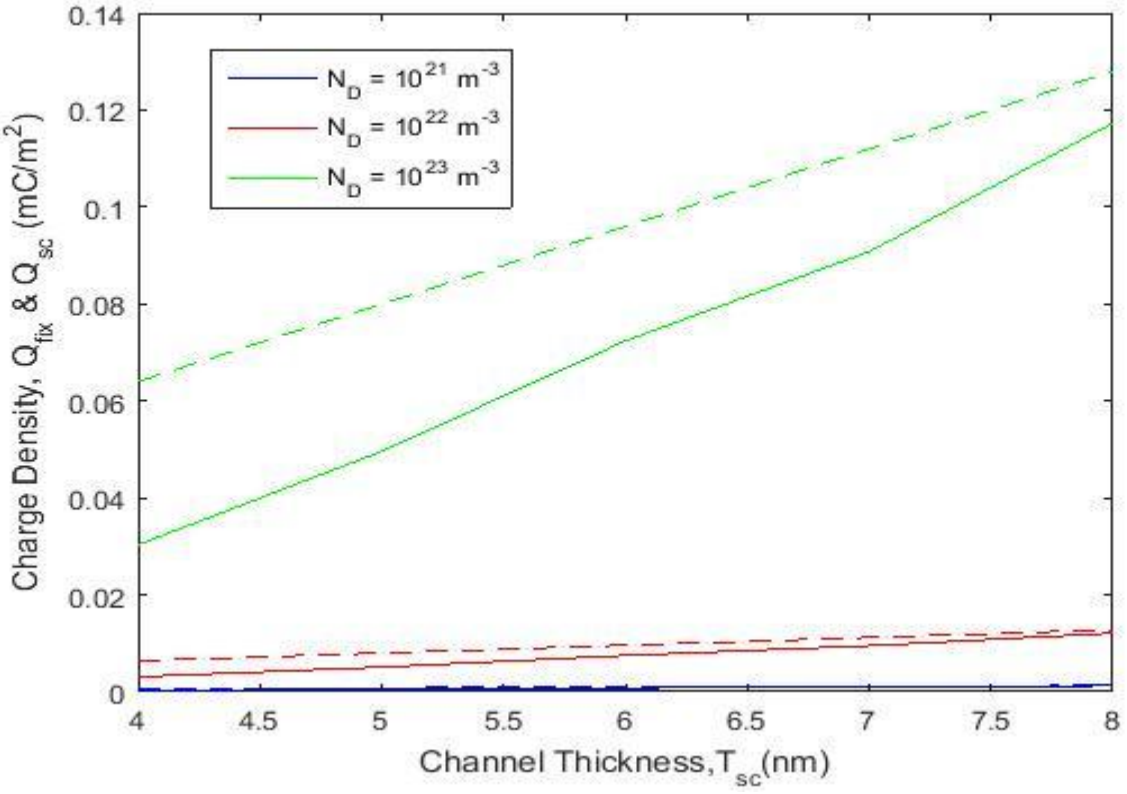

Fig 3.3: Charge Density vs Channel Thickness in Absence(broken) and Presence(solid) of the Quantum Effect in DG JLFET

Here we can see that total charge density including quantum effect is lower than fixed charge density. Also reduction in total charge density is more prominent in DG JLFET of smaller channel thickness.

B. Variation of Charge Density with Channel Doping in Absence and Presence of Quantum Effect:

Here channel thickness (T_{sc}) is kept constant at three different values i.e. 4 *nm*, 6 *nm* and 8*nm*. For three different channel thickness Channel doping (N_d) is varied from $10^{20}m^{-3}$ to $10^{25}m^{-3}$. The variation of fixed charge density in absence of quantum effect and total charge density in presence of quantum effect are presented as function of channel doping using equation (3.12a) and (3.21).

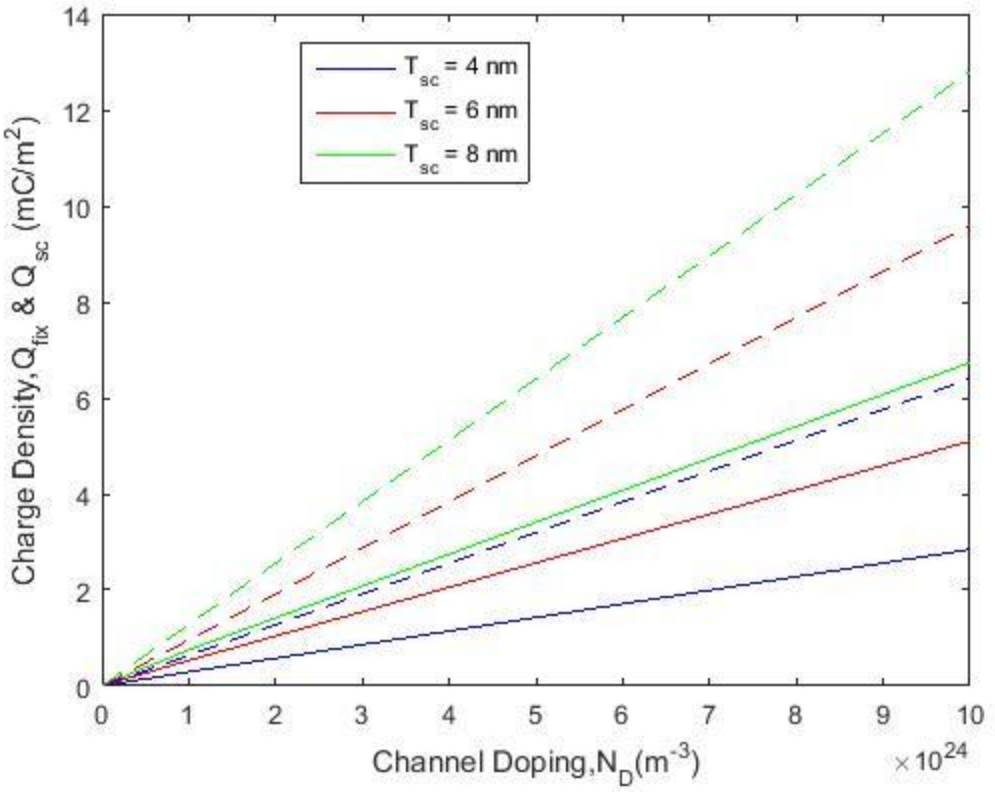

Fig 3.4: Charge Density vs Channel Doping in Absence(broken) and Presence(solid) of the Quantum Effect in DG JLFET

Here we can see that total charge density including quantum effect is lower than fixed charge density. Also reduction in charge density is more in higher doping concentration than lower doping concentration.

3.4 Influence of Quantum Effect on Threshold Voltage Shift in JLFET:

3.4.1 Modelling

Due to quantum effect charge density as is lower in case of thin and heavily doped channel as compared with thick and lightly doped channel. This gives a higher threshold voltage shift in thin and heavily doped channel. Threshold voltage shift can be obtained by comparing the fixed charge density with total charge density. The formula to calculate this is as mentioned below [19]

$\Delta V_{th} = (k_B T/q)\ln(Q_{fix}/Q_{sc})$……..(3.22)

3.4.2 Simulation

A. Variation of Threshold Voltage Shift with Channel Thickness in Presence of the Quantum Effect:

The channel doping , (N_d) is kept constant at $10^{21} m^{-3}$, $10^{22} m^{-3}$ *and* $10^{23} m^{-3}$. Channel thickness is varied from 4 *nm* to 8 *nm*.

The threshold voltage shift due to quantum effect is plotted against channel thickness for different doping using equation (3.22) -

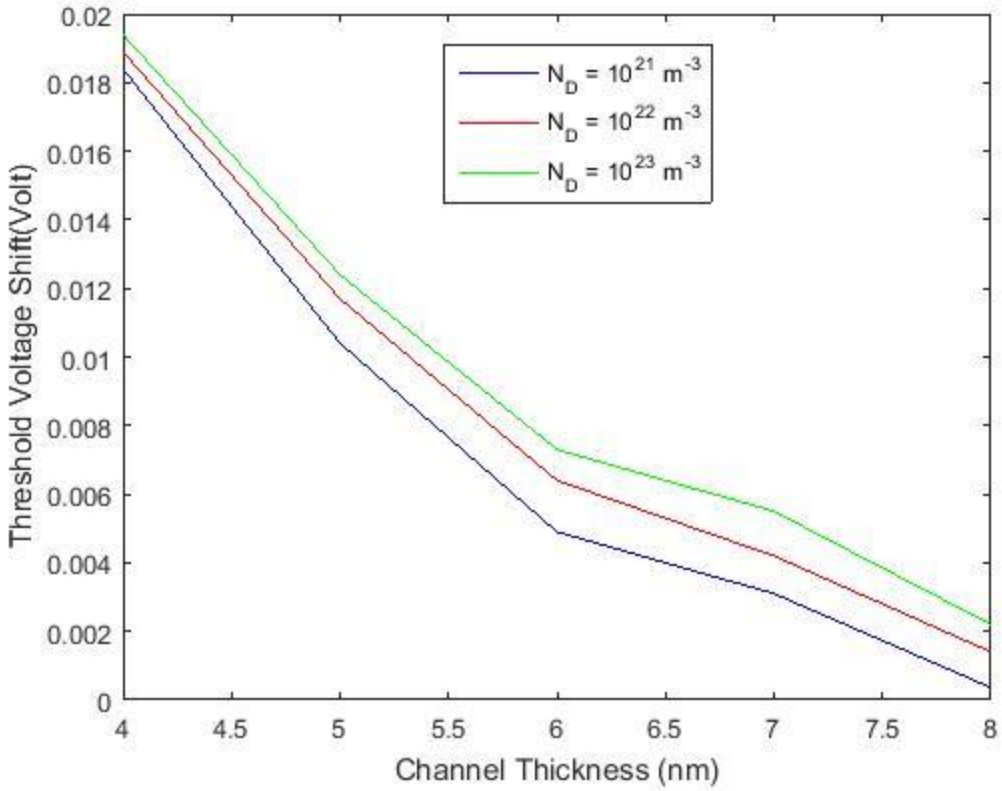

Fig 3.5 Threshold Voltage Shift vs Channel Thickness in Presence of Quantum Effect

In thin channel JLFET, the Quantum effect becomes more prominent as the subband energies themselves are higher and the interband separations are also larger. Electron redistribution over various subbands in the conduction band of the channel material vary widely from that in case of a JLFET with a relatively thick channel. The threshold voltage shift gets influenced accordingly as evident from the derived expression.

B. Variation of Threshold Voltage Shift with Channel Doping in Presence of the Quantum Effect:

Fig 3.6 presents variation of threshold voltage shift with channel doping for different thickness of JLFET channel using equation (3.22) -

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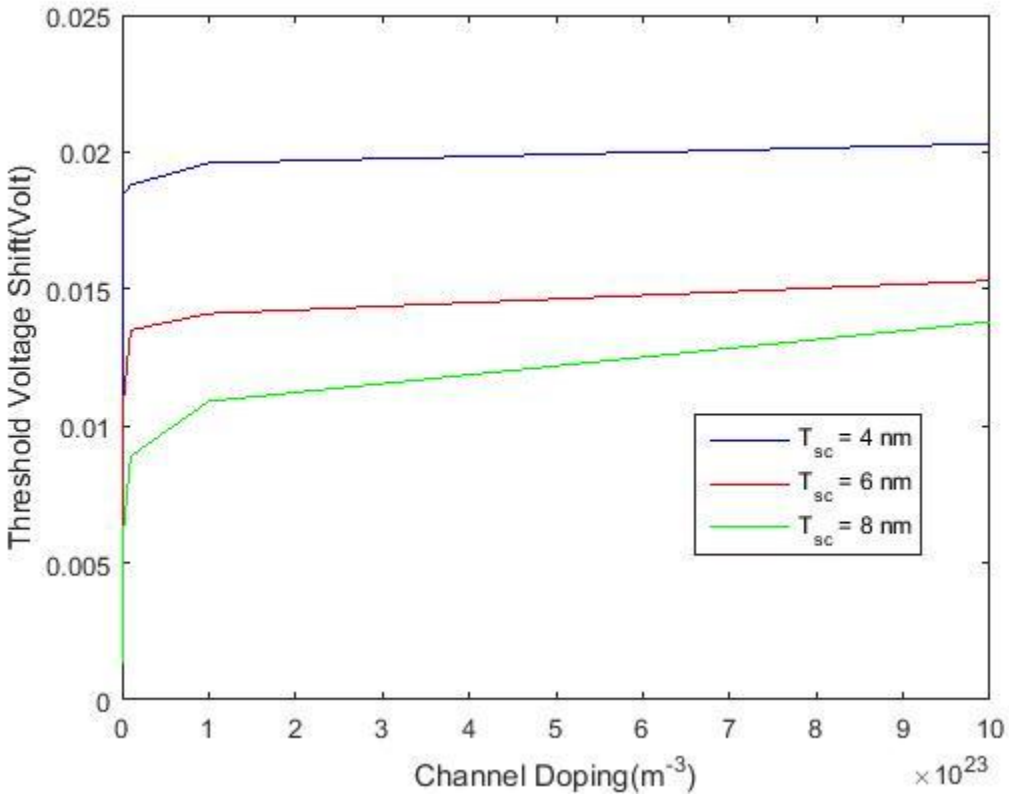


Fig 3.6 Threshold Voltage Shift vs Channel Doping in Presence of Quantum Effect

In heavily doped JLFET, the quantum effect becomes more prominent as more no. of charge carriers are quantized due to high degeneracy. So total charge density is reduced significantly and as a result of this threshold voltage shift is higher for larger channel doping.

3.5 Influence of Quantum Effect on ON Current in JLFET:

3.5.1 Modelling

Here we are considering only the impact of the first subband charge density only for estimating ON current as the contribution of other subbands on charge density is almost negligible.

If we rely on drift-diffusion transport model and consider uniform charge density the ON current can be given as [15] -

$$I_{ON} = [\left(\frac{W}{L_G}\right)\{(\mu_n Q_{fix}) - \mu_n \left(\frac{\alpha}{2}\right) Q_{sc}^2 + \mu_n U_T Q_{sc} + \mu_n U_T Q_{fix} \ln\left(1 - \frac{Q_{sc}}{Q_{fix}}\right)\}]$$

…….(3.23)

where, W = Channel wideth,

L_G = Channel length,

μ_n = Electron mobility,

$$\alpha = [\frac{1}{8C_{sc}} + \frac{\beta}{2\pi^2 C_{sc}} + \frac{1}{2C_{ox}} - \frac{1}{24C_{sc}}\left(1 - \frac{6}{\pi^2}\right)]$$

3.5.2 Simulation

Here we want to investigate variation of ON current(I_{ON}) on channel thickness(T_{sc}) and donor concentration(N_d).

Values of various parameters considered for simulation are given below:

W, Channel wideth = 1μm,

L_G, Channel length = 1μm,

μ_n, Electron mobility = 0.11 m^2/ V-sec

A. Variation of ON Current with Channel Thickness in Presence of the Quantum Effect:

Here channel thickness (T_{sc}) is varied from 4*nm* to 8*nm* for three different channel doping (N_d) i.e. $10^{21}m^{-3}$, $10^{22}m^{-3}$ and $10^{23}m^{-3}$. The variation of ON current in presence of quantum effect is presented as function of channel thickness using equation (3.23).

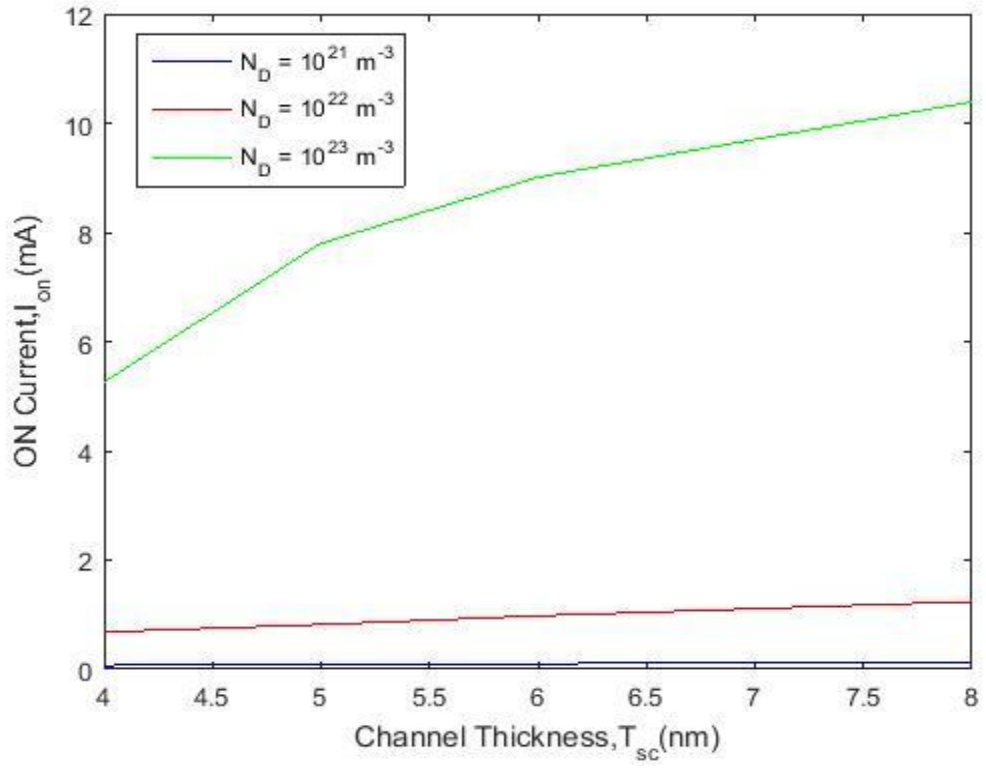


Fig 3.7 ON Current vs Channel Thickness in Presence of Quantum Effect

Here we can observe that ON current increases with increase in channel thickness as charge density increases with increase in channel thickness. ON current is higher for higher donor concentration as higher dopant density results in higher charge density.

B. Variation of ON Current with Channel Doping in Presence of the Quantum Effect:

Here channel thickness (T_{sc}) is kept constant at three different values i.e. 4 *nm*, 6 *nm* and 8*nm*. For three different channel thickness Channel doping (N_d) is varied from $10^{20}m^{-3}$ to $10^{23}m^{-3}$. The variation of ON current in presence of quantum effect is presented as function of channel doping using equation (3.23).

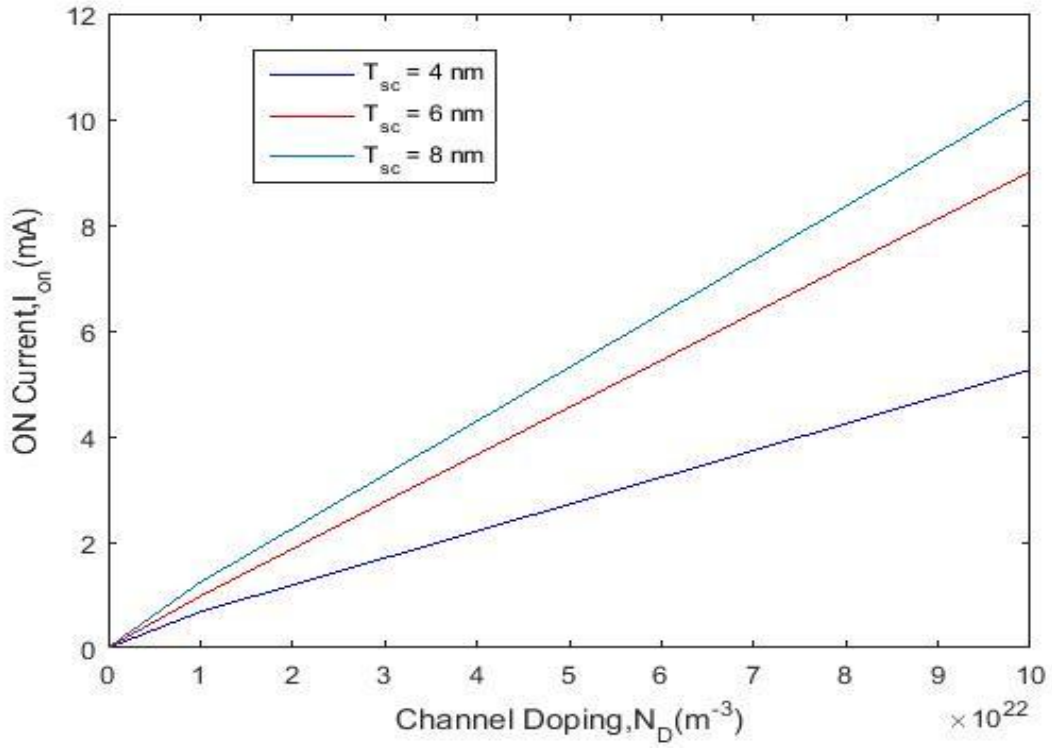


Fig 3.8 ON Current vs Channel Doping in Presence of Quantum Effect

Here we can see that ON current increases with increase in channel doping as charge density increases with increase in channel doping. ON current is higher for higher channel thickness as higher channel thickness results in higher charge density.

Chapter 4

Various Circuits Based on JLFET and Their Performance Evaluation

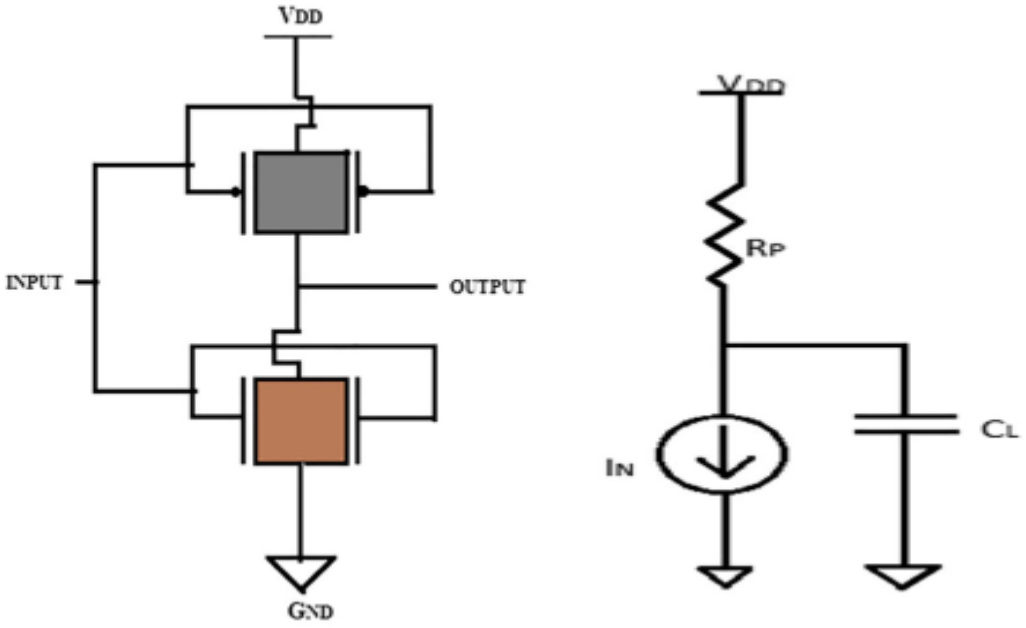
JLFET is a special kind of FET where no concentration gradient appears between source and drain. Uniform doping is maintained throughout the cross-section. As the doping is constant there is no physical junction present in the device. All the circuits representing basic logic gates like inverter, NAND gate, NOR gate, etc can be realized using JLFET. As structure of JLFET is different from that of MOSFET, the performance evaluation of the circuits based on JLFET becomes different. In this chapter various circuits based on JLFET will be studied. The power, delay and power-delay product for those circuits will be investigated and compared.

4.1 JLFET Inverter

A basic inverter will be investigated first.

4.1.1 Structure

Inverter consists of a p-type JLFET and a n-type JLFET. For logic – 0 input n-type JLFET acts as a current source and p-type JLFET acts as a resistor. Here we focus at only subthreshold region of operation.



a) *b)*

Fig 4.1 JLFET Inverter[18]: a)Schematic Diagram, b)Equivalent Circuit Diagram

4.1.2 Estimation of Static Power Dissipation

To estimate the static power dissipation, the drain current for an n-type is first considered. The equation of drain current is –

$I_N = k_N (W/L)_N \exp((V_{GS} - V_{TH})/V_T)(1 – \exp(V_{DS}/V_T))$

Here $V_{TH} = V_{TH0} - \lambda_{DS}V_{DS} + \Delta V_{TH,Q}$

So,

$I_N = k_N (W/L)_N \exp((V_{GS}-V_{TH0}+\lambda_{DS}V_{DS} -\Delta V_{TH,Q})/V_T)(1 – \exp(V_{DS}/V_T))$

$= \beta \exp(V_{GS}/V_T)(1 – \exp(V_{DS}/V_T))$

Here , $\beta = k_N (W/L)_N exp[(-V_{TH0} + \lambda_{DS} V_{DS} - \Delta V_{TH,Q})/V_T]$

$R_P = |dV_{DS}/dI_N|$

$I_N = \beta exp(V_{GS}/V_T)(1 - exp(V_{DS}/V_T))$

$\approx \beta exp(V_{GS}/V_T)(1 - 1 - (V_{DS}/V_T))$

$dI_N/dV_{DS} = - (\beta/ V_T) exp(V_{GS}/V_T)$

$R_P = V_T/ \beta exp(V_{GS}/V_T)$

Applying KCL we can get as -

$C_L (dV_{out}/dt) + I_N = (V_{DD} - V_{out})/ R_P$

After rearranging we can get as –

$R_P C_L (dV_{out}/dt) + I_N R_P = V_{DD} - V_{out}$

i.e. $R_P C_L (dV_{out}/dt) = V_{DD} - V_{out} - I_N R_P$

i.e. $R_P C_L \int_{\Delta V}^{V_{DD}-\Delta V} (dV_{out}/(V_{DD} - V_{out} - I_N R_P)) = \int_0^T dt$

i.e. $-R_P C_L \int_{\Delta V}^{V_{DD}-\Delta V} (d(V_{DD} - V_{out} - I_N R_P)/(V_{DD} - V_{out} - I_N R_P)) = \int_0^T dt$

i.e. $- R_P C_L ln|(V_{DD} - (V_{DD} - \Delta V) - I_N R_P)/ (V_{DD} - \Delta V - I_N R_P)| = T$

i.e. $V_{DD} - V_{DD} + \Delta V - I_N R_P = (V_{DD} - \Delta V - I_N R_P) exp(-T/R_P C_L)$

i.e. $\Delta V (1 + exp(-T/R_P C_L)) = V_{DD} exp(-T/R_P C_L) + I_N R_P (1 - exp(-T/R_P C_L))$

As we know that,

$T >> R_P C_L$, $exp(-T/R_P C_L) \rightarrow 0$

So , $\Delta V = I_N R_P$

$P = (\Delta V)^2 / R_P$……(4.1)

4.1.3 Estimation of Propagation Delay

Now we want to estimate the time taken by a signal to propagate from input to output. For this we need to apply KCL at the output node. Applying that rule at the output node of the JLFET we can get –

$C_L (dV_{out}/dt) + I_N = (V_{DD} - V_{out})/ R_P$

i.e. $R_P C_L (dV_{out}/dt) + I_N R_P = V_{DD} - V_{out}$

i.e. $R_P C_L \int_0^{\Delta V} (dV_{out} / (V_{DD} - V_{out} - I_N R_P)) = \int_0^T dt$

i.e. $- R_P C_L ln|(V_{DD} - \Delta V - I_N R_P)/ (V_{DD} - I_N R_P)| = T$

i.e. $T = R_P C_L ln|(V_{DD} - I_N R_P)/ (V_{DD} - \Delta V - I_N R_P)|$ ……..(4.2)

4.1.4 Estimation of Power Delay Product

Power Delay Product (PDP) is product of static power dissipation and propagation delay. Therefore, from derivations presented in above two subsections, the product becomes

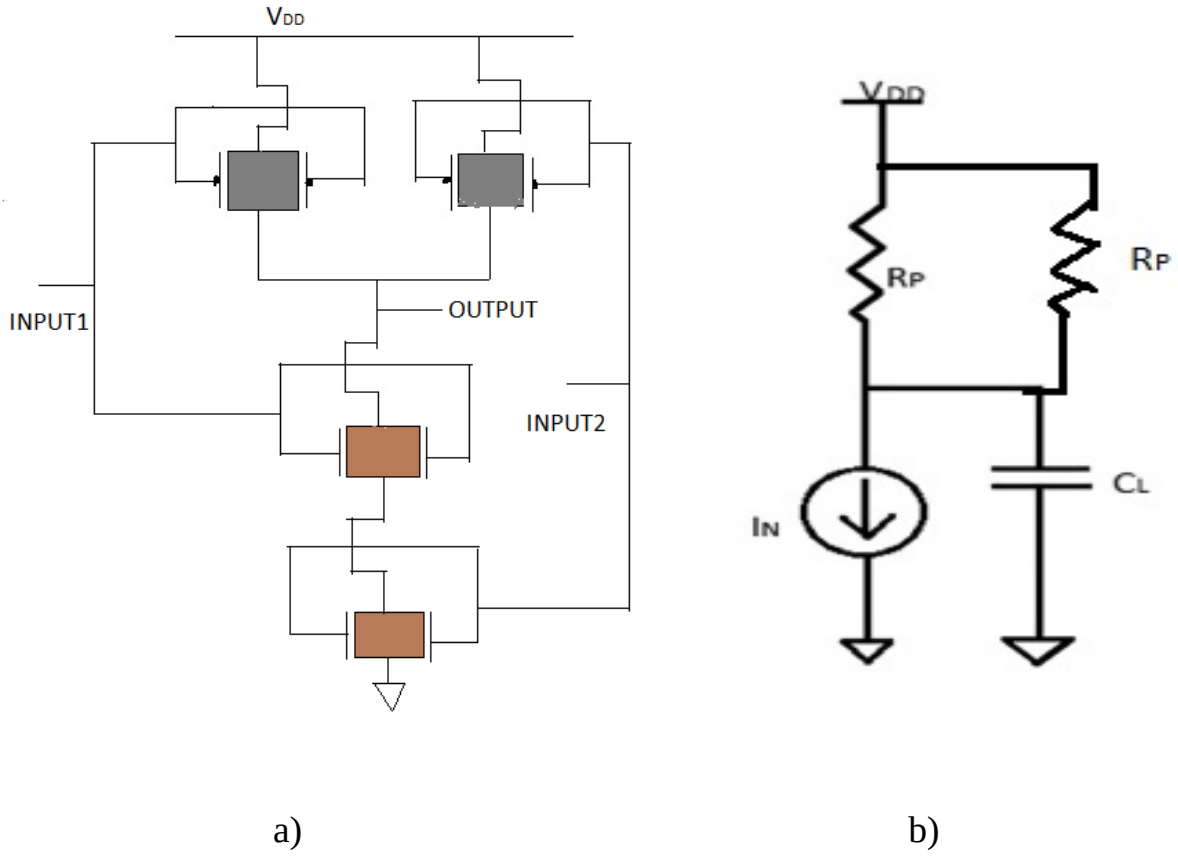
PDP = P*T = $(\Delta V)^2 C_L ln|(V_{DD} - I_N R_P)/ (V_{DD} - \Delta V - I_N R_P)|$ ……..(4.3)

4.2 JLFET NAND Gate

The universal logic gate NAND is next studied.

4.2.1 Structure

Schematic diagram of JLFET NAND gate is prescribed in fig. 4.3. NAND gate consists of two p-type JLFET connected in parallel and two n-type JLFET connected in series. For logic – 0 input n-type JLFET acts as a current source and p-type JLFET acts as a resistor. Here we shall concentrate at only subthreshold region of operation. Equivalent circuit diagram is presented in fig 4.4.



a) b)

Fig 4.2 JLFET NAND Gate: a) Schematic Diagram, b)Equivalent Circuit Diagram

4.2.2 Estimation of Static Power Dissipation

The equation of drain current for n-type FET can be expressed as –

$I_N = k_N (W/L)_N \exp((V_{GS} - V_{TH})/V_T)(1 – \exp(V_{DS}/V_T))$

Here $V_{TH} = V_{TH0} - \lambda_{DS}V_{DS} + \Delta V_{TH,Q}$

So,

$I_N = k_N (W/L)_N \exp((V_{GS} - V_{TH0}+\lambda_{DS}V_{DS}-\Delta V_{TH,Q})/V_T)(1– \exp(V_{DS}/V_T))$

$= \beta\exp(V_{GS}/V_T)(1 – \exp(V_{DS}/V_T))$

Here , $\beta = k_N (W/L)_N \exp((-V_{TH0} +\lambda_{DS}V_{DS} -\Delta V_{TH,Q})/V_T)$

$R_{P1} = |dV_{DS}/dI_N|$

$I_N = \beta\exp(V_{GS}/V_T)(1 – \exp(V_{DS}/V_T))$

$\approx \beta\exp(V_{GS}/V_T)(1 – 1 - (V_{DS}/V_T))$

$dI_N/dV_{DS} = - (\beta/ V_T) \exp(V_{GS}/V_T)$

$R_{P1} = V_T/ \beta\exp(V_{GS}/V_T)$

Applying KCL we can get as -

$C_L (dV_{out}/dt) + I_N = (V_{DD} - V_{out})/ R_{P1}$

After rearranging we can get as –

$R_{P1} C_L (dV_{out}/dt) + I_N R_{P1} = V_{DD} - V_{out}$

i.e. $R_{P1}\, C_L\, (dV_{out}/dt) = V_{DD} - V_{out} - I_N\, R_{P1}$

i.e. $R_{P1} C_L \int_{\Delta V}^{V_{DD}-\Delta V} (dV_{out}/(V_{DD} - V_{out} - I_N R_{P1})) = \int_0^T dt$

i.e. $-R_{P1} C_L \int_{\Delta V}^{V_{DD}-\Delta V} (d(V_{DD} - V_{out} - I_N R_{P1})/(V_{DD} - V_{out} - I_N R_{P1})) = \int_0^T dt$

i.e. $T = R_{P1}\, C_L ln|(V_{DD} - (V_{DD} - \Delta V) - I_N\, R_{P1})/ (V_{DD} - \Delta V - I_N\, R_{P1})|$

i.e. $V_{DD} - V_{DD} + \Delta V - I_N\, R_{P1} = (V_{DD} - \Delta V - I_N\, R_{P1})exp(-T/R_{P1}C_L)$

i.e$\Delta V\,(1+exp(-T/R_{P1}C_L))=V_{DD}exp(-T/R_{P1}C_L)+I_N R_{P1}(1-exp(-T/R_{P1}C_L))$

As we know that,

$T >> R_{P1}C_L$, $exp(-T/R_{P1}C_L) \rightarrow 0$

So , $\Delta V = I_N\, R_{P1}$

$P = (\Delta V)^2 / R_{P1}$

Here, $R_{P1} = R_P/2$

Hence, $P = 2(\Delta V)^2 / R_P$ ……(4.4)

4.2.3 Estimation of Propagation Delay

Now we want to estimate the propagation delay from input to output. For this we need to apply KCL at the output node. Applying the rule at the output node of the JLFET we can get –

$C_L\, (dV_{out}/dt) + I_N = (V_{DD} - V_{out})/ R_{P1}$

i.e. $R_{P1}\, C_L\, (dV_{out}/dt) + I_N\, R_{P1} = V_{DD} - V_{out}$

i.e. $R_{P1}\, C_L \int_0^{\Delta V} (dV_{out} / (V_{DD} - V_{out} - I_N\, R_{P1})) = \int_0^T dt$

i.e. $- R_{P1}\, C_L ln|(V_{DD} - \Delta V - I_N\, R_{P1})/ (V_{DD} - I_N\, R_{P1})| = T$

i.e. $R_{P1}\, C_L ln|(V_{DD} - I_N\, R_{P1})/ (V_{DD} - \Delta V - I_N\, R_{P1})| = T$

Here, $R_{P1} = R_P/2$

So,

$$T = (R_P/2)\, C_L ln|(V_{DD} - I_N\, (R_P/2))/ (V_{DD} - \Delta V - I_N\, (R_P/2))| \quad \text{.....(4.5)}$$

4.2.4 Estimation of Power Delay Product

As static power dissipation and propagation delay are known, Power Delay Product(PDP) can be easily found out.

So, PDP = P*T

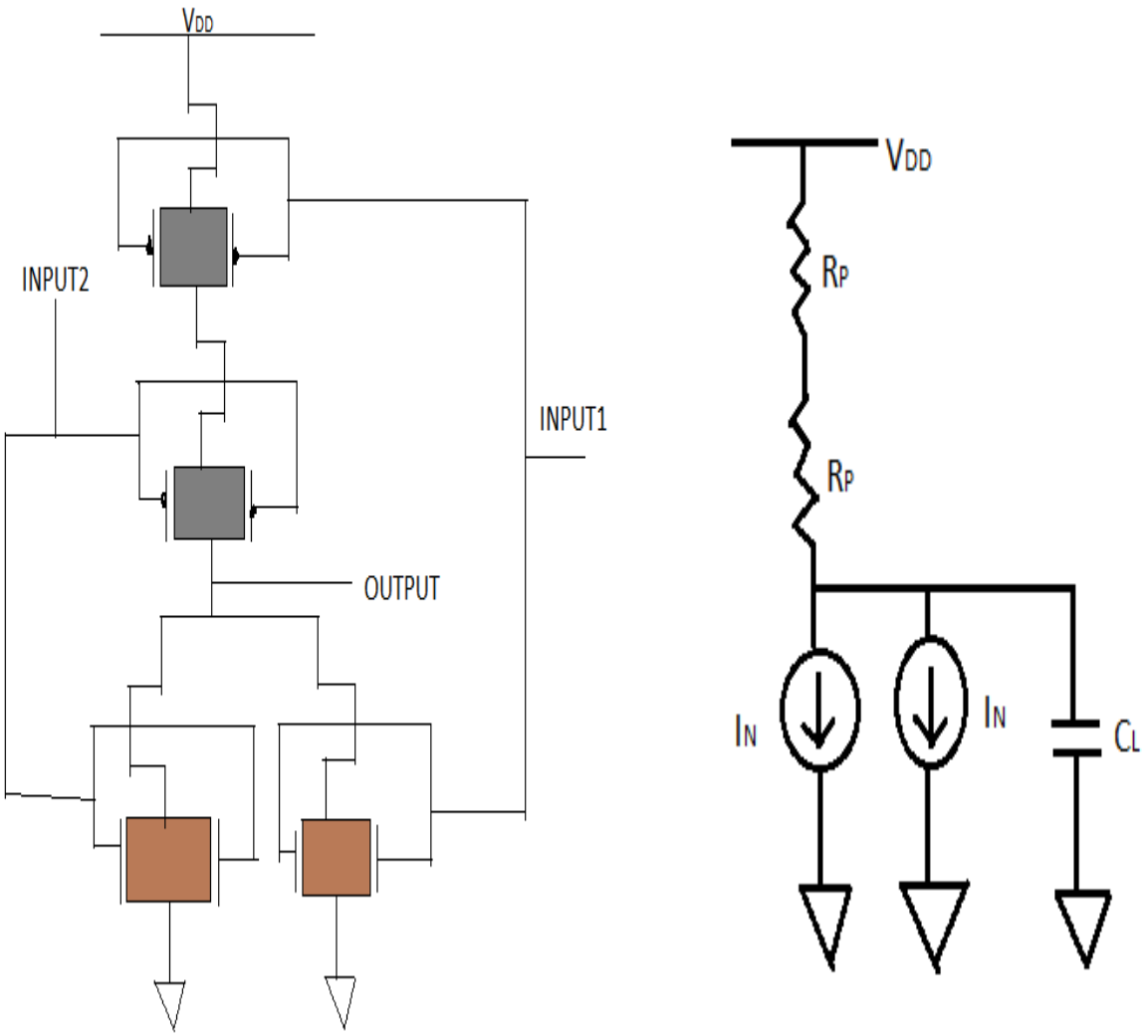
$$= (\Delta V)^2\, C_L ln|(V_{DD} - I_N\, (R_P/2))/ (V_{DD} - \Delta V - I_N\, (R_P/2))| \quad \text{.....(4.6)}$$

4.3 JLFET NOR Gate

The another universal gate NOR is realized using JLFET here.

4.3.1 Structure

The schematic diagram of JLFET NOR gate is presented in figure 4.5. It consists of two p-type JLFET connected in series and two n-type JLFET connected in parallel. For logic – 0 input n-type JLFET acts as a current source and p-type JLFET acts as a resistor. Here we shall discuss only subthreshold region of operation. The equivalent circuit is shown in fig. 4.6



a) b)

Fig 4.3 JLFET NOR Gate: a) Schematic Diagram, b)Equivalent Circuit Diagram

4.3.2 Estimation of Static Power Dissipation

The equation of drain current for n-type FET can be expressed as –

$I_{N2} = k_N (W/L)_N \exp((V_{GS} - V_{TH})/V_T)(1 – \exp(V_{DS}/V_T))$

Here $V_{TH} = V_{TH0} - \lambda_{DS}V_{DS} + \Delta V_{TH,Q}$

So,

$I_{N2}=k_N(W/L)_N\exp((V_{GS}-V_{TH0} +\lambda_{DS}V_{DS} -\Delta V_{TH,Q})/V_T)(1 – \exp(V_{DS}/V_T))$

$= \beta\exp(V_{GS}/V_T)(1 – \exp(V_{DS}/V_T))$

Here , $\beta = k_N (W/L)_N \exp((-V_{TH0} +\lambda_{DS}V_{DS} -\Delta V_{TH,Q})/V_T)$

$R_{P2} = |dV_{DS}/dI_{N2}|$

$I_{N2} = \beta\exp(V_{GS}/V_T)(1 – \exp(V_{DS}/V_T))$

$\approx \beta\exp(V_{GS}/V_T)(1 – 1 - (V_{DS}/V_T))$

$dI_{N2}/dV_{DS} = - (\beta/ V_T) \exp(V_{GS}/V_T)$

$R_{P2} = V_T/ \beta\exp(V_{GS}/V_T)$

Applying KCL we get as -

$C_L (dV_{out}/dt) + I_{N2} = (V_{DD} - V_{out})/ R_{P2}$

After rearranging we can get as –

$R_{P2} C_L (dV_{out}/dt) + I_{N2} R_{P1} = V_{DD} - V_{out}$

i.e. $R_{P2}\, C_L\, (dV_{out}/dt) = V_{DD} - V_{out} - I_{N2}\, R_{P2}$

i.e. $R_{P2} C_L \int_{\Delta V}^{V_{DD}-\Delta V} (dV_{out}/(V_{DD} - V_{out} - I_{N2} R_{P2})) = \int_0^T dt$

i.e. $-R_{P2} C_L \int_{\Delta V}^{V_{DD}-\Delta V} (d(V_{DD} - V_{out} - I_{N2} R_{P2})/(V_{DD} - V_{out} - I_{N2} R_{P2})) = \int_0^T dt$

i.e.$-R_{P2}\, C_L \ln|(V_{DD} - (V_{DD} - \Delta V) - I_{N2}\, R_{P2})/ (V_{DD} - \Delta V - I_{N2}\, R_{P2})| = T$

i.e. $V_{DD} - V_{DD} + \Delta V - I_{N2}\, R_{P2} = (V_{DD} - \Delta V - I_{N2}\, R_{P2}) exp(-T/R_{P2}C_L)$

i.e$\Delta V\,(1+exp(-T/R_{P2}C_L)=V_{DD} exp(-T/R_{P2}C_L)+I_{N2}R_{P2}(1-exp(T/R_{P2}C_L))$

As we know that,

$T >> R_{P2}C_L$, $exp(-T/R_{P2}C_L) \rightarrow 0$

So , $\Delta V = I_{N2}\, R_{P2}$

$P = (\Delta V)^2 / R_{P2}$……(4.7)

Here, $R_{P2} = 2R_P$ & $I_{N2} = 2\, I_N$

4.3.3 Estimation of Propagation Delay

Now we want to estimate the propagation delay from input to output. For this we need to apply KCL at the output node. Applying the formula at the output node of the JLFET we can get –

$C_L\, (dV_{out}/dt) + I_{N2} = (V_{DD} - V_{out})/ R_{P2}$

i.e. $R_{P2}\, C_L\, (dV_{out}/dt) + I_{N2}\, R_{P2} = V_{DD} - V_{out}$

i.e. $R_{P2}\, C_L \int_0^{\Delta V} (dV_{out} / (V_{DD} - V_{out} - I_{N2}\, R_{P2})) = \int_0^T dt$

i.e. $- R_{P2}\, C_L ln|(V_{DD} - \Delta V - I_{N2}\, R_{P2}) / (V_{DD} - I_{N2}\, R_{P2})| = T$

i.e. $T = R_{P2}\, C_L ln|(V_{DD} - I_{N2}\, R_{P2}) / (V_{DD} - \Delta V - I_{N2}\, R_{P2})|$

Here, $R_{P2} = 2R_P$ & $I_{N2} = 2I_N$

So,

$$T = 2R_P\, C_L ln|(V_{DD} - 4I_N R_P) / (V_{DD} - \Delta V - 4I_N R_P)| \quad \text{……..(4.8)}$$

4.3.4 Estimation of Power Delay Product

As static power dissipation and propagation delay are known, Power Delay Product(PDP) can be easily estimated.

So, PDP = P*T

$$= (\Delta V)^2\, C_L ln|(V_{DD} - 4I_N R_P) / (V_{DD} - \Delta V - 4I_N\, R_P)| \text{……(4.9)}$$

4.4 Performance Comparison of JLFET Inverter NAND Gate and NOR Gate

In this section static power dissipation, propagation delay and power-delay product will be compared among JLFET inverter, NAND gate and NOR gate by varying single parameter among

four parameters i.e. parasitic resistance(R_p),current source(I_N), load capacitance(C_L) and voltage source(V_{DD}) *at a time.*

4.4.1 Comparison of Power Dissipation in JLFET Inverter, NAND Gate and NOR Gate

Here power dissipation for JLFET inverter, NAND gate and NOR gate will be compared for variation of parasitic resistance(R_p), current source(I_N), load capacitance(C_L) and supply voltage(V_{DD}).

A. Variation of Power with Parasitic Resistance

Here C_L = 2 *pF*, I_N = 0.5 *mA*, V_{DD} = 20*V*. R_p is varied from 1 *k*Ω to 4 *k*Ω. With this variation the following variation is observed in power dissipation using equation (4.1), (4.4) and (4.7)-

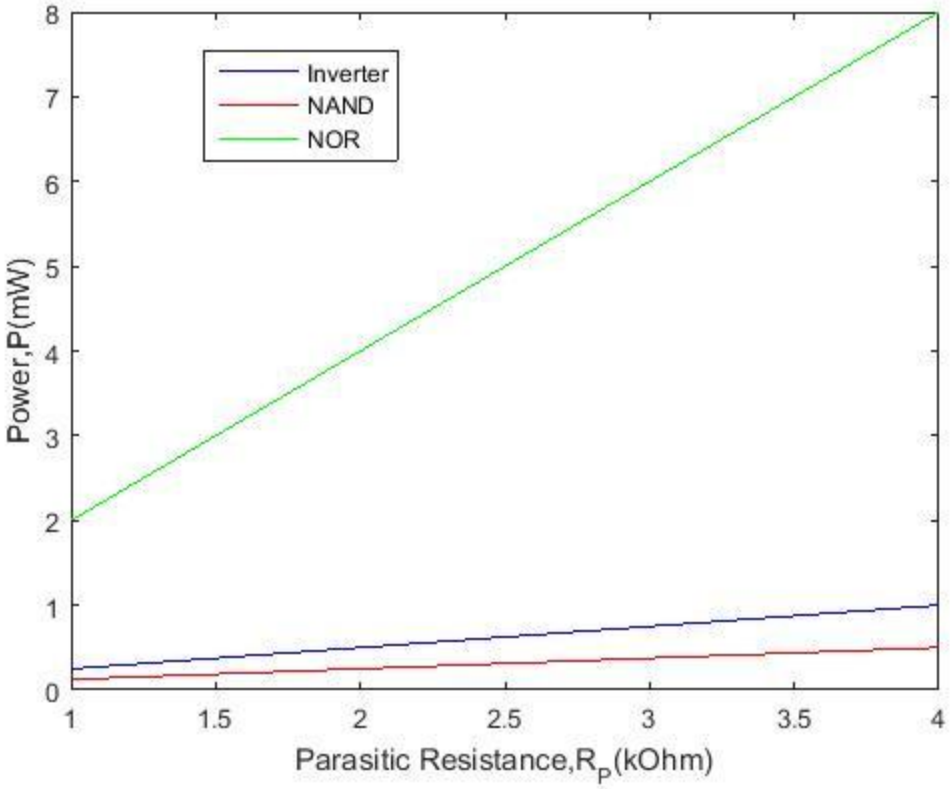


Fig 4.4 Variation of Power with Parasitic Resistance

B. Variation of Power with Current Source

Here $R_P = 1\ k\Omega$, $C_L = 2\ pF$, $V_{DD} = 20V$. I_N is varied from 0.5 mA to 1.5 mA. With this variation the following variation is observed in power dissipation using equation (4.1), (4.4) and (4.7) -

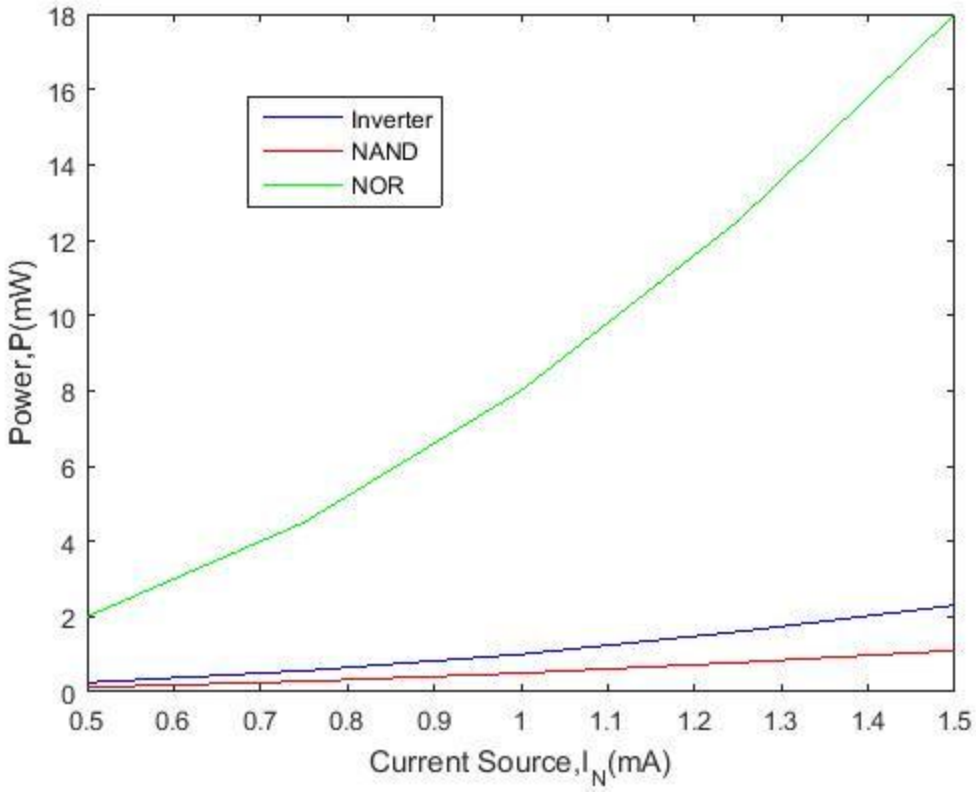


Fig 4.5 Variation of Power with Current Source

C. Variation of Power with Load Capacitance

Here $R_P = 1\ k\Omega$, $I_N = 0.5\ mA$, $V_{DD} = 20V$. C_L is varied from 2 pF to 6 pF. With this variation the following variation is observed in power dissipation using equation (4.1), (4.4) and (4.7)-

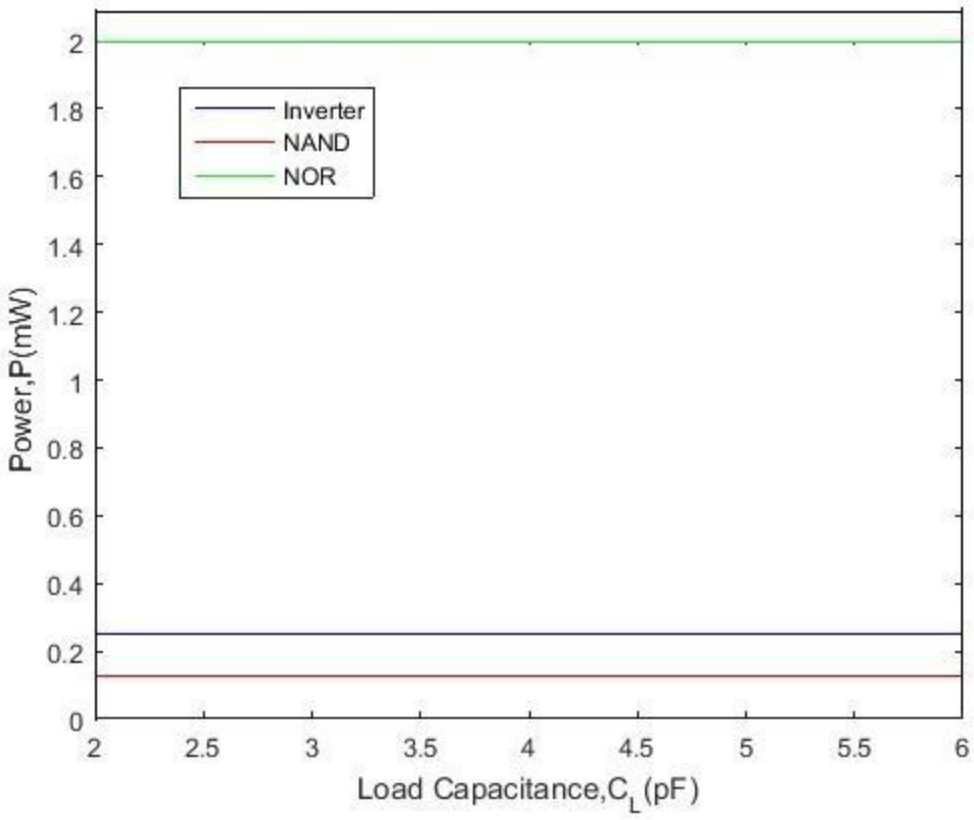


Fig 4.6 Variation of Power with Load Capacitance

D. Variation of Power with Voltage Source:

Here R_P = 1 $k\Omega$, I_N = 0.5 mA, C_L= 2 pF. V_{DD} is varied from 10 V to 20 V. With this variation the following variation is observed in power dissipation using equation (4.1), (4.4) and (4.7)-

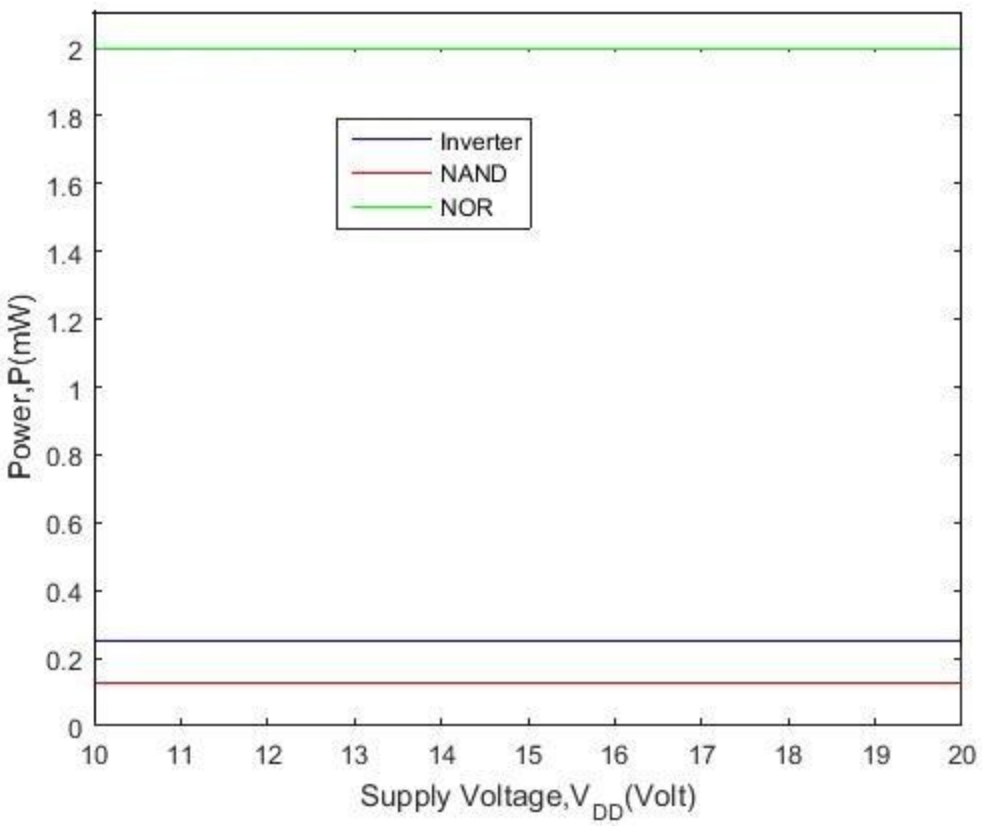


Fig 4.7 Variation of Power with Supply Voltage

4.4.2 Comparison of Propagation Delay in JLFET Inverter, NAND Gate and NOR Gate

Under this subsection propagation delay for JLFET inverter, NAND gate and NOR gate will be compared for variation of parasitic resistance(R_p), current source(I_N), load capacitance(C_L) and supply voltage(V_{DD}).

A. Variation of Propagation Delay with Parasitic Resistance:

Here C_L = 2 *pF*, I_N = 0.5 *mA*, V_{DD} = 20*V*. R_p is varied from 1 *k*Ω to 4 *k*Ω. With this variation the following variation is observed in propagation delay using equation (4.2), (4.5) and (4.8) -

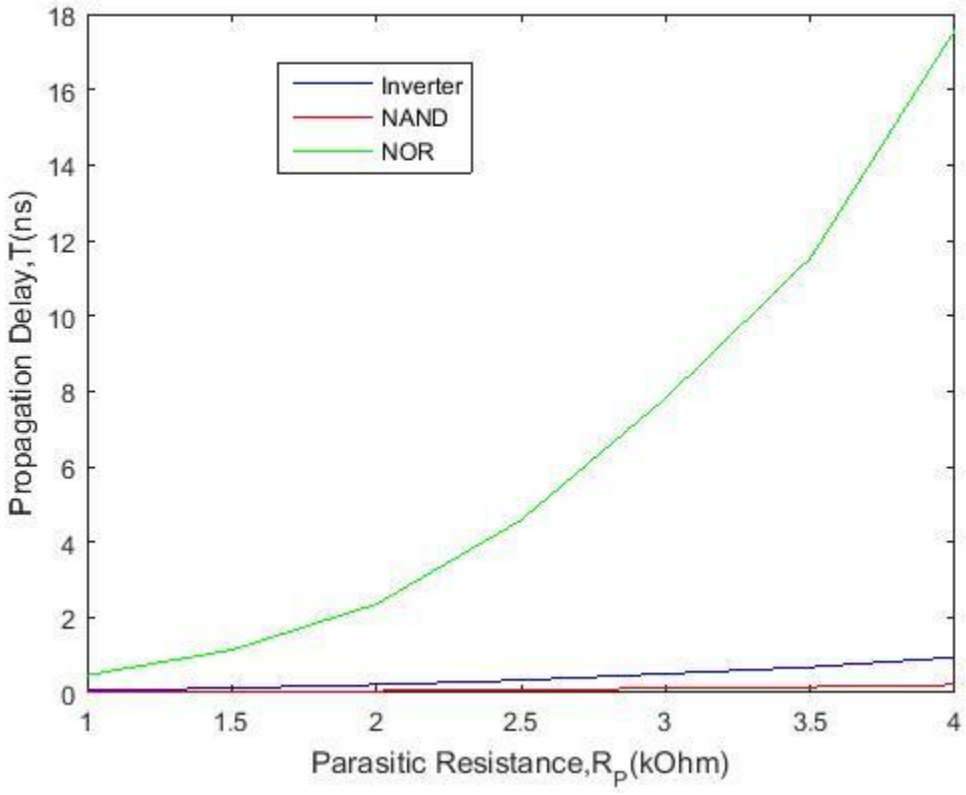


Fig 4.8 Variation of Propagation Delay with Parasitic Resistance

B. Variation of Propagation Delay with Current Source:

Here R_P = 1 *k*Ω, C_L = 2 *pF*, V_{DD} = 20*V*. I_N is varied from 0.5 *mA* to 1.5 *mA*. With this variation the following variation is observed in propagation delay using equation (4.2), (4.5) and (4.8) -

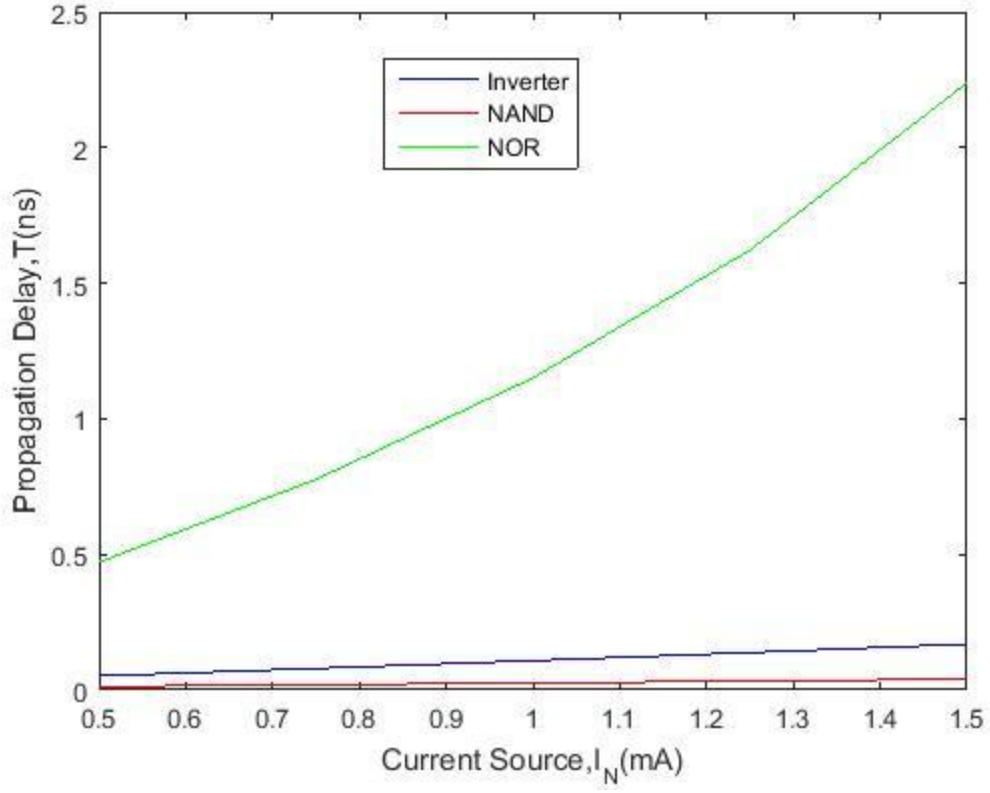


Fig 4.9 Variation of Propagation Delay with Current Source

C. Variation of Propagation Delay with Load Capacitance:

Here $R_P = 1\ k\Omega$, $I_N = 0.5\ mA$, $V_{DD} = 20V$. C_L is varied from 2 pF to 6 pF. With this variation the following variation is observed in propagation delay using equation (4.2), (4.5) and (4.8) -

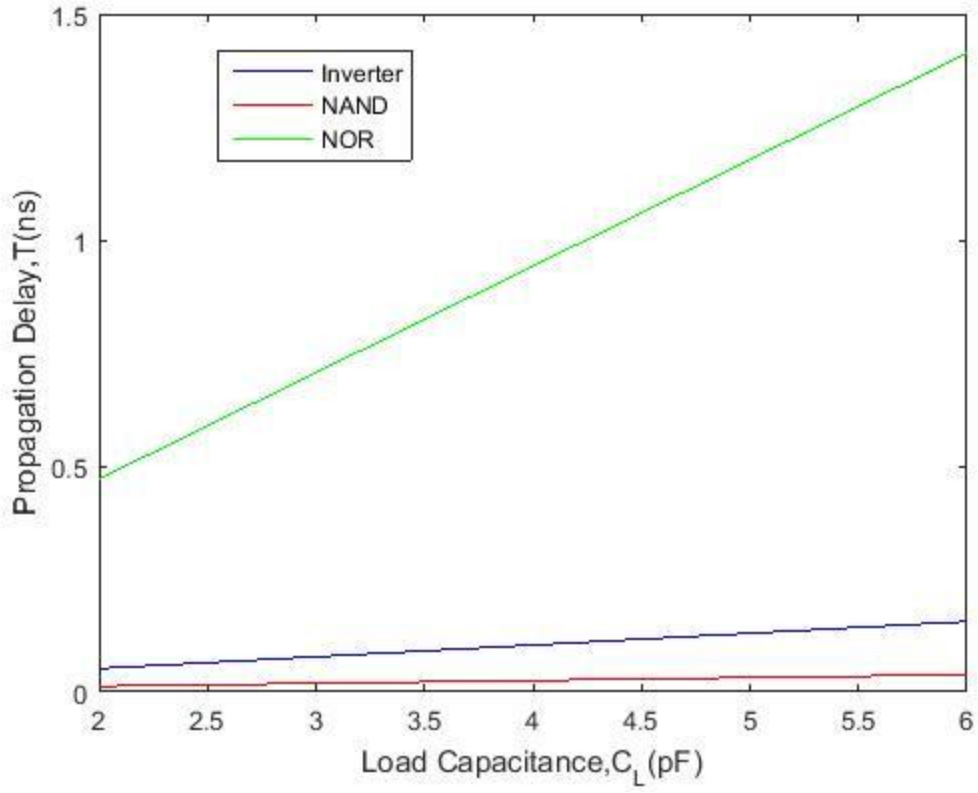


Fig 4.10 Variation of Propagation Delay with Load Capacitance

D. Variation of Propagation Delay with Supply Voltage:

Here $R_P = 1\ k\Omega$, $I_N = 0.5\ mA$, $C_L = 2\ pF$. V_{DD} is varied from 10 V to 20 V. With this variation the following variation is observed in propagation delay using equation (4.2), (4.5) and (4.8) -

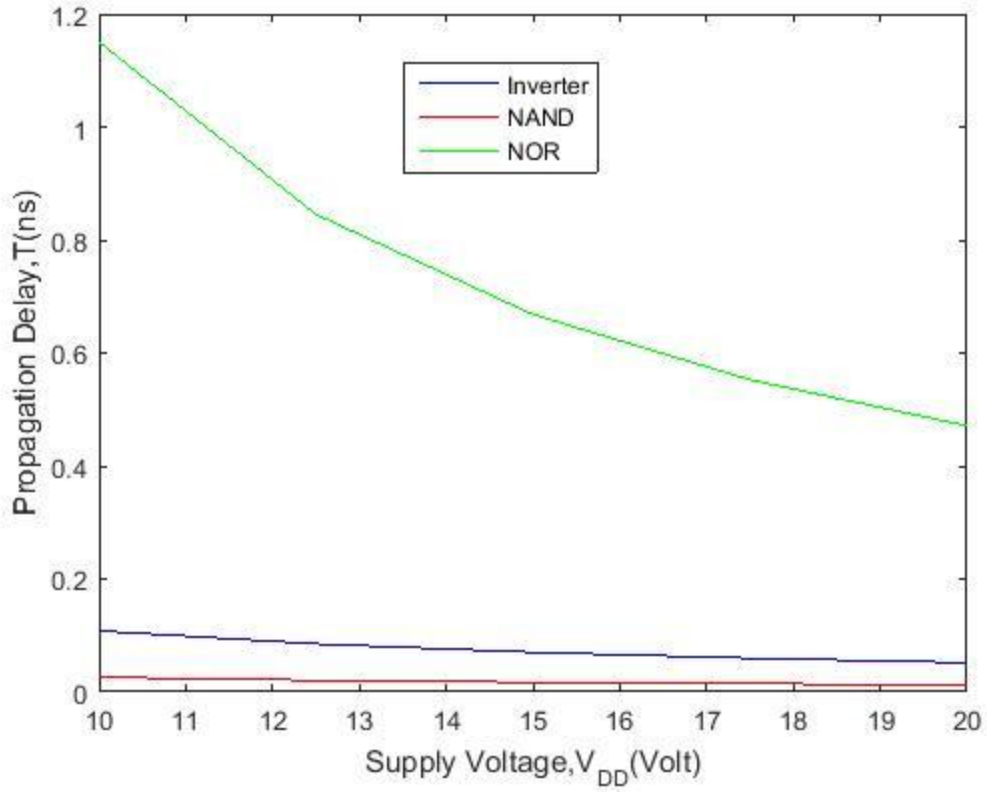


Fig 4.11 Variation of Propagation Delay with Supply Voltage

4.4.3 Comparison of Power Delay Product in JLFET Inverter, NAND Gate and NOR Gate:

In this subsection power delay product for JLFET inverter, NAND gate and NOR gate will be compared for variation of parasitic resistance(R_p), current source(I_N), load capacitance(C_L) and supply voltage(V_{DD}).

A. Variation of Power Delay Product with Parasitic Resistance:

Here C_L = 2 pF, I_N = 0.5 mA, V_{DD} = 20V. R_p is varied from 1 $k\Omega$ to 4 $k\Omega$. With this variation the following variation is observed in power delay product using equation (4.3), (4.6) and (4.9) -

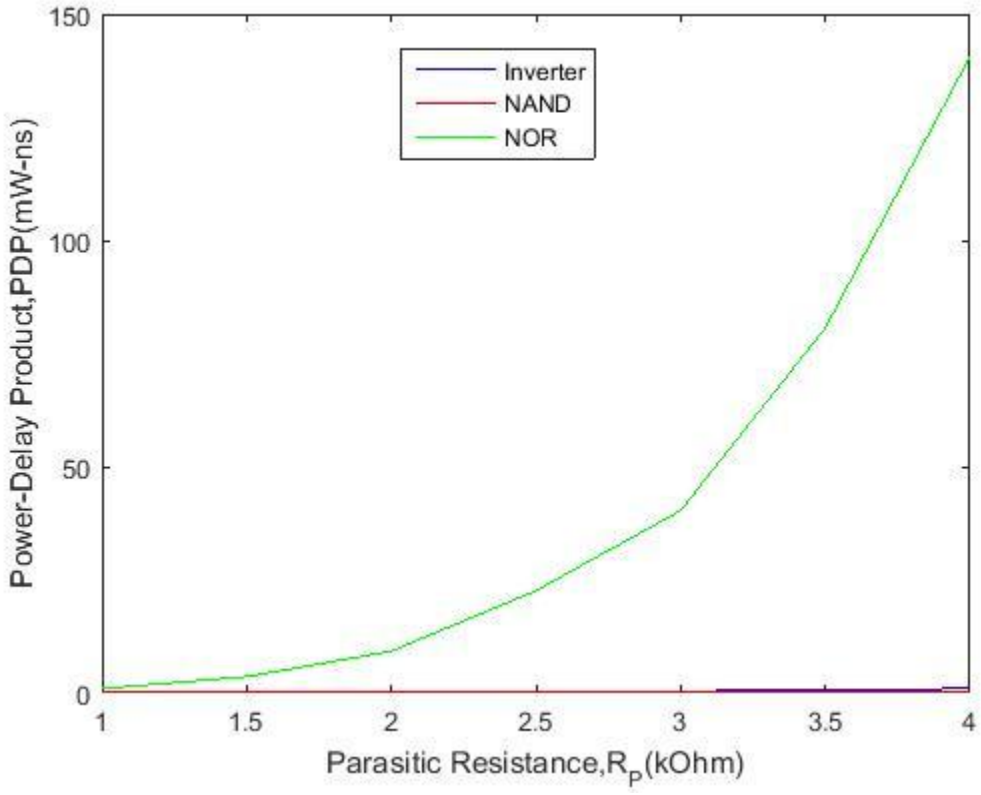


Fig 4.12 Variation of Power-Delay Product with Parasitic Resistance

B. Variation of Power Delay Product with Current Source:

Here R_P = 1 $k\Omega$, C_L = 2 pF, V_{DD} = 20V. I_N is varied from 0.5 mA to 1.5 mA. With this variation the following variation is observed in power delay product using equation (4.3), (4.6) and (4.9) -

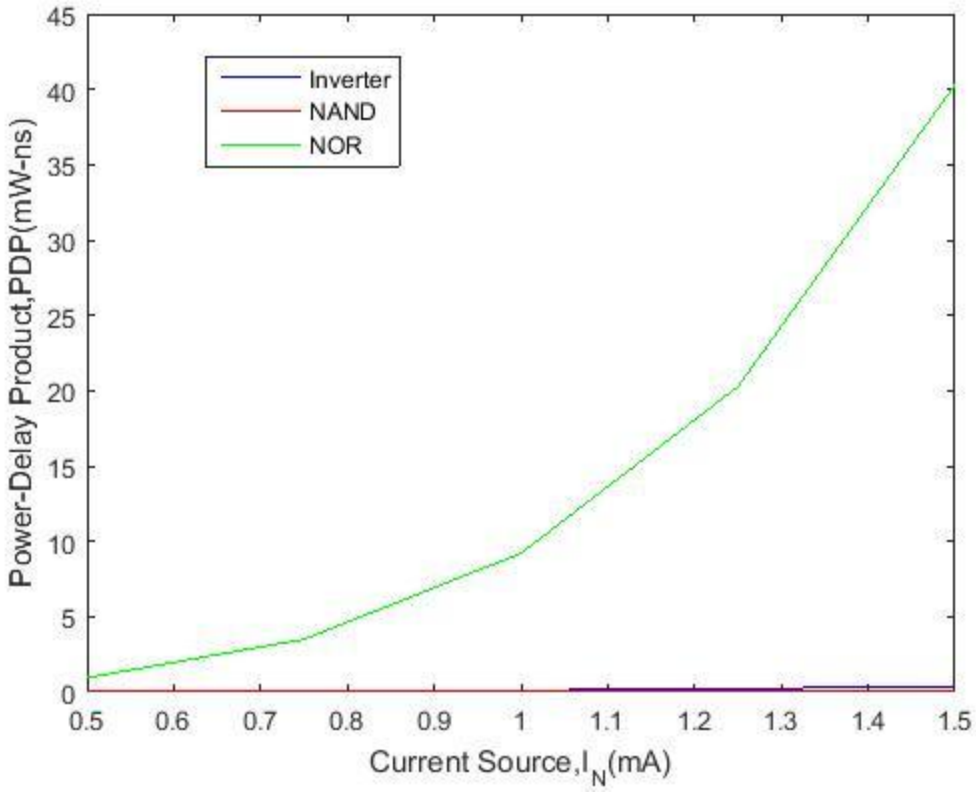


Fig 4.13 Variation of Power-Delay Product with Current Source

C. Variation of Power Delay Product with Load Capacitance:

Here $R_P = 1\ k\Omega$, $I_N = 0.5\ mA$, $V_{DD} = 20V$. C_L is varied from 2 pF to 6 pF. With this variation the following variation is observed in power delay product using equation (4.3), (4.6) and (4.9) -

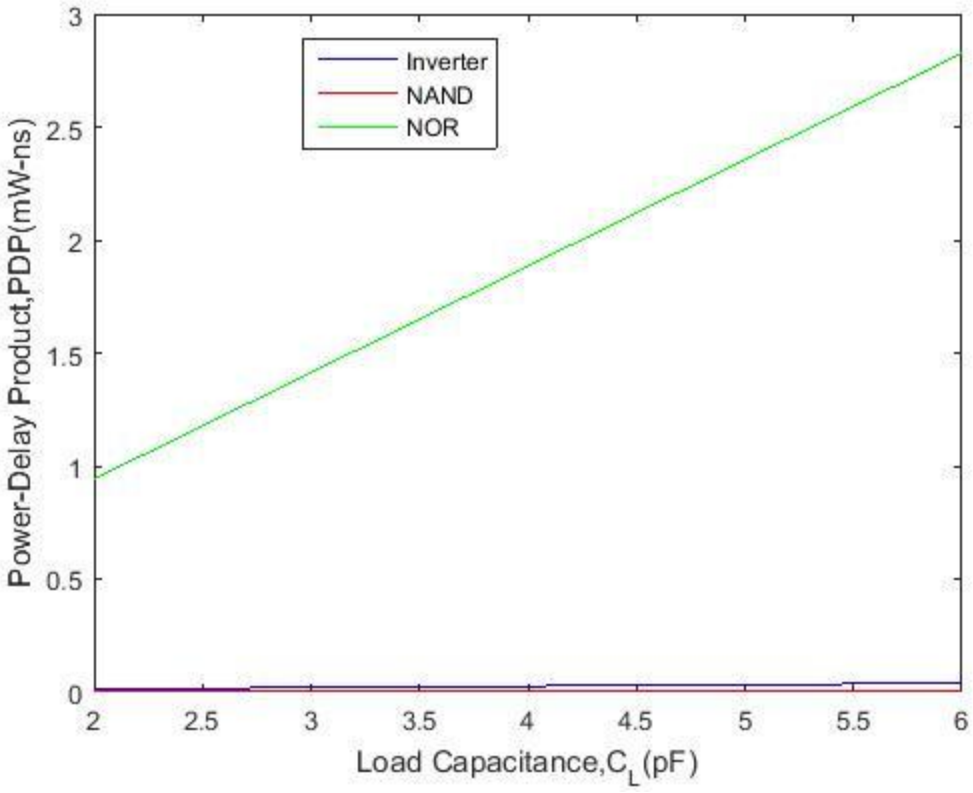


Fig 4.14 Variation of Power-Delay Product with Load Capacitance

D. Variation of Power Delay Product with Supply Voltage:

Here $R_P = 1\ k\Omega$, $I_N = 0.5\ mA$, $C_L = 2\ pF$. V_{DD} is varied from 10 V to 20 V. With this variation the following variation is observed in power delay product using equation (4.3), (4.6) and (4.9) -

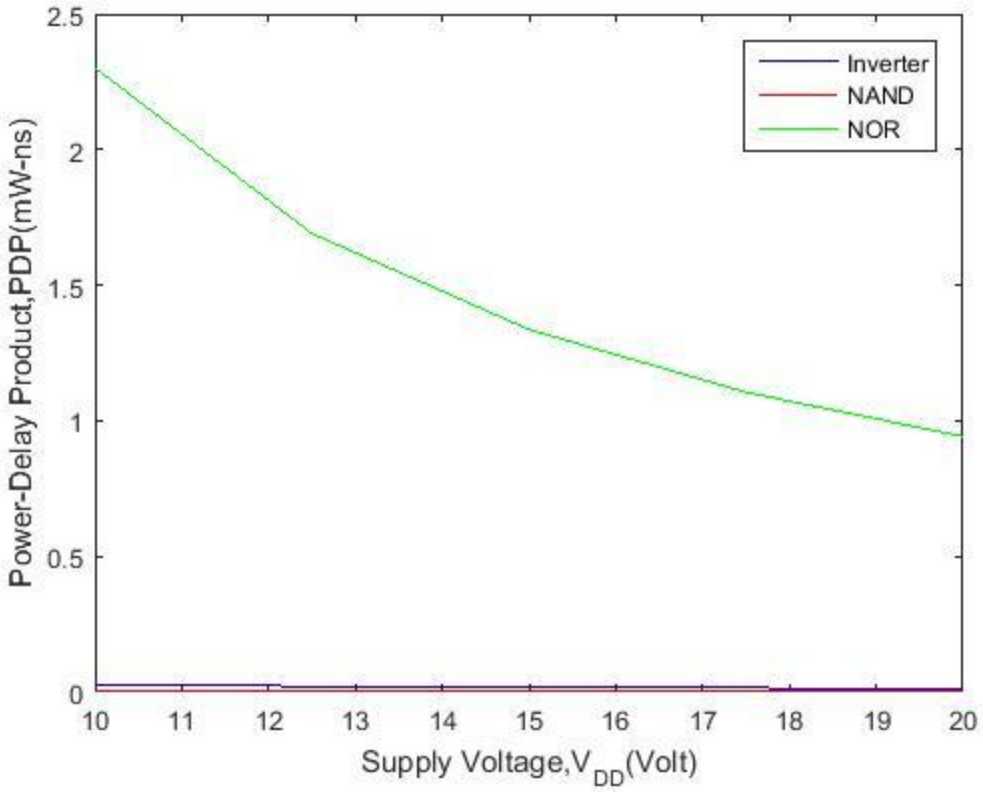


Fig 4.15 Variation of Power-Delay Product with Supply Voltage

We can observe that static power dissipation increases linearly with increase in parasitic resistance and increases in square proportion with current source. However the static power dissipation remains constant with increase in load capacitance and supply voltage.

Results indicate that the propagation delay increases non-linearly with increase in parasitic resistance and current source, but linearly with increase in load capacitance. Propagation delay however decreases with increase in supply voltage.

Power-delay product is the result of product of static power dissipation and propagation delay. The product increases with increase in parasitic resistance, current source and load capacitance while it reduces with supply voltage.

Chapter 5

Conclusion and Proposed Future Work

5.1 Summary of Results

It has been observed that quantum effect is more prominent with smaller channel thickness and higher channel doping. The decrement in total charge density increases with increase in dopant concentration for constant channel thickness. Also the decrement in total charge density increases with decrease in channel thickness for constant dopant concentration. Threshold Voltage Shift is larger for a JLFET with very thin channel and high channel doping. ON current is higher for higher channel thickness and higher channel doping and lower for lower channel thickness and lower channel doping. In a nutshell the observation can be summarized as below :

		Total Charge Density	**Threshold voltage Shift**	**ON Current**
Channel Thickness	Small	Low	High	Low
	Large	High	Low	High
Channel Doping	Small	High	Low	Low
	Large	Low	High	High

For inverter, NAND gate and NOR gate using JLFET it can be observed that static power dissipation, propagation delay and power-delay product are the highest in case of NOR gate and

lowest in case of NAND gate. So we prefer NAND design over NOR design whenever available. The overall picture is described as below-

	NAND	**NOR**	**Inverter**
Static Power Consumption	Low	High	Moderate
Propagation Delay	Low	High	Moderate
Power Delay Product	Low	High	Moderate

5.2 Future Scope of Work

In this dissertation, influence of quantum effect on the charge density, threshold voltage shift and ON-current has been investigated. Other parameters like, OFF-current, I_{OFF} and their ratio are also important parameters in determining the performance of a JLFET. So influence of quantum effect on the variations in I_{OFF} and I_{ON}/I_{OFF} are worth investigation. Also quantum effect can be investigated using different material like GaAs, InGaAs as carrier mobility is higher in those materials than in Si leading to faster operation. In addition some important analog circuits viz. current mirror, oscillator etc. can also be realized based on JLFET.

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SIMILARITY INDEX