Simulation based Design of Double Gate TFET Structure for better Analog performance by Gate Metal Work Function Modulation

This thesis is submitted for the partial fulfilment of the requirement for the Degree of **Masters of Engineering (M.E)** in the **Department of Electronics and Tele-Communication Engineering (ETCE)** under the Specialization of **Electron Devices**.

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UNDER THE GUIDANCE OF

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FACULTY OF ENGINEERING AND

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CERTIFICATE

This is to certify that the thesis entitled, **" Simulation based Design of Double Gate TFET Structure for better Analog performance by Gate Metal Work Function Modulation"** submitted by **Snehashis Biswas** (Roll No.: **002010702014**) of Jadavpur University, Kolkata is a record of legitimate research conducted under my supervision and guidance that may be accepted in partial completion of the requirements for the Master of Engineering in Electronics and Tele-communication Engineering with a specialisation in Electron Devices from the Institute. Any other paper submitted for the award of a degree to any other University or Institute does not include the research results reported in this thesis.

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List of Abbreviations

VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
TVRO	Threshold Voltage Roll Off
HCE	Hot Carrier Effect
SOI	Silicon On Insulator
FD SOI	Fully Depleted Silicon on Insulator
PD SOI	Partially Depleted Silicon on Insulator
BOX	Buried Oxide
SON	Silicon on Nothing
DG	Double Gate
TG	Tri gate
GAA	Gate All Around
DG TFET	Double Gate Tunnel Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunnel Field Effect Transistor

Abstract

In this thesis, we have proposed a Double gate tunnel field-effect transistor (DG-TFET) to enhance the Analog/RF performance. The proposed structure has been optimized through simulations. The DG-TFET shows both point and line tun-neling. 2-D Simulations are carried out in Silvaco TCAD ATLAS tool using nonlocal band to band tunneling models. The optimized DG-TFET provides a low threshold voltage of 0.36 Volt, a low subthreshold swing (SS) of 17.55 mV/decade and a high I_{ON} /$I_{OF\ F}$ of 2.5 x 10^{12}. Furthermore, the proposed device achieves a maximum transconductance, g_m of 1.75 x10^{-4} S/µm, an electric field, EF of 1x10^{7} V/m and a potential of 1.58 V. Here we shown, Design and Performance Investigation of Analog Performance of Double Gate TFET structure in this thesis.

Keywords: Band-to band tunneling (BTBT), inverter, line tunneling, sub-threshold swing (SS), transconductance, Tunnel Field Effect Transistor (TFET)

Chapter 1

Introduction

The vogue to follow the renowned Moore's Law has led to an enormous reduction in the dimensions of the transistors. This drastic reduction in transistor size, on the bright side, helped in packaging a huge amount of functionality in the ICs. However, on the pitfall, such scaling has surged the power dissipation and introduced various short channel effects (SCEs) in MOSFETs.

Tunnel Field Effect Transistors

The tunnel field-effect transistor (TFET) has proven to be one of the potential successors of MOSFET, due to the resemblance of their basic structures. Working of TFET is based on the band-to-band tunneling phenomenon, which is evidently different from that of MOSFET.

Basically a TFET is a reversed-biased p-i-n diode with gate modulation of tunneling probability. A typical TFET structure with band diagram is as shown in Figure. at off state, the potential barrier between channel and the source is so wide that no tunneling occurs. In the on-state, gate voltage modulate the potential barrier and makes it narrow to allow a significant tunneling current. Theoretical analysis showed that the SS value of TFET can be reduced to below 60mV/dec. More recently several groups have shown experimental results and confirmed that in a certain bias range the SS can be reduced below 60mV/dec.

Making the gated tunnelling process more effective while successfully suppressing numerous leakage paths is the main challenge with TFET. The bandgap energy, reduced effective mass, and electrical field within the tunnel barrier are three variables in the exponential term that have a significant impact on the likelihood of tunnelling, as shown in equation. Low tunnel barrier height is preferred by an efficient tunnelling process, which is dictated by the bandgap energy, and In an abrupt pn junction, a short tunnel width typically translates to a large electrical field. The decreased effective mass is mostly reliant on the material and highly sensitive to bandstructure alteration caused by quantum confinement, strain effect, etc.

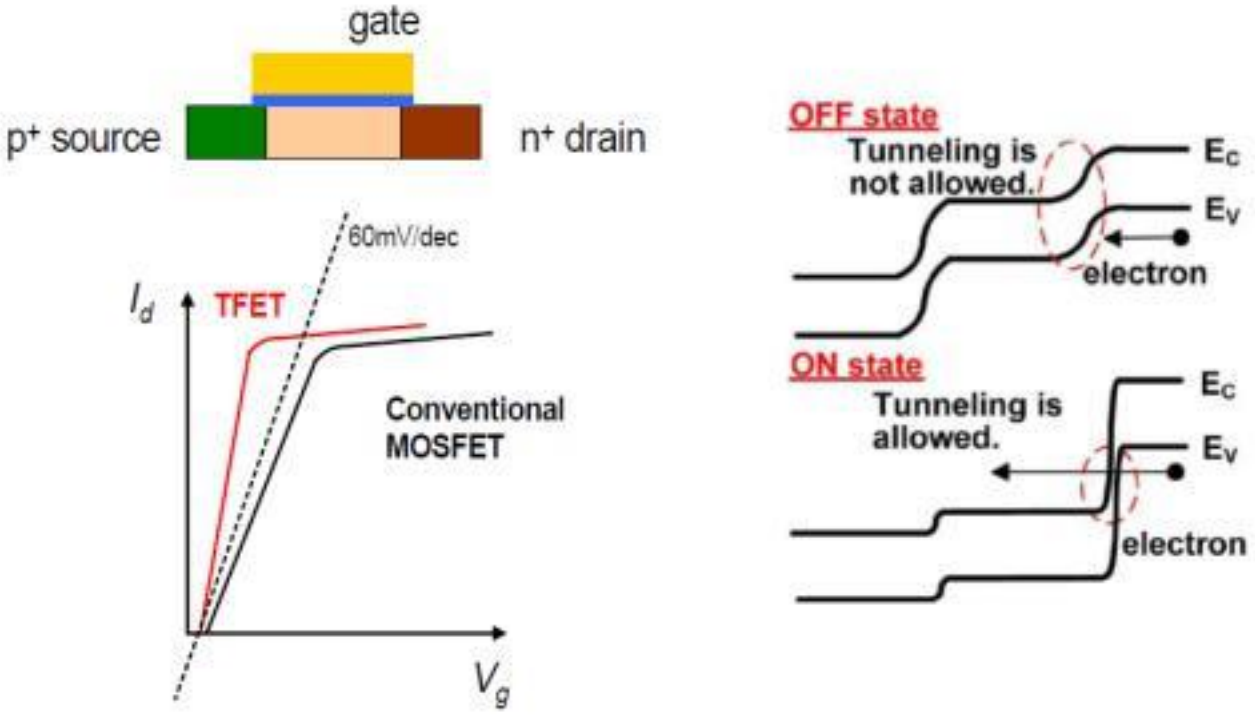


Figure : Device structure and band diagram in the ON/OFF states of the n-channel TFET, desired Id~Vg curve of TFET is shown.

Use of tiny bandgap material is the simplest technique to improve TFET performance. Devices employing silicon germanium alloy or pure germanium as the source material have clearly reduced SS and increased driving current. It is essential to build an abrupt junction in order to strengthen the electrical field.

Unfortunately, there hasn't been much success so far in creating acute junctions in FET structures. Ion implantation dopant atoms' high energy tail is difficult to remove, and the high temperature annealing process that follows to repair implantation damage can quickly result in a widened doping profile that prevents the creation of abrupt junctions. Additionally, source to drain junction leakage current affects a TFET's SS and off-state current negatively. There are numerous techniques to prevent leakage current between the source and drain, such as using a thin channel body (10nm), a gate-all-around construction (nanowire), and a high K dielectric to maximise gate to channel coupling.

Due to the similarities in their fundamental architectures, the tunnel field-effect transistor (TFET) has emerged as one of the viable alternatives to MOSFET. The band-to-band tunnelling process underlies TFET operation, which is clearly distinct from MOSFET operation.

TFETs are a fantastic choice for low-power applications like memory devices since they can produce subthreshold swings (SS) lower than 60 mV/decade. Additionally, TFETs only rely on the band overlapping required for band-to-band tunnelling because MOSFETs have the thermionic emission threshold for channel construction. High ION/IOF F can be achieved with TFETs. TFETs can dissipate relatively little dynamic power since they have low supply voltage requirements and low threshold voltages.

To improve TFET performance, many researchers tried to structure engineer them. To enhance the ION, some researchers have experimented with lower bandgap materials. However, this could cause the IOF F current to increase significantly, which would result in more static power dissipation. Other research attempted to model TFETs to boost ION while maintaining a low IOF F, but at the same time the complexity of the process rose. The ON current was increased by a few researchers that attempted to engineer the channel from conventional to L-channel to U-channel by enabling both line and point tunnelling to enter the picture.

TCAD simulations of TFETs, like the one in this thesis, are significant in a number of ways. In order to better understand the device physics and the tunnelling likelihood inside the device, we have presented the Electric eld vector distributions. Using 1D or 2D cross-sections, it aids in our ability to look through the apparatus. We have taken steps toward optimising the device settings at various drain heights through simulations.

In this thesis, we present a simulation-based, definitive TFET structure engineering that will aid in the creation of future models and a deeper comprehension of the device.

The central issue with TFET is to make the gated tunneling process more efficient with various leakage path successfully suppressed. As seen in equation, tunneling probability is highly sensitive to three variables in the exponential term: bandgap energy, reduced effective mass and the electrical field within tunnel barrier. Efficient tunnel process favors low tunnel barrier height, which is determined by the bandgap energy,short tunnel width, which normally translates to high electrical field within an abrupt pn junction. The reduced effective mass is mainly material dependent and very sensitive to bandstructure modification by quantum confinement, strain effect, etc.

The most straightforward way to boost the TFET performance is to adopt small bandgap material. Devices with replacement of the source material by silicon germanium alloy or pure gemanium have shown obvious reduction of SS and increase of the drive current. To increase the electrical field strength it is critical to fabricate abrupt junction.

Unfortunately so far little success has been made in producing sharp junction in a FET structure. It is hard to eliminate the high energy tail of ion implantation dopant atoms, and subsequent high temperature annealing process to repair implantation damage can easily result in broadened doping profile preventing formation of abrupt junction. Furthermore, source to drain junction leakage current has negative effect on off-state current and SS of a TFET. Suppression of leakage current between source and drain can be done in many ways, for example, thin channel body (<10nm), gate-all-around structure (nanowire), in combination with high K dielectric to increase gate to channel coupling.

Motivation

TFETs can achieve subthreshold swings (SS) lower than 60 mV/decade, which enables TFET to be a great candidate for low-power applications like memory devices. Also, TFETs does not possess the thermionic emission threshold present in MOSFETs for its channel formation and solely rely on the band overlapping which is necessary for the band-to-band tunneling. With TFETs, very high I_{ON} /$I_{OF\ F}$ is achieve-able. Having low threshold voltages and low supply voltage requirements, TFETs are able to dissipate very low dynamic power.

The major pitfalls of TFETs are its low ON current and its am-bipolar current nature, which we have tried to improve through structural engineering.

Current Scenario

Many researchers tried to structure engineer TFETs for better performance . Some of the researchers have tried using lower bandgap materials to improve the I_{ON} . However, with this the I_{OFF} current could rise significantly thereby leading to higher static power dissipation. Other studies tried to model TFETs to improve I_{ON} by keeping I_{OFF} low but the process complexity increased simultaneously. Few of the researchers tried to engineer the channel from conventional to L-channel to U-channel allowing both line and point tunneling to come into the picture thereby increasing the ON current.

1.4 Objective

TCAD simulations of TFETs such as the one presented in this thesis are important in various ways. We have presented the Electric eld vector distributions which help up better understand the device physics along with the tunneling probability inside the device. It helps us to see through the device using 1D or 2D cross-sections.

Through simulations we have approached towards the optimization of the device parameters for various drain height. In this thesis, we have given a simulation based conclusive TFET structure engineering that will help in the future model development and understanding the device better.

Thesis Organization

This Thesis is oriented as follows :

Chapter 1: Gives an overview of the basic topics related to this thesis and explanation of certain keywords mentioned in the abstract.

Chapter 2: Provides an extensive overview of the small geometry devices and their journey of evolution beginning from long channel MOSFETs to recent short channel devices. Several consequences arising due to such device dimension miniaturization.

Chapter 3: This chapter is about Basics of TFET,MOSFETs vs TFETs,Working principle of TFET,Working Principle of MOSFETs vs TFET, Tunneling Mechanism, Line tunneling and Point tunnelling etc.

Chapter 4: The method of simulation used in this project is explained in this particular chapter. As Silvaco Atlas TCAD has been used for simulations, most of its syntax has been discussed

Chapter 5: Describes the structure of the proposed TFET and its operation. It includes the device physics part to explain the working of TFETs with the band to band tunneling phenomenon between the source and channel. Also, the two types of tunneling mechanisms are illustrated in the proposed structure. It also includes I-V, C-V characteristics, energy band diagrams, electric field plots etc

Chapter 6: Describes the discussion of the Analog parameter characteristics for the proposed structure characteristics along with g_m, f_T and Gain bandwidth product for the proposed structure.

Chapter 7: Provides a summary of the work done and the future scope for newer research areas for this proposed structure.

Chapter 2

Literature Review

The last few decades have witnessed a phenomenal growth in the microelectronics industry being obsessed by the continuous shrinking of device dimension to increase the device integration density with subsequent reduction in manufacturing cost. The future of VLSI as predicted by Moore since 1965 with proportional device downscaling also portrays its progress through high operating speed VLSI circuits and minimum power consumption. However, aggressive downscaling of conventional MOS technology suffers the limitations of complex fabrication techniques and the associated cost. Moreover, ultra nano-scaled device physics also require lucid concept of quantum mechanical laws. Such small scaled devices when integrated on a single chip may loss its functional competency and degrade the overall circuit operation. These challenges are driving the researcher community to investigate non-conventional MOS structures that can circumvent the scaling limitations and allow further miniaturization without compromising the device performance. While some of these devices employ the principle of quantum mechanical phenomena and are referred as revolutionary nano-electronic devices (quantum well, quantum wire, quantum dot based devices e.g. HEMT, Spintronics, SET, etc.), the other group of scaled devices with geometrical modifications and improvisation in material properties in existing technology fall under the category of evolutionary nano-devices (e.g. Carbon Nanotube FETs, heterojunction based FETs, Nanowire FETs, Ge channel devices, strained channel FETs, structurally refined FETs, etc.). Incessant research exploration in pursuit of such non-conventional devices can satisfy Moore's scaling trend and realize superior functionality by suppressing inevitable short channel effects in terms of drain induced barrier lowering, threshold voltage roll off, hot carrier effect, to mention a few [72]. The architecture, operating principles, analytical modeling approaches of such devices are quite different from conventional ones and have been focused in the present thesis highlighting the available options of further scaling and proper device optimization.

Overview on Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has earned commendable popularity since 1970s owing to its simple architecture, reduced fabrication cost, minimized power consumption, inherent high input impedance, momentous speed of operation and improved noise immunity. Superior scalability of MOSFET device for incremented transistor count/chip as predicted by Moore's law has marked the evolution of semiconductor industry from the era of sub-micron to present sub-nano regime. The fundamental principle of MOSFET was proposed by Julius Edgar Lilienfeld in the year 1925 which performs the basic operations of amplification and switching of electronic signals. The name MOSFET itself gives a clue to the MOS capacitor based working principle of the device with the dielectric layer of silicon dioxide (SiO2) being sandwiched between the metal gate electrode and bulk silicon substrate that act as terminals/plates of capacitor. The schematic of basic MOSFET structure is illustrated in figure 2.2.1. It consists of four terminals depicted as heavily doped source and drain, metal gate and lightly doped silicon body. Depending upon the type of dopants of source and drain regions that determine the type of channel formed, MOSFET can be categorized as p-channel and

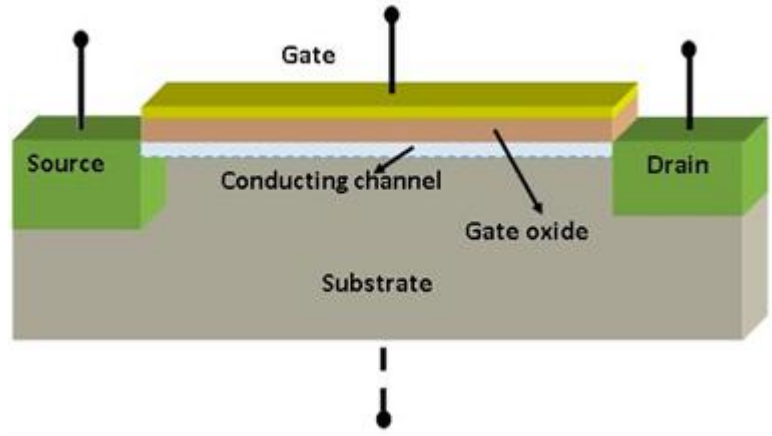


Figure. - Basic MOSFET structure.

n-channel variants. p-type substrate and heavily doped source/drain with

n+ impurities realize n-channel MOSFET where electrons act as majority carriers in the induced channel. Similarly, for p-type MOSFET, holes act as the majority carriers within the induced p-channel where n-type substrate and p+ source/drain form the basic structure. The conducting channel is actually a layer of inversion charge formed at the interface of oxide-semiconductor and bears the flow of carriers from the source towards the drain region on application of suitable drain bias. An n-channel MOSFET with heavily doped n+ source and drain regions being diffused or ion-implanted into the lightly doped silicon substrate is presented in figure. A dielectric layer of silicon dioxide is grown over the silicon body between the source and drain regions followed by metal gate deposition to dielectrically insulate the gate electrode from the device. This isolation ensures high input impedance of MOSFET in order of Mega ohms or approximately infinite preventing flow of carriers from the gate to the device itself. MOSFET is also termed as the gate controlled resistor where the induced channel and its conductivity depend upon the gate potential and its variation respectively. The device is symmetrical with respect to source and drain which being doped with same dopants can be interchanged easily depending upon the direction of current flow within the device as per the external applied bias. However, the high input impedance of the device induces considerable static charges that may hamper the functionality of MOSFET unless taken care of or handled cautiously.

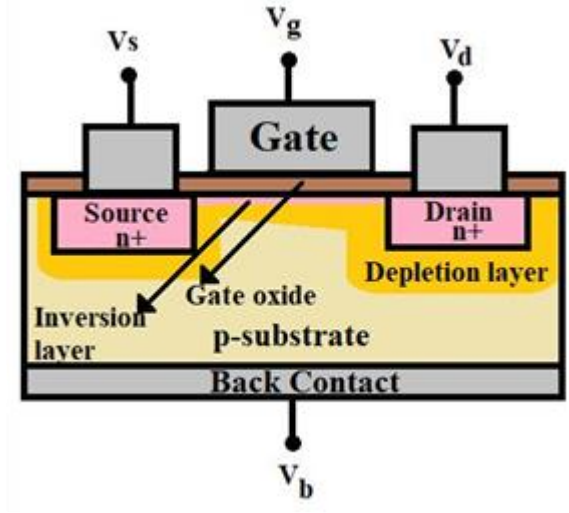


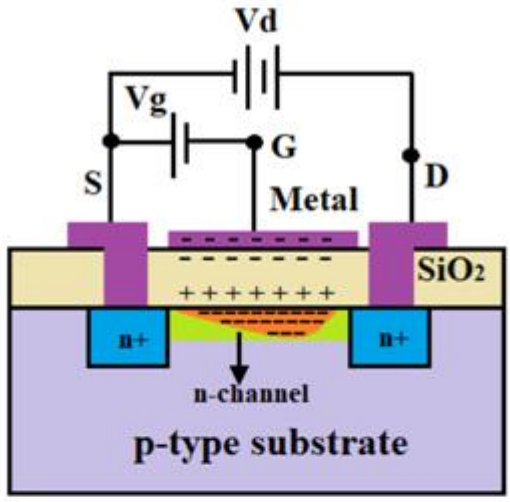
Figure. - Schematic representation of n-channel MOSFET.

Types of MOSFET

Depending upon the process of channel formation in MOSFET, it can operate either in Depletion mode or Enhancement mode.

Depletion mode MOSFET

The existence of preformed channel between the source and drain regions under zero bias condition of depletion mode MOSFET distinguishes it from broadly used enhancement mode equivalent. It acts as 'normally switched on' device and a suitable gate voltage is required to switch the device to OFF state condition. Unlike enhancement type MOSFET, the channel of depletion mode MOSFET is diffused with same type of dopants used for source/drain diffusion regions. Considering n-channel depletion type MOSFET, application of negative gate voltage makes the channel depleted of charge carriers thus reducing the drain current while positive gate voltage increases the number of charge carriers that contribute to incremented drain current of the device. The schematic diagram and current voltage characteristics of n-channel depletion mode MOSFET are represented in the below figure.



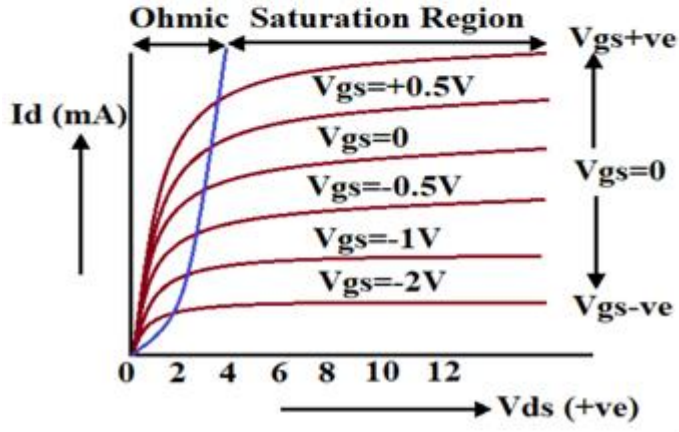


Figure - Representation of n-channel depletion mode MOSFET and its current-voltage characteristics.

The opposite behavior is exhibited by p-channel depletion mode MOSFET. This type of device bears close resemblance to JFET with low resistance channel extending between source and drain and pre-doped with electrons and holes for n-channel and p-channel device respectively. However, the conductivity of depletion type MOSFET is much less relative to enhancement mode counterpart. It can be operated as enhancement mode MOSFET also although vice versa is not applicable.

Enhancement mode MOSFET

The distinct feature of Enhancement mode MOSFET is its undoped or very lightly doped channel region that remains non-conductive under zero bias gate condition. For n-channel enhancement type MOSFET as depicted in figure 2.2.4 (a), applying positive gate voltage generates a vertical electric field from the gate towards the channel that attracts the minority electrons of the p-type substrate at the semiconductor/oxide interface and pushes the holes within the body. This increases the thickness of the channel and reduces its resistivity to enhance the drain current conduction. The voltage at which the channel is fully inverted is referred as the threshold voltage Vth while subthreshold condition exists for range of voltage before inversion condition is achieved as presented

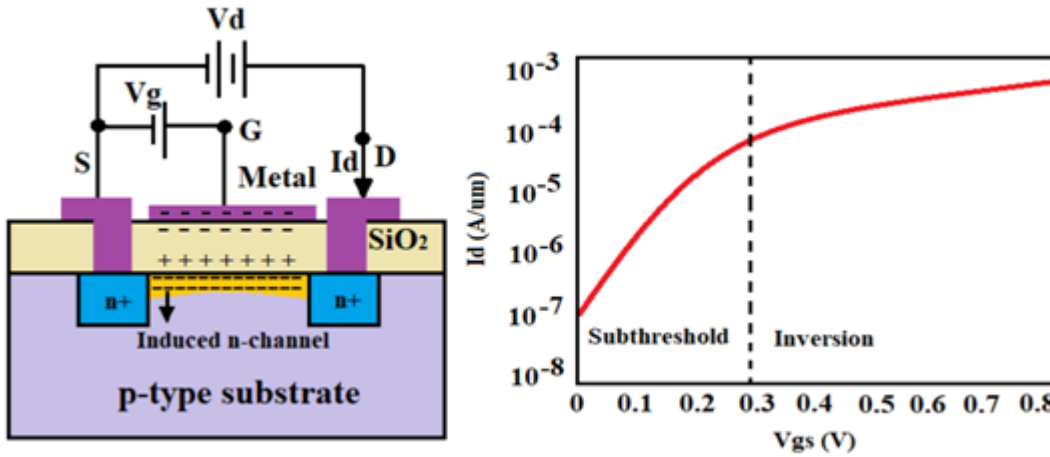


Figure. - Representation of (a) basic n-channel Enhancement mode MOSFET structure and (b) its Id-Vgs characteristics

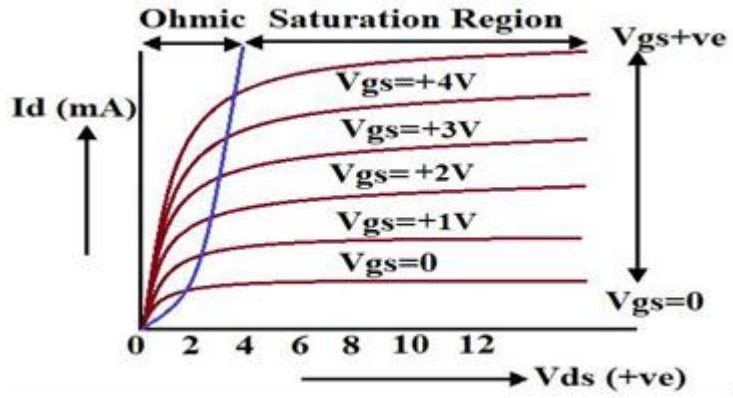


Figure- Representation of (c) Current-Voltage characteristics of n-channel Enhancement mode MOSFET.

Figure. - (b). As the gate bias crosses the threshold voltage, electron rich n-type channel under inversion condition prevails facilitating a continuous flow of device current from drain to source once a suitable positive drain bias is applied.

Thus, it can be inferred that for n-channel enhancement MOSFET as positive gate voltage increases, the channel resistivity is lowered resulting effective enhancement in channel current thereby justifying the name Enhancement mode MOSFET. The device acts as 'Normally open' switch with zero/negative gate voltage while it turns 'ON' under positive gate bias condition. The low resistivity of the device in 'ON' state condition and high 'OFF' state resistance with extremely high gate resistance also make it suitable for applications in power switching circuits and as CMOS logic gates. The Id versus Vds characteristics of n-channel enhancement mode MOSFET is shown in figure. (c).

Operational regions of MOSFET

The principle operation of MOSFET can be explained by the theory of MOS capacitor. Considering n-channel Enhancement MOSFET, a positive gate voltage will induce positive charges being accumulated at gate surface acting as one plate while corresponding negative charges are induced in the opposite plate of p-type substrate at oxide/semiconductor interface. The negative charges are due to the minority carriers (electrons) and are dependent on the gate bias. Hence, with increase in gate voltage, more number of minority carriers are attracted thereby decreasing the hole density below the gate region.

The condition of ‘channel inversion’ is achieved on further increase in gate bias where presence of large number of free electron carriers decreases the effective channel resistance and contribute to device current with appropriate drain bias. The MOSFET operational regions depending upon the applied gate voltage are enlisted below and also illustrated in figure.

a. **Cut-off region**: When the applied gate to source voltage (Vgs) is less than the specified device threshold value, MOSFET exhibits no current conduction and acts as ‘open circuit’. This region is referred as cut off region of MOSFET and the same is depicted in figure.

b. **Linear or ohmic region:** When the applied gate bias (Vgs) is greater than the threshold value provided the drain to source voltage (Vds) is more than Vgs, the drain current increases linearly with Vds through the

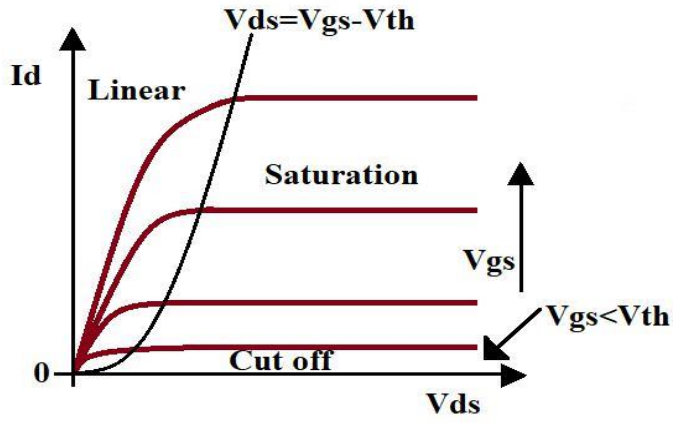


Figure. - Illustration of different regions of operation in drain current characteristics of MOSFET.

Device and it acts like voltage controlled resistor whose value in turn is dependent on Vgs. This mode of operation is linear or ohmic region and is utilized for MOSFET signal amplification.

Saturation region: Keeping the gate to source voltage well above the threshold value, as the drain bias reaches the saturation voltage, i.e. Vds=Vgs-Vth, the drain current reaches its maximum value acquiring constant current region. The transistor under this region switches to 'fully ON' state and acts as closed circuit. This region is referred to as saturation region finding application in digital switching circuits.

Analytical model description of MOSFET

As already described in the principle of MOSFET conduction mechanism is based on the condition of channel inversion induced by applying suitable bias on the gate electrode of the device. It generates a vertical electric field underneath the gate terminal and modulates the flow of carriers from the source to drain through the conducting channel. Here, proper gate bias (Vgs) refers to the gate to source voltage at which the semiconductor channel is inverted to maintain the subsequent conduction and is termed as the threshold voltage (Vth). When applied Vgs is not sufficient to achieve the inversion region, i.e. Vgs < Vth, the absence of conducting channel prevents the current flow through the device until the gate bias exceeds Vth. Once the applied Vgs is chosen to be higher than the device threshold value, a large number of minority carriers (electrons in case of n-channel MOSFET) get attracted owing to the induced

vertical field towards the interface of oxide/semiconductor and an inverted channel is formed supporting an effective device current flow.

The four physical components of threshold voltage of MOSFET as identified for almost all practical purposes comprises of :

i) The workfunction difference ($_{gc}$) between the gate electrode and semiconductor channel

Depending on the material of the gate terminal, the workfunction difference is given by:

$$gc_{f} \quad (substrate)_{m} (metal \quad gate) \ldots\ldots\ldots \qquad (1)$$

$$gc_{f} \quad (substrate)_{f} (polysilicon \quad gate) \ldots\ldots\ldots \qquad (2)$$

ii) The gate terminal voltage component required to adjust the surface potential ($_f$)

$_f$ presents the component of externally gate voltage required to achieve surface inversion by altering the surface potential by $2\ _f$.

Advantages of MOSFET and its suitable applications

Incessant research in the domain of semiconductor industries have already brought several ground breaking techniques for feasible fabrication of scaled MOSFET devices with drastically improved performance. The extreme low power consumption, momentous speed of operation, small area requirement of MOSFETs with higher integration density and low cost make it a potential choice for complex high performance IC designs. MOSFET acts as suitable electronic switch or common-source amplifier for its low power consumption and as ideal buffer amplifier for its high input impedance. Its ability to capture weak signal for its excellent noise immunity and also its elevated scalability with increased package density as compared to BJT make it a sole choice for future applications. However, one vital limitation of MOSFET is the poor frequency response with respect to BJT owing to the presence of numerous parasitic capacitances.

Power consumption in MOSFETS

For an inverter, the dynamic power consumed can be given as :

$$P_{DY\ N} = \quad f_{CLK}\, C_L\, V_{DD}^2$$

We can see that the dynamic power has square dependence on V_{DD}. Hence if we for example, say scale down V_{DD} by 2, the dynamic power of the inverter will come down 4 times. The constant here is the activity factor of the particular node, which is defined as the probability of a particular node switching. f_{CLK} is the frequency of the clock signal applied. C_L is the load capacitance (contribution of all parasitic capacitance of the inverter).

The static/steady state power dissipated in the inverter is given as :

$$^{P}\text{LEAK} = \text{ILEAK VDD}$$

I_{LEAK} denotes the leakage current through the transistors when they are in Off State.

The power consumption of an operating MOSFET can be categorized into two types: Active Power consumption and Dynamic Power consumption.

Static Power Consumption

The existence of leakage current in a device due to the presence of certain parasitic components is mainly responsible for the static power consumption. The parasitic components refer to the gate to source leakage, gate to drain leakage, direct drain to source leakage and drain to bulk leakage that contribute to the overall leakage current (I_l) of the device. Thus, the static power consumption can be expressed by:

Total Power = Dynamic Power + Static Power

Dynamic Power = A * C * $V_{dd}2$ * f

Static Power = V * I_{leak}

I_{leak} = Leakage current from sub-threshold, gate oxide leakage and reverse biased diodes

A = Fraction of gates actively switching (switching activity passed to power tools as SAIF file)

C = Total capacitive load of all gates

Vdd = Supply voltage

f = Frequency of operation

P_{st} $I_l V_{dd}$ ($I_{d,l} I_{g,l}$) V_{dd} with V_{dd} denoting the supply voltage.

The chief source of leakage current ($I_{g,l}$) is the tunneling of carriers through the gate dielectric of MOSFET and its intensity is determined by the thickness of the dielectric and the barrier height. Although, conventional silicon dioxide is preferred in MOSFET devices for ease of fabrication, however, to keep in pace with the aggressive scaling demands, the proportionate downsizing of the oxide thickness has resulted higher tunneling possibility of carriers through the dielectric thereby increasing the leakage current. An effective solution to this problem as proposed in contemporary research reports is the application of high-k gate stack in MOSFET that will achieve the same range of oxide capacitance using thicker layer of oxide and will consequently prevent the tunneling of carriers through the gate oxide.

On the other side, the leakage across the drain side ($I_{d,l}$) has mainly three following components:

a. leakage from the drain region to bulk which is referred as gate induced drain leakage
b. leakage due to transfer of carriers from source to drain directly
c. leakage under subthreshold condition between source and drain regions

Thus, $I_{d,l}$ can be represented as: $I_{d,l} I_{direct,t} I_{GIDL} I_{sub,th}$

Dynamic Power Consumption:

This sort of power consumption is mainly attributed to the switching action of the MOSFET. Applying proper gate bias switches the device to ON state condition, while some built up charges in the channel region are transported to the source/drain contacts and across the gate terminal. As the device is turned OFF on removal of supply voltage, these charges are required to be emptied from the device. However, this phenomenon is irreversible in nature resulting dissipation of power.

Considering f as the switching frequency, the dynamic power consumption is expressed as : $P_{dy} fC_{ox}V_{dd}^{2}$. Here, C_{ox} is the gate capacitance which stores the energy for charging and discharging the device while switching.

Total Power dissipation

$$Pdp + Pdn = (C_L/tp)\,(V_{DD})^2$$
$$= C_L.\,f.\,(V_{DD})^2$$

Taking node activity factor α into consideration:

The power dissipation $= \alpha\, C_L.\,f.\,(V_{DD})^2$

MOSFET scaling and its consequences:

The progressive advancements in modern digital world and computational speed are driven by the advent of Integrated Circuits introduced by Jack Kilbey at Bell Labs. This momentous growth is further sustained by uninterrupted device scaling or miniaturization following the exponential trend of Moore's law. The incessant improvisation in scaling techniques accompanied by increased device density on a single chip have resulted boosted computing capability and high performance systems at affordable price. As per the scaling rule of MOSFET published by Dennard, the scaling parameter α is used along with a multiplying factor of 1/α. While the doping concentrations are scaled by the factor α, the voltages are multiplied by 1/α to maintain the internal electric field unaffected.

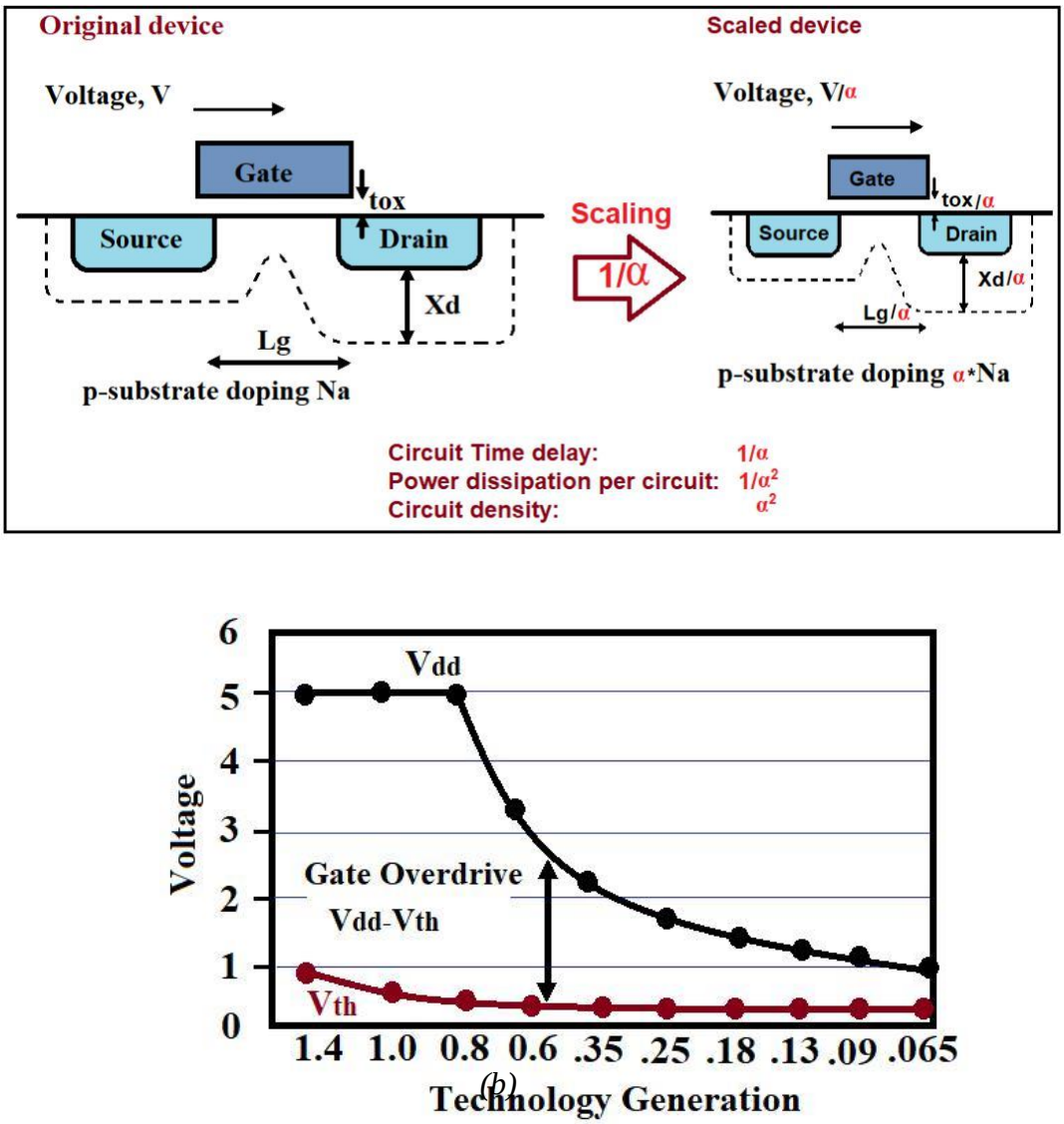


Figure. - (a) Scaling rule; (b) Scaling trend of supply voltage.

Again the speed of the circuit gets boosted by the factor α with consequent lowering of power dissipation by α2. The scaling law is depicted in figure (a). The technology trend with scaling as illustrated in figure (b) shows that threshold voltage reduction does not follow the Dennard's Rule because of the gate overdrive. To keep pace with scaling trend, device feature size is scaled every year and the number of transistors on chip gets doubled every two years as predicted by Moore's law.

This is reflected in the evolution of nanotechnology and nano-electronics from micro-regime as transistor feature size is scaled from micrometer to 100nm orders. The success of the IC industry is credited by the reduction in feature size without compromising the scaled device performance.

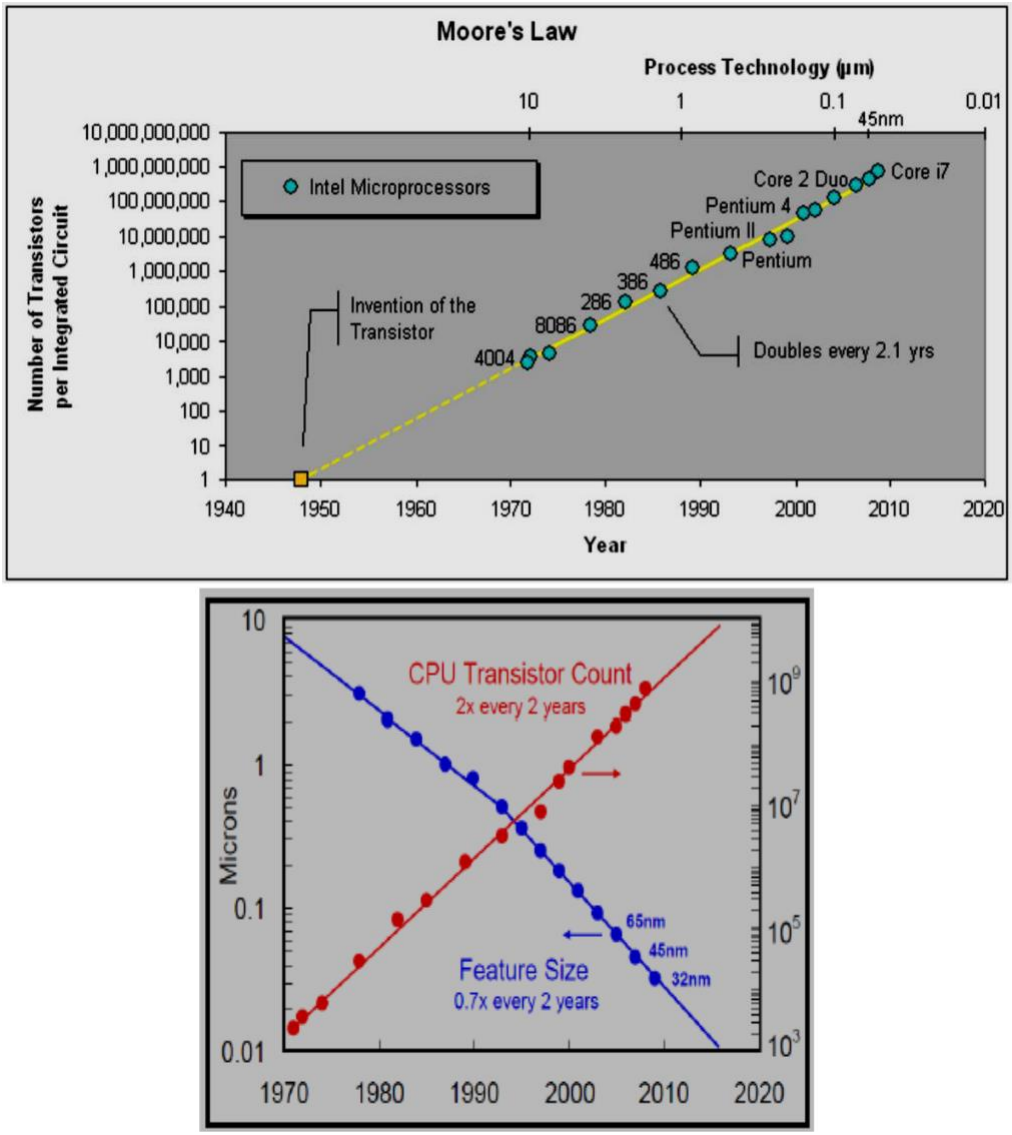


Figure. - Moore's law

International Technology Roadmap for Semiconductor (ITRS) has defined the trend of device miniaturization with future technology nodes. In figure, MOSFET scaling trend indicates the fact that with transition to each technology node, MOSFET feature size is gradually decreasing which in turn increases the integration density and its associated cost by half every two years. The major hindrance to this high package density is the increased power consumption which is now being aimed to be suppressed by adopting some ingenious techniques. Supply voltage scaling is one of the viable options to reduce the dynamic power consumption. The bias voltage has been scaled from 1.2V to 1V abiding scaling rules as per the scaling trend of 2005 to 2011. Hence, the threshold voltage is to be scaled down also to a range of 0.5V-0.6V to maintain high driving capability of the device. However, due to transistor control reasons,

This voltage cannot be scaled below 0.45V till the end of the road-map. Although a series of benefits including high integration density ICs, improved speed of operation, high complexity at reduced cost have fomented the non-stop scaling trend, there is obviously some high price that needs to be paid off to reap such radical advantages. It has been found that the normal device performance is affected by daunting short channel effects (SCEs) which degrade the efficiency of the device as its feature size is gradually reduced. This performance deterring phenomenon can be explained by the lose of electrostatic gate control over the channel due to charge sharing phenomenon between source and drain of short channel device [93-94]. Due to this reduced gate control, the device threshold voltage characteristics and subthreshold slope becomes function of channel length. Some adverse SCEs can be summarized as threshold voltage degradation, hot carrier effect, drain induced barrier lowering, random dopant fluctuation etc. Apart from such limitations, reduction in feature size also impinges the need for much higher resolution of photo-lithography, excellent process control, enhanced reliability, thinning of gate oxide layer, interconnect formation that complicates the actual fabrication of such miniaturized devices. In addition to such practical challenges, design, testing and packing of ICs containing billions of transistors pose a high alarm to the microelectronics industry.

Hence, refinement in IC technology with expensive revolutionary techniques is to be allowed in such a way that significant performance improvement can be achieved with a feasible computing hardware practically. CMOS based circuits have earned polarity due to the low power consumption of CMOS technology suitable for portable consumer applications where battery life is the major concern. Such low power

dissipation is also desirable in highly complicated circuits where however, it is very difficult to maintain the normal room temperature operating condition. With rise in temperature, the silicon becomes intrinsic in nature and the free carrier concentration within the conduction band gets dependent on the thermally generated carriers leading to device breakdown. Thus, heat sink techniques are applied which however are not fully capable to dissipate the waste heat. Hence CMOS based circuits need proper thermal management to control the power dissipation efficiently.

Thus, it can be inferred that with continuous scaling of device feature size, several complexities hamper the overall performance as well as the intrinsic properties of the device. Such affects are vulnerable in nature and cumulatively referred as short channel effects. The detrimental SCEs are discussed in detail in the following section.

Short Channel Effects:

As the dimension of the effective length of the MOSFET channel becomes comparable to its source and drain junction depths, it is referred to as the short channel MOSFET. As the long channel MOSFET approaches the short channel dimension with gradual downscaling of the channel, several vulnerable effects crop up which in turn deteriorate the performance of the scaled device. Such adverse effects are collectively termed as 'short channel effects (SCEs)' which again can be categorized as described below depending on their physical origin.

(a) 2D Electric field profile:

Unlike long channel MOSFET, where the current flow between the source and the drain through the conducting channel is reliant only on the vertical electric field; in short channel MOSFET, both the vertical and horizontal electric fields existing within the channel control the device current. This in turn limits the application of 1D Gradual Channel Approximation (GCA) concept to account for some of the device characteristics as evident in nano-scale regime. The significance of such two dimensional electric field distribution is elaborately described below.

(1) Drain Induced Barrier lowering (DIBL) :

The effect of drain induced barrier lowering (DIBL) common in short channel MOSFET devices is manifested by threshold voltage degradation /roll off which reveals a sharp decay in threshold voltage value as function of drain to source voltage with reduction in device channel length. The close proximity of the source and drain regions in short channel MOSFET makes the source and drain depletion regions to approach each other with consequent increase in horizontal electric field which otherwise could be ignored in GCA approach. Under such situation, the total charge within the channel is governed by both the gate to source voltage and applied drain bias and such condition is termed as '2D charge sharing'.

With gradual decrease in channel length, the horizontal electric field increases and eventually the gate loses control over the device channel charge which is finally being governed by the gate and drain voltages. Hence, under such circumstances, a small gate voltage is now required to attain the condition of inversion indicating a roll off in device threshold voltage with continuous scaling of channel length.

The concept of threshold voltage degradation can be further explained by the alternate prospective of surface potential barrier within the channel between the source and the drain. When the applied gate to source bias is less than the threshold voltage of long channel MOSFET device, surface inversion is not achieved and the potential barrier is high enough to prevent the flow of carriers from source to drain region in the absence of inverted channel. When suitable gate voltage is applied to reach the condition of inversion, the potential barrier gets lowered allowing the thermionic emission of carriers from source towards the channel driven by the electric field. Thus, it can be inferred that the applied gate bias solely controls the potential barrier height in case of long channel MOSFETs which however follows a complex nature in case of short channel MOSFET where both the gate and drain biases modulate the barrier height. Thus, under such circumstance, even if the gate voltage is lower than the threshold voltage, the applied drain bias tends to lower the potential barrier facilitating the flow of carriers from source to the drain region thus resulting an undesired subthreshold current conduction. Such phenomenon of barrier lowering due to applied drain bias leading to current flow in subthreshold state is termed as drain induced barrier lowering and is recognized as one of the detrimental short channel effects as shown in figure.

As the drain bias increases, the depletion region across the drain encroaches into the channel gradually leading to the lowering of potential barrier height;

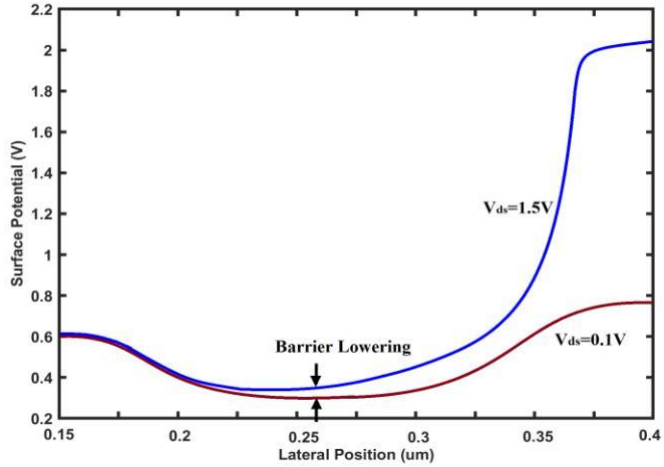


Figure. - Surface potential variation along lateral position.

Thereby attaining subthreshold conduction at lower value of gate voltage. DIBL is usually measured as the difference of threshold voltage between a low and a high drain bias. Thus, a device with high value of calculated DIBL exhibits high threshold voltage decay and increased OFF state leakage conduction.

(2) Effect of gate induced electric field on carrier mobility:

With the progressive reduction in transistor channel length, the thickness of the gate oxide is also downscaled proportionately in addition to other physical dimensions of the device. With gradual scaling of gate oxide thickness, the vertical electric field intensity as directed from the gate electrode increases towards the channel making the transverse electric field dominant. This in turn pushes the electrons towards the oxide-substrate interface which suffers collision and gets scattered rapidly degrading the mobility of the electrons in silicon crystal. As the electrons move along the channel being very close to the interface, a small increase in transverse electric field will eventually lower the surface mobility to almost half of the bulk mobility.

(b) High electric field strength within the channel

With the shortening of channel length, a notable increase in the electric field is observed as the voltage source are not scaled proportionately. Hence, a series of vulnerable effects are observed in such short channel devices due to this uncontrolled rise in electric field which may ultimately cause device breakdown.

Saturated carrier velocity: One of the significant consequences of high channel electric field is the saturated carrier velocity. At lower values of electric field, the carrier velocity exhibits a linear dependency on channel electric field. However, as the channel length is gradually scaled, the electric field within the channel increases and as it reaches a critical value, the carrier velocity gets saturated. The linear relation of carrier velocity with electric field thus no longer exists at such high electric field due to increased scattering of such highly energized carriers which now takes longer transit time to flow through the channel. Drift velocities of both electrons and holes get saturated at above 100kV/cm of applied electric field while for short channel devices, the drain side electric field attains value as high as 400kV/cm.

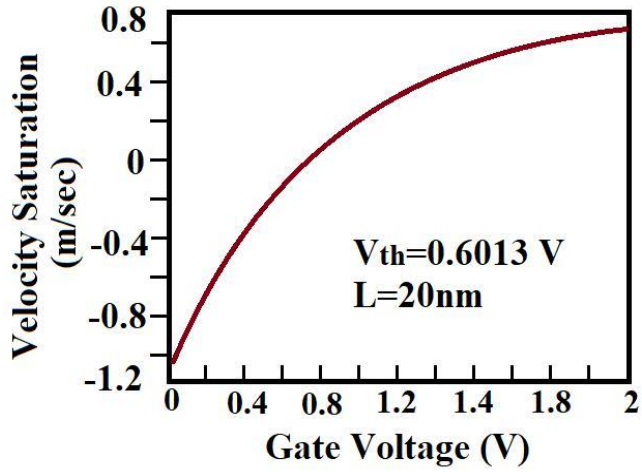


Figure - Saturation in carrier velocity with incremented gate voltage

Impact on ionization: The electric field induced impact ionization at the drain end is another adverse SCE due to the application of sufficiently high electric field in a short channel MOSFET. With channel length reduction, the electric field increases considerably at the drain side and initiates the impact ionization phenomenon. The carriers while moving from the source towards the drain under the influence of high electric field gain sufficient kinetic energy to knock an electron from its bound state in valence band and promote it to a free state in the conduction band thus generating an electron-hole pair as depicted in figure.

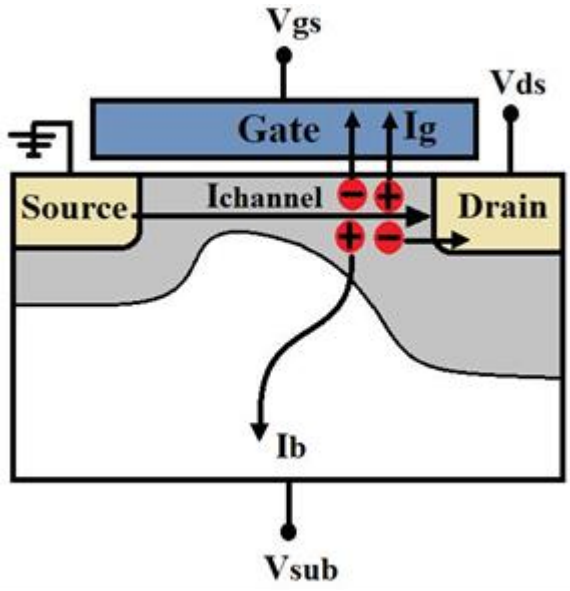


Figure. - Generation of electron-hole pairs due to electric field induced impact ionization

Electrons generated in such way regain more kinetic energy from the high channel electric field and create more electron-hole pairs cumulatively. The generated electrons from electron-hole pairs get accelerated towards the positively biased drain side while holes migrate to the substrate resulting parasitic substrate current. The accumulation of holes in the substrate creates a voltage drop which may be sufficient to forward bias the normally reverse biased source/substrate junction. When it exceeds the junction built-in potential value, the junction becomes forward biased injecting several electrons from the source to the channel thereby increasing the current. The electrons thus newly injected; again come under the influence of existing high electric field at the drain side and gain sufficient kinetic energy to initiate the electron-hole pair generation. Thus, this high electric field induced impact ionization is referred as a cumulative process and acts as a major performance deterrent factor for short channel devices.

Parasitic bipolar effect:

This parasitic bipolar effect is an after effect of impact ionization where excess electron hole pairs are generated repeatedly at the drain end under the influence of high electric field. While the electrons get swept towards the drain side of nMOS, the generated holes are accumulated within the p-substrate. The injected holes build a net positive charge in the substrate with respect to the grounded source which in turn forward biases the otherwise reverse biased source/substrate junction. Thus, a parasitic transistor is created with n-type source, p-type substrate and n-type drain giving rise to the parasitic bipolar

effect. Such forward bias of the substrate/source junction encourages further injection of electrons from n-type source to the p-type substrate below the inverted channel of nMOS transistor. These newly injected electrons when reaches the vicinity of high electric field at the drain side again participate in impact ionization resulting avalanche multiplication of carriers. The positive feedback of parasitic bipolar effect to impact ionization threatens the device reliability even at low drain bias

Hot carrier effect (HCE):

The term ‘hot electron’ is first used by Conwell [99] to describe the behavior of electrons under non equilibrium condition in semiconductor crystal. Incessant trend of device miniaturization tends to raise the intensity of horizontal electric field between the source and drain and may be sufficient enough to heat the carriers across the drain end. Such electrons are termed as ‘hot electrons’ which gain sufficient kinetic energy at the expense of potential energy and overcome the potential barrier between the channel and the gate oxide. Existence of high electric field across the drain end of short channel MOSFETs enables these hot electrons to penetrate into the gate oxide resulting the gate current which in turn reduces the input impedance of the device. Some of the injected hot electrons also get trapped within the gate dielectric as fixed oxide charges and deteriorate the channel/oxide interface states. These hot carriers have severe adverse effect on device performance resulting device heating, degraded subthreshold slope, reduced transconductance and high leakage current

Gate oxide charging:

It can be well understood from the previous discussion that continuous scaling of device channel length increases the horizontal as well as vertical electric field within the channel region and at times becomes high enough to heat the carriers and generate hot electrons. Such hot carriers acquire high kinetic energyand surmount the potential barrier existing across the oxide-channel interface and penetrate the gate dielectric. These build-up charges eventually degrade the quality of the oxide layer and the prolonged transport of carriers into the oxide ultimately causes the electrical breakdown of the oxide. This long term degradation phenomenon is called time dependent destructive breakdown (TDDB) or hot electron ageing. To combat such alarming issue, conventional silicon dioxide gate dielectric is being replaced by high-k gate oxides like HfO2, Al2O3, TiO, ZrO with higher relative permittivity. Application of such high-k dielectrics aids realization of same

gate capacitance with thicker gate oxides, thereby lowering the probability of such breakdown issues and hence the device reliability threat associated with scaled gate oxides.

Some of the SCEs encountered due to the decrease in physical distance between the source and drain of short channel MOSFET are summarized below :

Channel length modulation: The channel length modulation (CLM) arises from the shortening of the effective channel length of short channel MOS affecting the drain current characteristics of the device

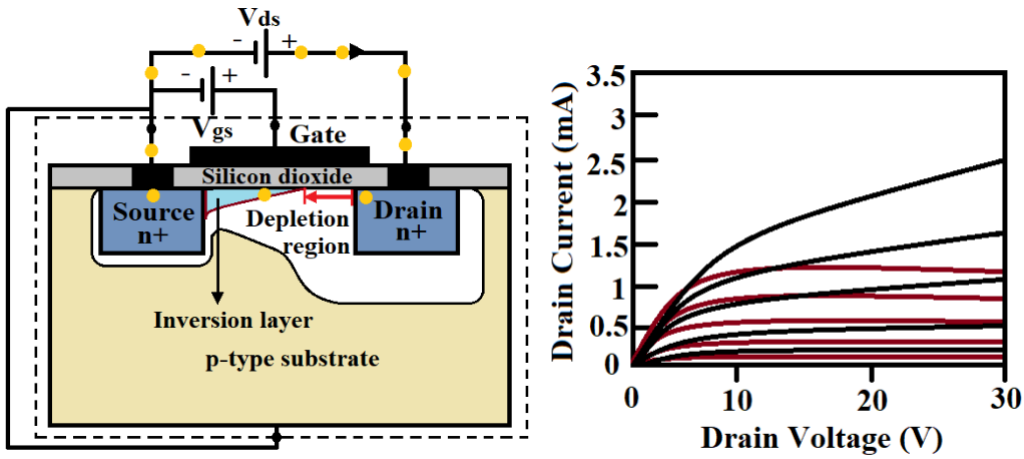


Figure. - MOSFET structure showing channel length modulation and its effect on drain current characteristics of the device.

As the drain bias is increased, the depletion width at the drain end intrudes into the channel leading to the reduction in effective device channel length which now becomes equal to the actual channel length minus the depletion region width of the source and drain region.

The effect of this channel length modulation is clearly evident in output characteristics of short channel MOSFET as shown in figure. where the current increases beyond saturation exhibiting a finite non-zero slope. The CLM effect is more pronounced in short channel device with low doped substrate than in long channel devices.

Punch through:

Punch through is considered as the ultimate consequence of channel length modulation. In short channel devices, continuous increase in drain bias widens the reverse biased drain-substrate depletion region which gradually approaches the source depletion region and merges at a certain drain bias. The effective channel length thus becomes zero and such phenomenon is termed as punch through.

The channel current under this condition increases rapidly with increase in drain bias raising the output conductance and consequently limiting the maximum operating voltage of the device.

Apart from the adverse SCEs discussed so far, some other challenging issues like source-drain resistance, gate leakage current, random dopant fluctuation and complicated fabrication techniques, affect the overall function of scaled devices.

Body Effect

The effect of body effect for short channel transistors is shown in below Figure

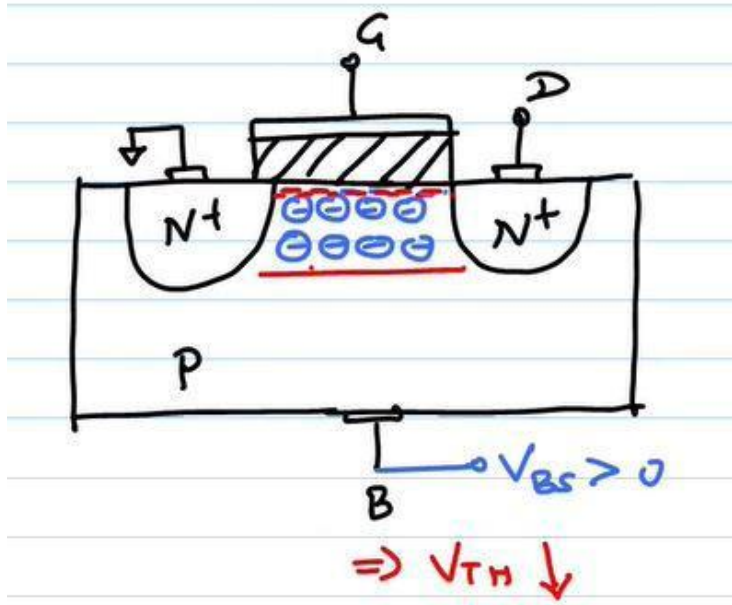


Figure. - Body Effect in short channel devices

The body bias ($V_{BS} > 0$) acts as a back gate for the transistor and helps in channel formation even before the gate voltage is applied. So now V_{GS} has to now less work to invert the channel. Hence the V_T decreases with body bias ($V_{BS} > 0$ for n-channel MOSFET).

Channel Length Modulation :

With decrease in the size of the transistor channel length also decreases creating a room for another type of short channel effect known as channel length modulation. This is depicted in Figure

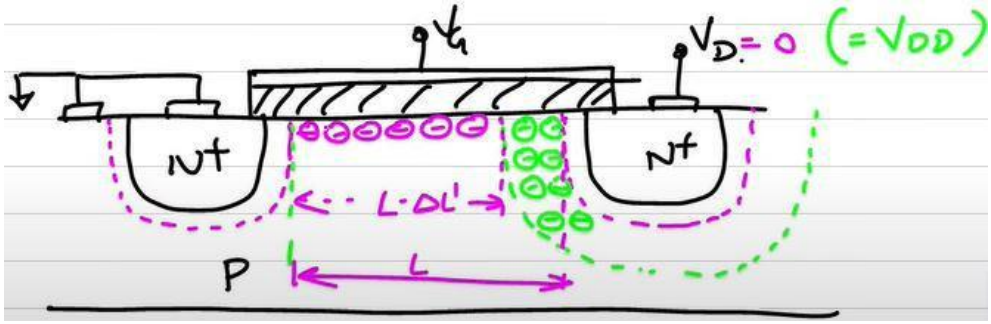


Figure. - Channel Length Modulation in short channel devices

It is evident from above that when we apply a drain potential, V_{DS}, the depletion region in the N+ region eats into the channel and depletes the channel to some extent, therefore now V_{GS} has to do less work to invert the channel. So again in this case, V_{TH} decreases. Since this phenomenon is e ective when V_{DS} is large, hence it can be seen in saturation region. The current equation for MOSFET in saturation was given as :

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Now the new drain current equation becomes

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

where is the CLM parameter whose units are in V^1

Velocity Saturation

Velocity saturation is the phenomenon where due to supply voltages being dropped for downsizing of transistors, so as to avoid breakdown of the device operation; the velocity tends to saturate for a particular V_{ds} value. This saturation of V_{ds} makes the device operation to go into saturation well before the long channel device with same parameters could go into saturation. This is depicted in the Figure below :

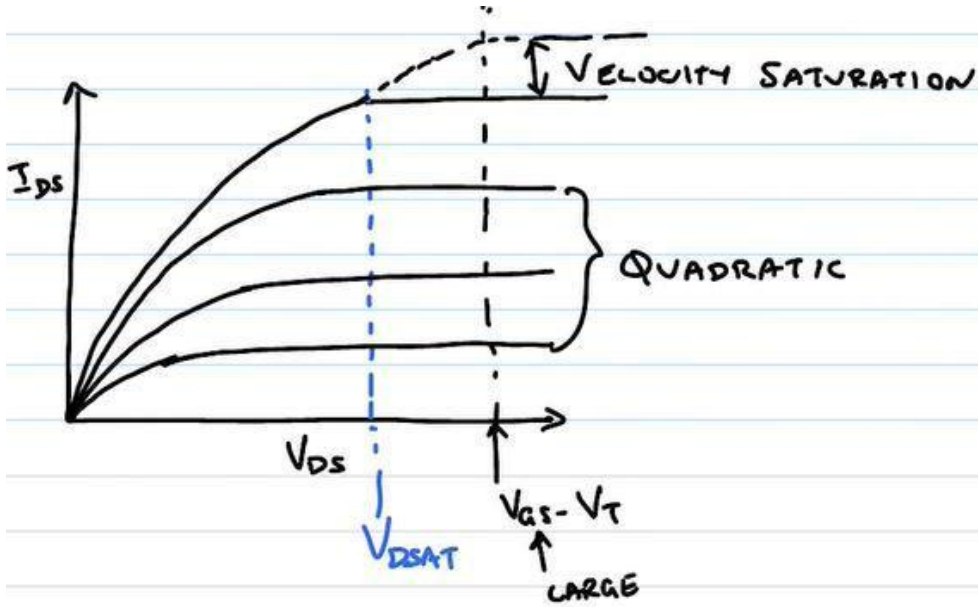
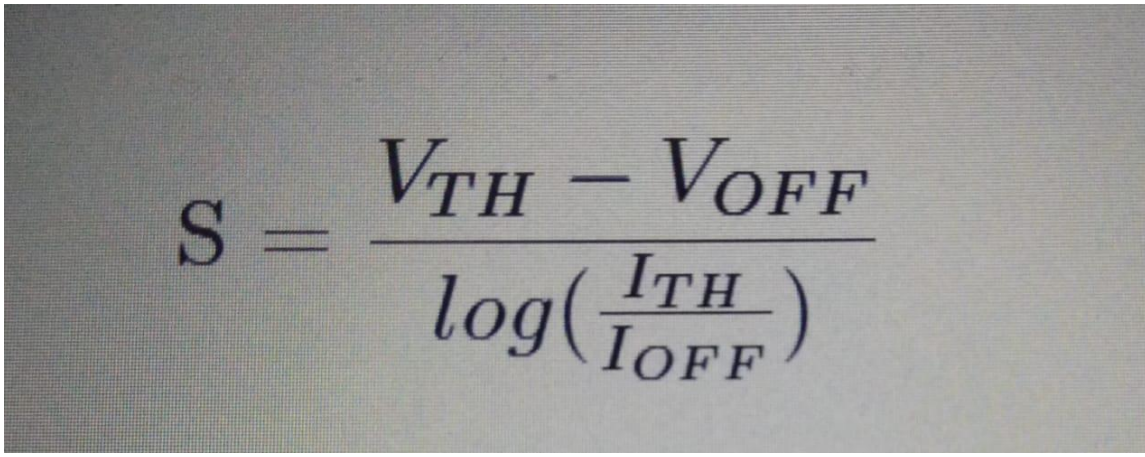


Figure. - Variation of output characteristics due to Velocity Saturation in short channel devices

Subthreshold Slope and Avg. Subthreshold Slope

The subthreshold swing is de ned by $S = (d\log I_D/dV_{GS})^{1}$ in units of mV/decade, and in the MOSFET, it is independent of V_{GS} below the threshold voltage. For the TFET, the tunnel current can be described.

Several ways to de ne subthreshold swing have been proposed for the TFET. The most often used method, as illustrated by the reports summarized is to give the tangential inverse slope of the I_D-V_{GS} curve at the steepest part of the characteristic. Bhuwalka and Boucart and Ionescu have proposed an equation, which will provide an average swing



$$S = \frac{V_{TH} - V_{OFF}}{log(\frac{I_{TH}}{I_{OFF}})}$$

where $V_{T\,H}$ is the threshold and $V_{OF\,F}$ is the voltage below threshold at which the OFF current, $I_{OF\,F}$ is a minimum. Here, the problem is to de ne the threshold voltage and for this constant current method can be applied. For example, as in the MOSFET, the threshold current can be de ned as $I_{T\,H} = 10^{\,7}=L_G$ ampere, where the gate length L_G is given in nanometers.

A new definition for the TFET threshold voltage, proposed by Boucart and Ionescu has the threshold voltage de ned as the voltage where the $I_D\{V_{GS}$ or $I_D\{V_{GS}$ characteristics transitions between quasi-exponential and linear dependence on the drain current. In this method, two threshold voltages are determined. This de nition has the disadvantage that it depends strongly on the TFET junction design and gate geometry.

We propose a practical definition for effective subthreshold swing which anticipates the voltage scaling attribute of low-subthreshold-swing devices. First, de ne the threshold voltage to be half the supply voltage, i.e., $V_{T\,H} = V_{DD}/2$ and $I_{T\,H} = I_D(V_{GS} = V_{DD}/2)$. In this definition, the o -voltage equals zero, the o -current becomes the drain current at $V_{GS} = 0$, and the e ective subthreshold swing is simply de ned by $S = V_{DD}/[2\ \log(I_{T\,H}\ /I_{OF\,F}\ )]$. Basic direct current (dc) performance of the TFET is then characterized by specifying on-current, supply voltage, and effective S.

Evolution of advanced MOSFET structures

The aggressive downscaling of planar MOSFET structures suffers from several short channel effects which sought for the evolution of non-conventional device architectures to keep pace with the scaling trend specified by ITRS. Fabricational complexities and functional limitations of traditional MOS at low dimension make it unsuitable for implementation in nano-scaled integrated circuits. Further diminution of MOSFET feature size faces various challenging issues in terms of saturation current while lowering the leakage conduction, reducing the power supply and achieving uniform device parameters within the chip. Hence new alternative devices referred as "non-classical CMOS" with newer structural designs and materials pave a new path towards the explosive growth in microelectronics industry.

Here, some advanced MOSFET architectures and their structural benefits are described below:

Silicon On Insulator (SOI) MOSFET:

The main inspiration to switch from conventional MOS to Silicon On Insulator (SOI) MOSFET technology is to widen the scalability of CMOS with enhanced

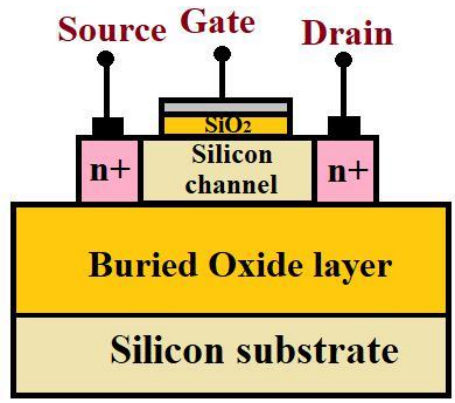


Figure. - Cross-sectional representation of SOI MOSFET.

device performance so that they can override the future silicon technology. Like MOSFET, it also maintains silicon as the starting material for fabrication of integrated circuits owing to the low cost of silicon and its ability to form a good quality oxide with smooth interface over device channel.

The exclusive feature of SOI structure is the existence of a thick layer of silicon dioxide (orders of 100 nm) embedded between thin layer of silicon channel (orders of 10 nm) and silicon substrate. The thick oxide layer referred as the buried oxide layer (BOX) can be grown by oxidation or by implantation of oxygen into the silicon wafer. The thin silicon film over the BOX layer is the 'silicon channel' while relatively thicker silicon layer below the BOX is the 'SOI body'. The cross-sectional view of SOI MOSFET is shown in figure.

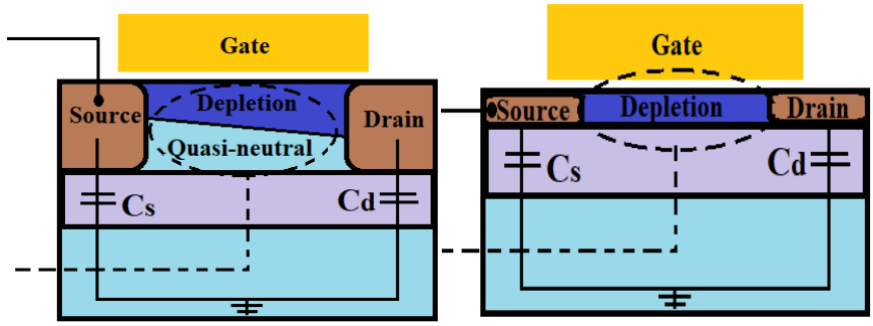


Figure. - Cross-sectional view of (a) PD SOI MOSFET and (b) FD SOI MOSFET.

Depending upon the thickness of the silicon channel, SOI MOSFET can be operated either in partially depleted (PD) or fully depleted (FD) mode of regime

as shown in figure In partially depleted SOI structure, the depletion region does not fully cover the silicon film hence leaving undepleted neutral silicon layer even when the device is operating under inversion condition on application of suitable bias voltage. Thus, the thickness of the silicon film exceeds the maximum gate depletion width and this undepleted region at the back interface acts as a floating body in PD SOI MOSFET. In contrast to this, in FD SOI MOSFET, the silicon film with thickness less than the gate depletion width causes the entire silicon channel to be depleted even before achieving the threshold condition. The relatively thinner silicon film eliminates the floating body effects while the presence of very thick buried oxide reduces the junction capacitance in FD SOI. Some of the notable advantages of SOI MOSFET are reduction in source-substrate and drain substrate parasitic capacitance with momentous improvement in speed, power consumption and performance gain of the circuits, additional isolation between adjacent SOI devices due to the existence of thick BOX layer which in turn

facilitates higher package density, prevention in latch up and latch up induced device breakdown, reduction in p-n junction leakage current due to the thin silicon film and its reduced source/drain junction depths, high immunity to SCEs and highly energized radioactive elements being blocked by the thick BOX layer. However, ultra-low dimensional SOI MOSFET performance is also limited by some challenging issues that degrade the short channel characteristics of the device. PD SOI MOSFET exhibits 'Kink effect' resulting drain current overshoot in DC circuits due to the combined action of floating body effect and parasitic bipolar effects which are very difficult to suppress. Again the fabrication of ultra-thin films of FD SOI requires complicated design processing and also excellent interface quality is needed at BOX/channel interface to reduce scattering. SOI is further subjected to self- heating phenomenon due to lower thermal conductivity of silicon dioxide of BOX that has a serious impact on device reliability and performance

Silicon On Nothing (SON) MOSFET:

Silicon On Nothing (SON) is considered as an improvised alternative to SOI MOSFET with enhanced scalability based on the concept of buried layer engineering. In contrast to SOI, the buried oxide layer in SON MOSFET is replaced by air gap beneath the silicon channel as shown in figure. Such structure

has been proved to provide excellent imperviousness to short channel effects with improved electrical characteristics thereby satisfying the aggressive scaling requirements of ITRS.

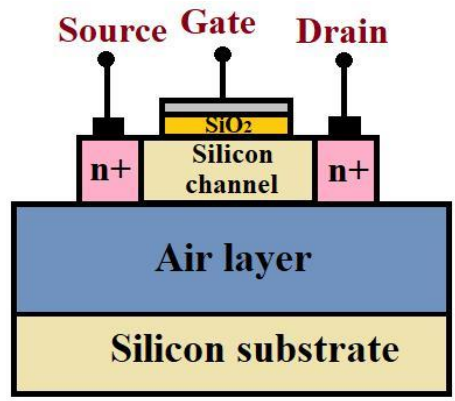


Figure. Schematic of Silicon On Nothing (SON) MOSFET.

Researchers have explored SON technology both experimentally and analytically as a lucrative option for future low power applications. The lower dielectric permittivity of the buried 'air' layer reduces the parasitic junction capacitance across the source/substrate and drain/substrate junction resulting high speed operating devices. It also offers the highest electrostatic isolation from undesirable field line penetration to the active channel region. Electrostatic coupling is also reduced through the lower dielectric air layer relaxing the requisite of ultra thin silicon film. Additional inherent features of SON include reduced power consumption, immunity to radioactive elements, improved scalability, low noise performance and faster switching performance at reduced cost.

Multi-gate MOSFET:

As already discussed, unlike long channel MOSFETs where current conduction is dominated by gate induced electric field, short channel MOSFETs experience two dimensional charge sharing with gate and drain electric field lines controlling the channel charge. Thus, the sole gate controllability over the device channel is suppressed leading to several inevitable short channel effects. Recently, multi gate MOSFET structures are emerging as potential solution to prevent the intrusion of drain side electric field lines into the channel and control the SCEs effectively. The existence of more than one gate increases the driving current capability of the device, improves the subthreshold characteristics and hence enhances the device scalability. Double-gate, tri-gate, FinFET, quadruple gate, gate all around are some of the special multi gate configuration of MOSFET structures. The double gate geometry is suggested in 1984 by Hayashi to achieve high transconductance and improved subthreshold slope with enhanced gate control. Double gate structures can be operated either as tied or independent gate. In tied gate mode, both the front and back gates are biased with the same voltage whereas in independent gate mode, the gate electrodes are independently connected to separate bias voltages. Hence, in independent mode, the front gate threshold voltage is controlled using back gate bias in contrast to tied gate mode, where the channel charge is controlled by both the gates simultaneously. Although, experimental demonstration of double gate structures has been reported in literature, existence of silicon film between the front and back gates with thickness less than the physical gate length involves complicated fabrication processes and hence commercially not so popular [15]. Trigate MOSFET is another popular structure where the active channel is wrapped by the gate on all three sides: the two side surfaces with height H and the top surface with width W. The three surfaces in

trigate configuration thus control the channel charge conduction while its corners where the side surfaces meet the top one act as critical contributor towards device operation. In FinFET, the top surface is covered by the thick layer of oxide and hence does not contribute to the conduction of the channel. FinFET has aspect ratio higher than tri-gate with 'fin width' being determined by the height and width and 'fin height' being defined by thickness of the active channel. Such gate structure modulation is further extended to gate all around configuration with gate electrode encircling the channel on all sides. Due to its unique device geometry of gate wrapped channel, the gate electrostatic control and subthreshold behavior of the device is highly improved with consequent suppression of undesirable short channel effects in comparison to single and double gate counterparts.

Gate work function engineering: Emerging performance boosting technique of scaled devices:

It is quite evident from the previous discussion that downscaling of device feature size for progressive growth of VLSI industry faces the unavoidable detrimental SCEs and associated bottlenecks that are constantly degrading the overall performance of the devices. Hence, to improve the device functional competence, novel device architectures with modulated material property are being propounded by device engineers and researchers satisfying the aggressive specifications of ITRS requirements. Gate work function engineering is another possible solution to combat the adverse SCEs while enhancing the device performance effectively thereby opening a new research avenue to explore.

Recently, metal gates are replacing the standard polysilicon gates and emerging as a suitable alternative to suppress the undesirable SCEs, polysilicon depletion effects, boron penetration, etc. However, metal gates have some inherent limitations including thermal or chemical instability with high-k gate dielectric, annealing needed to passivate the interface charges trapped unintentionally, problems related to plasma layer damage due to cross-contamination, deposition of material and reactive ion etching (RIE) and adequacy in the availability of metal work-functions.

In short channel devices, both the horizontal and vertical field constitute the resultant electric field at any point of the device. The gate electrodes with two or three metals having dissimilar workfunctions placed adjacently modulate the vertical electric field at any point in the device channel, thereby controlling the total channel electric field. This popular concept of 'gate material engineering' is termed as dual /triple material gate. The fascinating feature of such gate workfunction engineering lies in the presence of abrupt step in the potential profile at the interface of the two/three gate metals. The step profile in channel potential aids in lowering the DIBL effect by shielding the potential minima across the source side from any drain bias fluctuations and thus makes the device highly immune to SCEs. The concept of gate material engineering is further extended to the binary metal alloy gate electrode for MOSFET applications as introduced by the research group led by Tsui. Recently, ZnCdSSe alloy nanowire with continuous mole fraction adjustment has been fabricated by Pan et al. Another research outcome as reported by Christen et al. have demonstrated the fabrication of continuous compositional spread (CCS) thin film by applying pulsed laser deposition (PLD) and have verified the compositions at each position of the film with analytical values. Several experimental demonstrations of fabricated metal alloy in due course of time establish the feasibility of binary metal alloy as gate electrode of MOSFET in near future. Deb et al. further explored the idea of spatial composition graded gate electrode in SOI MOSFET where the lateral variation of workfunctions of individual constituent metals has been applied to adjust the overall electric field of the system and to reduce the short channel surface potential asymmetry consequently. Since then, several research accomplishments have been reported exploiting the popular scheme of linearly graded binary metal gate electrode in innovative short channel device architectures to suppress the DIBL effect and boost the nano-scaled device performance.

Chapter 3

Tunnel Field-Effect Transistor (TFET)

A TFET is essentially a reversed-biased p-i-n diode with tunnelling probability gate modulation. Figure. depicts a band diagram for a common TFET structure. The potential barrier between the channel and the source is so great in the off state that tunnelling does not happen. Gate voltage in the on-state narrows the potential barrier and modulates it to permit a sizable tunnelling current. According to a theoretical analysis, the SS value of a TFET can be lowered to less than 60mV/dec. More recently, various groups have demonstrated experimental findings and proved that the SS may be decreased below 60mV/dec in a specific bias range.

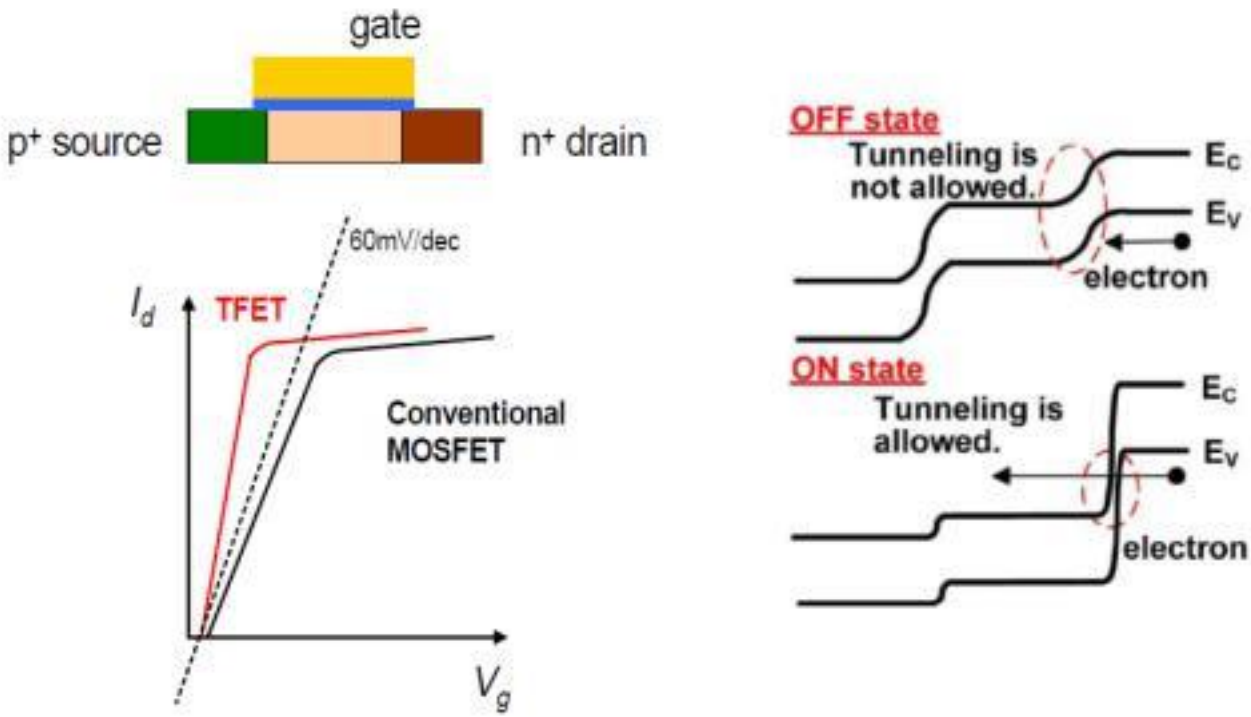


Figure : Device structure and band diagram in the ON/OFF states of the n-channel TFET, desired Id~Vg curve of TFET is shown.

Making the gated tunnelling process more effective while successfully suppressing numerous leakage paths is the main challenge with TFET. The bandgap energy, reduced effective mass, and electrical field within the tunnel barrier are three variables in the exponential term that have a significant impact on the likelihood of tunnelling, as shown in equation. Low tunnel barrier height is preferred by an efficient tunnelling process, which is dictated by the bandgap energy, and In an abrupt pn junction, a short tunnel

width typically translates to a large electrical field. The decreased effective mass is mostly reliant on the material and highly sensitive to bandstructure alteration caused by quantum confinement, strain effect, etc.

Use of tiny bandgap material is the simplest technique to improve TFET performance. Devices employing silicon germanium alloy or pure germanium as the source material have clearly reduced SS and increased driving current. It is essential to build an abrupt junction in order to strengthen the electrical field.

Unfortunately, there hasn't been much success so far in creating acute junctions in FET structures. Ion implantation dopant atoms' high energy tail is difficult to remove, and the high temperature annealing process that follows to repair implantation damage can quickly result in a widened doping profile that prevents the creation of abrupt junctions. Additionally, source to drain junction leakage current affects a TFET's SS and off-state current negatively. There are numerous techniques to prevent leakage current between the source and drain, such as using a thin channel body (10nm), a gate-all-around construction (nanowire), and a high K dielectric to maximise gate to channel coupling.

Due to the similarities in their fundamental architectures, the tunnel field-effect transistor (TFET) has emerged as one of the viable alternatives to MOSFET. The band-to-band tunnelling process underlies TFET operation, which is clearly distinct from MOSFET operation.

TFETs are a fantastic choice for low-power applications like memory devices since they can produce subthreshold swings (SS) lower than 60 mV/decade. Additionally, TFETs only rely on the band overlapping required for band-to-band tunnelling because MOSFETs have the thermionic emission threshold for channel construction. High ION/IOF F can be achieved with TFETs. TFETs can dissipate relatively little dynamic power since they have low supply voltage requirements and low threshold voltages.

To improve TFET performance, many researchers tried to structure engineer them. To enhance the ION, some researchers have experimented with lower bandgap materials. However, this could cause the IOF F current to increase significantly, which would result in more static power dissipation. Other research attempted to model TFETs to boost ION while maintaining a low IOF F, but at the same time the complexity of the process rose. The ON current was increased by a few researchers that attempted to engineer the channel from conventional to L-channel to U-channel by enabling both line and point tunnelling to enter the picture.

TCAD simulations of TFETs, like the one in this thesis, are significant in a number of ways. In order to better understand the device physics and the tunnelling likelihood inside the device, we have presented the Electric eld vector distributions. Using 1D or 2D cross-sections, it aids in our ability to look through the apparatus. We have taken steps toward optimising the device settings at various drain heights through simulations.

In this thesis, we present a simulation-based, definitive TFET structure engineering that will aid in the creation of future models and a deeper comprehension of the device.

MOSFETs vs TFETs :

MOSFETs have been around for a while. Over the years, it has had quite good downscaling. MOSFETs are still good candidates for the scaling of transistors that Gordon Moore's Law predicted would occur. But as dimensions have shrunk over time, MOSFETs have become much more vulnerable to short channel effects and power loss.

The fundamental result of scaling is that for nodes with advanced technology, the gate overdrive voltage (VGS-VT comparable to VDD - VT) almost always stays constant (short channel lengths). Reduced ON-current has a negative impact on device performance metrics such the ION/IOF F ratio and dynamic speed (CVDD/ION) when gate overdrive voltage drops. There are two potential remedies for the issue of the advanced technology nodes' low on-current. Increase VDD; decrease VT.

Working Principle:

The operating principles of MOSFETs and TFETs differ because TFETs exhibit the phenomenon of band-to-band tunnelling while MOSFETs operate through the thermionic emission of electrons.

The discharge of electrons from an electrode as a result of temperature is known as thermonic emission. This happens because the thermal energy applied to the charge carrier overrides the material's work function. Ions or electrons may serve as the charge carriers. Following liberation, a charge initially remains in the liberating zone that is equal in magnitude and opposite in sign to the total charge liberated. The emitter will finally be in the same state as it was prior to freedom if the liberator is attached to a battery, where the charge left behind is neutralised by charge supplied by the battery as the liberated charge carriers migrate away from the liberator**.**

When the valence band of the P-type region and the conduction band of the intrinsic region are parallel to one another, band to band tunnelling occurs. Current can flow across the device when electrons from the valence band of the p-type area (Source) tunnel into the conduction band of the intrinsic region (Channel). The bands get out of alignment as the gate bias is decreased, and current flow is cut off. Both TFETs and tunnel diodes exhibit band-to-band tunnelling.

TFETs are an attractive option for low-power electronics because, despite the structural similarities between MOSFETs and TFETs, their fundamental switching mechanisms differ. Instead of adjusting thermionic emission over a barrier like conventional MOSFETs, TFETs switch by modifying quantum tunnelling via a barrier. This explains why the thermal Maxwell-Boltzmann tail of carriers, which in ideal conditions restricts MOSFET drain current substhreshold swing to around 60 mV/decade of current at normal temperature, does not apply to TFETs.

Below Figure. shows the difference in their working principles.

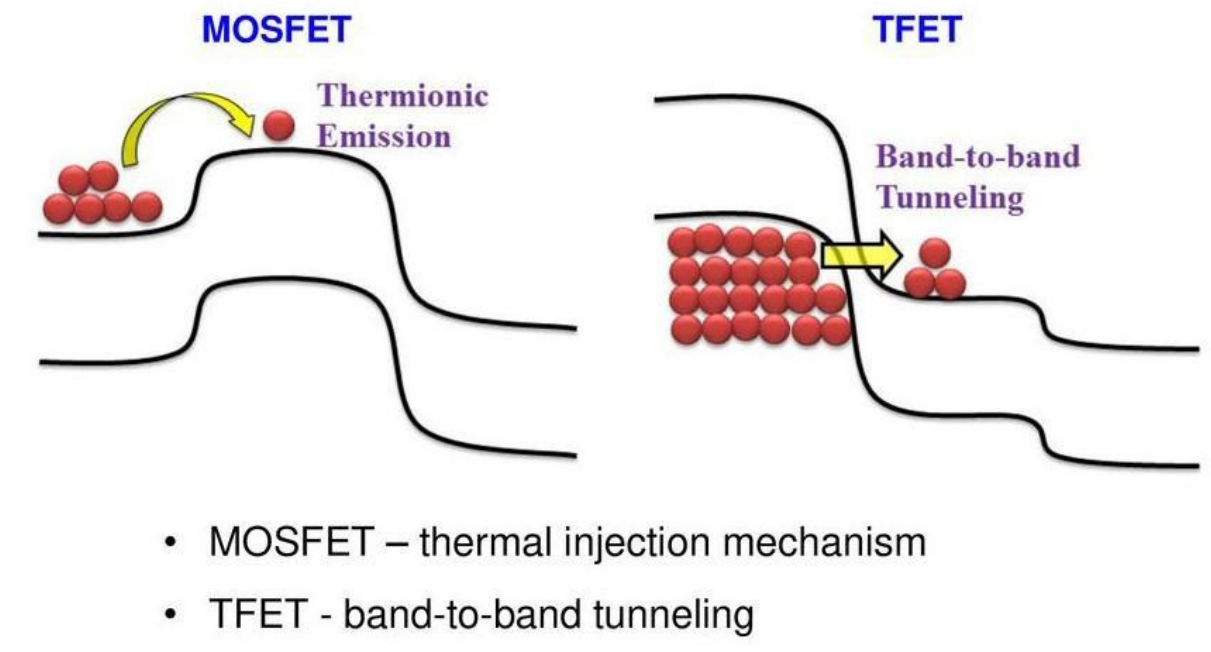


Figure. - Working principle of MOSFET vs TFET

Tunneling Mechanisms

The TFET is made up of two parts, according to Wang . The source-channel interface is where the first component, known as "point tunnelling," occurs. This component's dominant contribution is confined to a narrow region. The source region overlapped by the gate contains the second component, called "line tunnelling." Line tunnelling is the term used to describe this phenomena because the area where BTBT originates resembles a line.

Line Tunneling

There have been in-depth studies on TFET devices for ultralow-power and high-performance operation over the past 15 years. Tunneling phenomenon permits functioning at sub-60 mV subthreshold levels, which may reduce leakage and enhance ON-current at lower supply voltages. Despite numerous improvements, including SiGe sources, high-source spacers, low drain doping, highly doped sources, abrupt source junction profiles, post-silicidation implants, bandgap engineering, and double-gate topologies, the early TFETs (gated p-i-n diodes) had incredibly low ON-currents. The main cause of this was the small amount of tunnelling cross section or area present in gated p-i-n diodes (also known as point tunnelling FETs). Devices for vertical tunnelling, area-scaled tunnelling, and line tunnelling were developed to address these issues, and in theory they demonstrated greatly increased ON-current, decreased leakage, and subthreshold slope (SS) due to the gate-field-aligned binary tunnelling mechanism and increased tunnelling cross section.

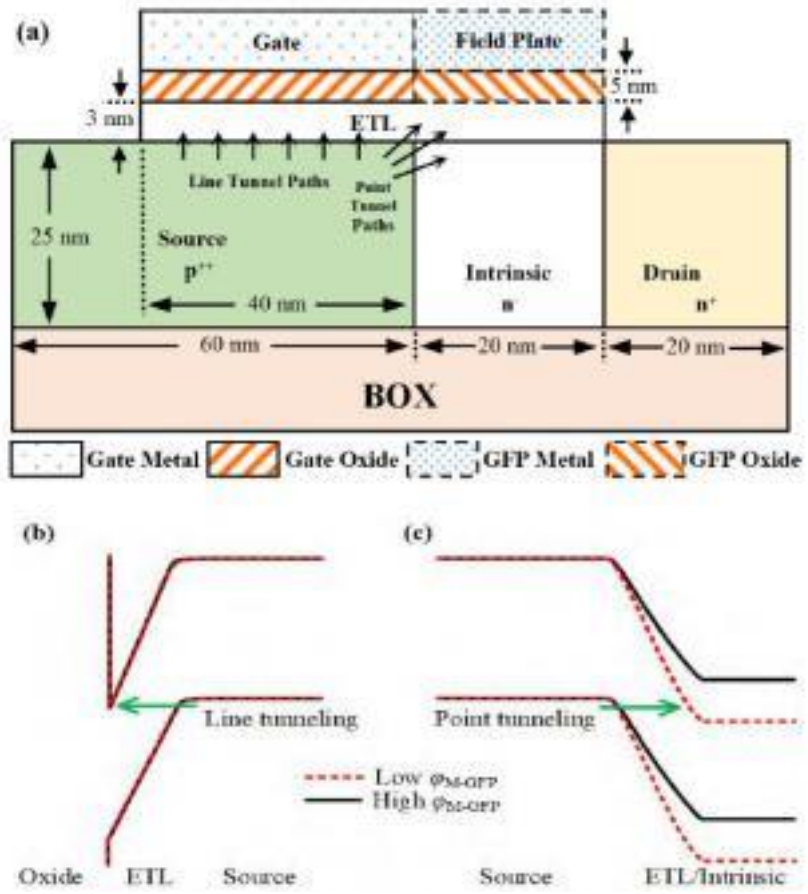


Figure : Energy Band Diagram for Line Tunneling and Point Tunneling

Point Tunneling :

At the source-channel interface, two-dimensional tunnelling is discussed in this section. A depletion area forms at the source-channel interface, the channel potential changes, and a little amount of charge flows into the channel from the drain when a positive Vgs is applied. A modest depletion region is sufficient in the case of a highly doped source, which is necessary to provide a large on-current, to create a significant electric field in the channel.

Bandgap and dielectric thickness have a significant impact on the on-current caused by point tunnelling. A smaller onset voltage will result from a smaller bandgap. VF B plus Eg = Vonset. As a larger doping level will affect the metal-semiconductor atband voltage, it is advantageous for a reduction in the onset voltage.

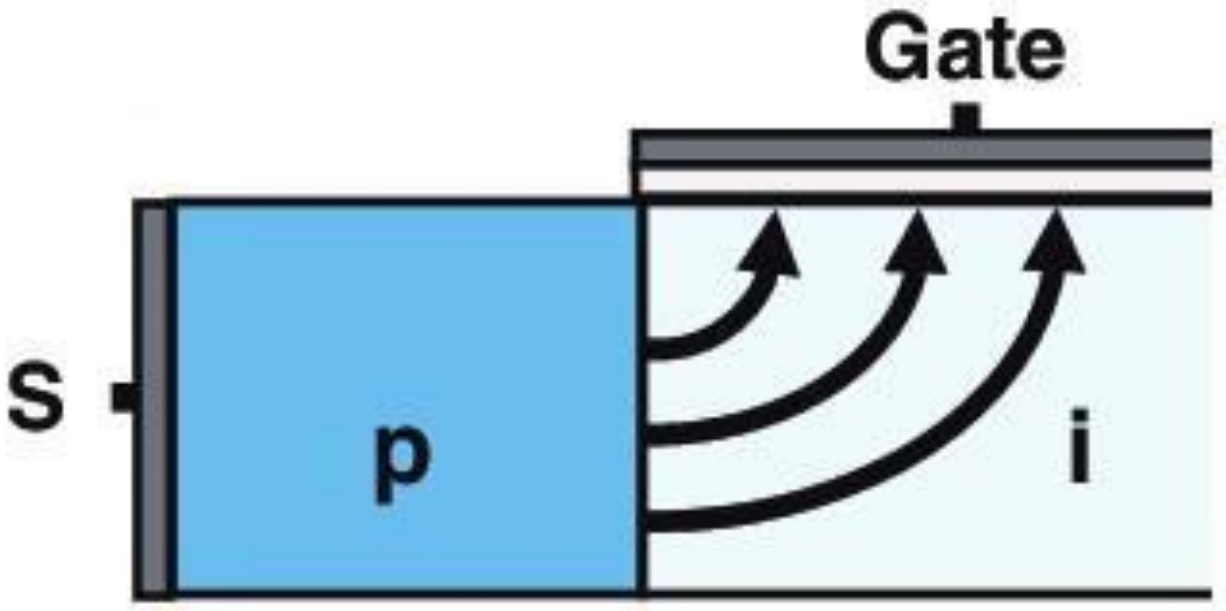


Figure -Point Tunneling from Source to Channel

Line Tunneling :

This section examines source region tunnelling in the direction perpendicular to the gate electrode, which is significant at high gate voltages.

A depletion region will be generated when a positive Vgs is applied, allowing the potential to be treated in one dimension. An inversion layer can occur at higher gate voltages, but since the electrons in the inversion layer significantly occupy the conduction band, we can ignore their contribution to the BTBT production current and simply assess the latter for the depletion region. An analytical formula for the line tunnelling current is produced by this treatment.

The lack of a 60 mV/decade subthreshold-slope is indicated by the square reliance on the Vgs. With a smaller band-gap and more doping, the ion increases. As long as it doesn't compromise the TFET Ioff, a tiny bandgap will be pursued because it lowers the onset voltage as well. The doping level will be capped by a maximum onset voltage or voltage drop over the dielectric. Finally, a thin dielectric thickness will increase the accuracy of the approximations by allowing the gate to adequately regulate the source region.

Line Tunneling vs Point Tunneling

The standard Point tunnelling device and the proposed Line tunnelling device based on Ge are shown schematically in the following figures, respectively. In line with the conventional Tunnel FET's heavily doped drain and source regions, an abrupt P-N junction is formed between the source and the channel. As seen by the white arrows, this abrupt junction is extremely important for point tunnelling. The top and rear gates of a point tunnelling device apply the same work function and bias, resulting in point tunnelling at the bottom and top of the channel. However, in a line tunnelling device, the top and back gates are used for various job purposes, and the rear gate is grounded. Additionally, there needs to be a space between the drain and the back gate.

In this manner, the road tunnelling is created, as indicated by the yellow arrows in Figure, from channel-bottom to channel prime. This back-gate engineering sacrifices the half point tunnelling current while providing the road tunnelling current to dual-gate TFET.

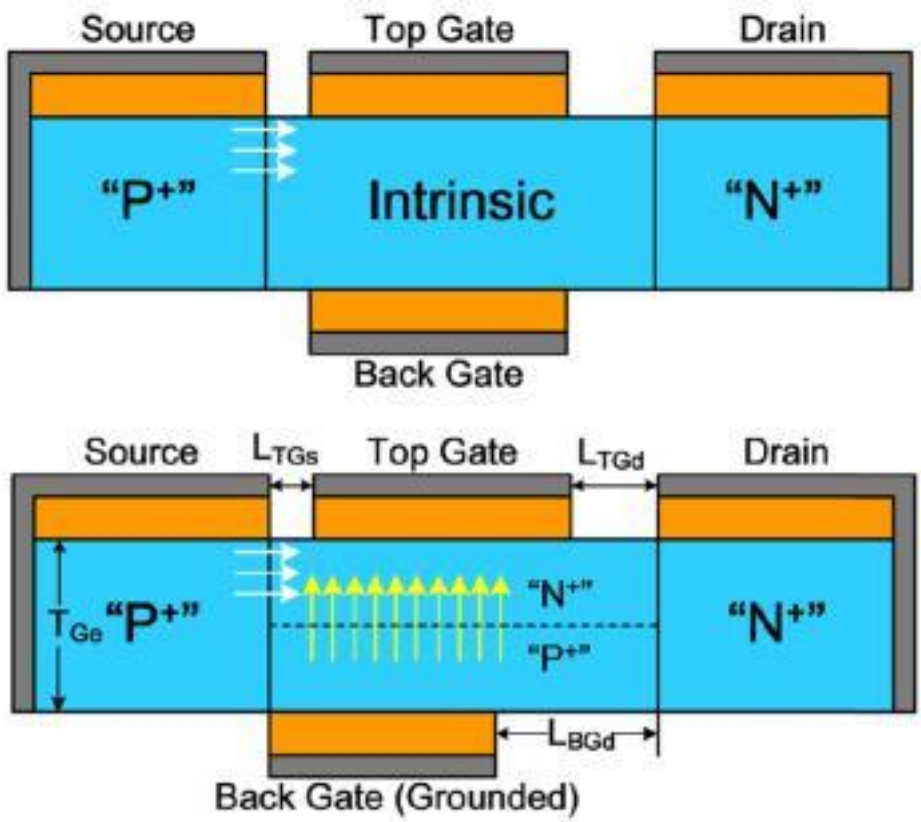


Figure. - Illustration of Line Tunneling and Point Tunneling happening in a single structure.

Line Tunneling vs Point Tunneling : Device Characteristics

At drain voltage Vd=0.5V, line tunnelling and point tunnelling devices are used. Line tunnelling device has been found to have an upper drain current. When the gate voltage (Vg) is increased to about 0.3V for a line tunnelling device, the transfer curve exhibits distortion. This is because line tunnelling begins to predominate the drain current at this voltage, but for purpose tunnelling devices, solitary purpose tunnelling controls the drain current. The rising of tunnelling current in Line tunnelling device is not obvious once gate voltage Vg is more than 1V because the pt tunnelling generation rate is greater than that of line tunnelling generation rate at the condition of larger gate voltage.

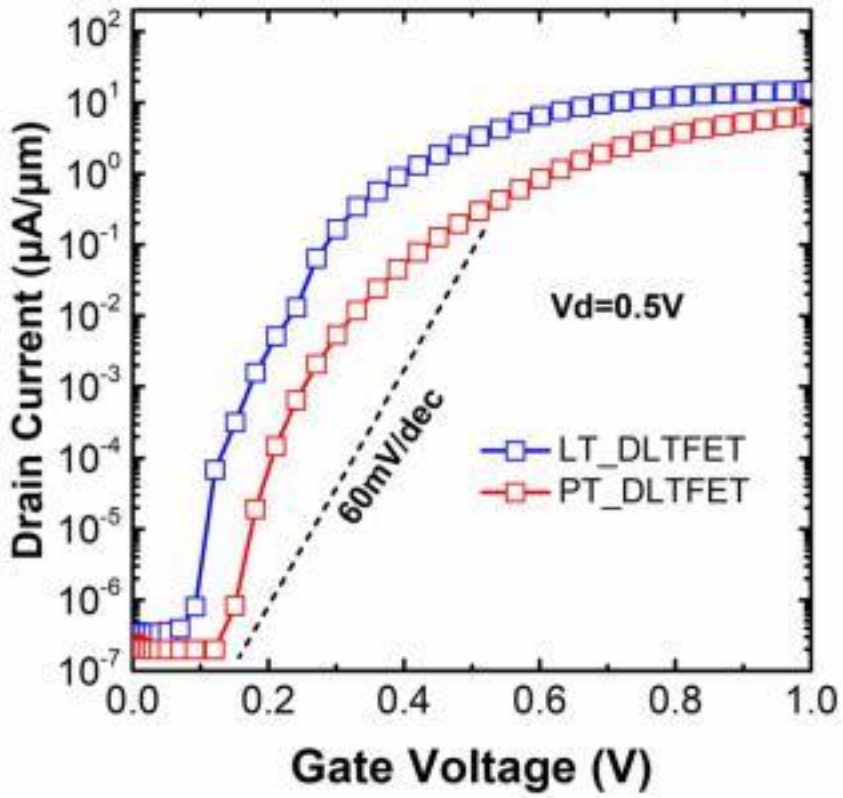


Figure: Drain Current Comparison between Line Tunneling and Point Tunneling

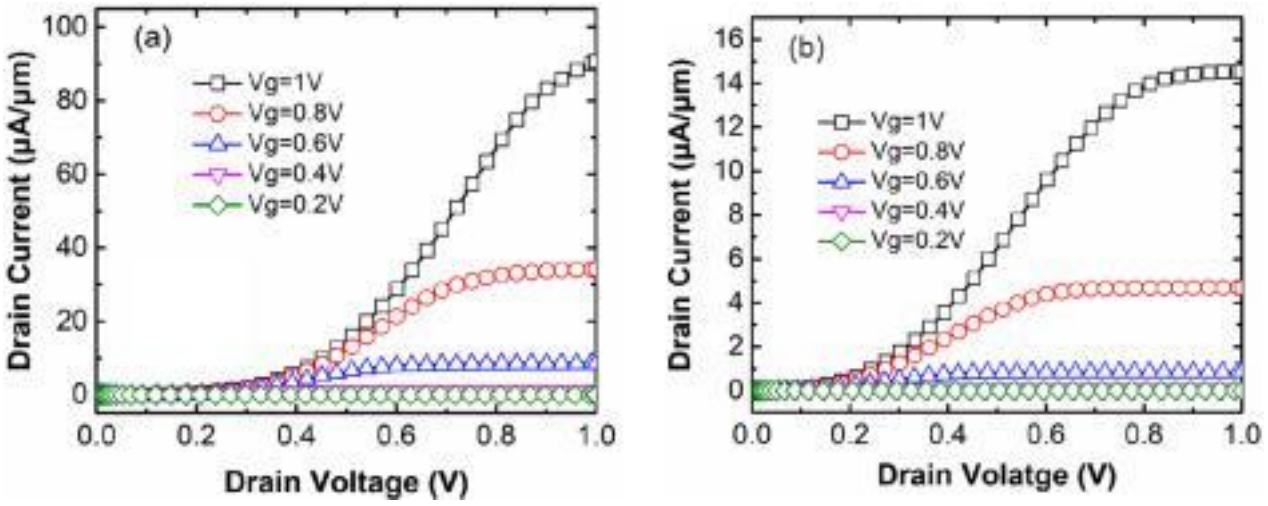


Figure : Output Characteristic Comparison between Line Tunneling and Point Tunneling

The output characteristics of those two devices are depicted in the above figure. The drain current increases linearly with drain voltage once the drain voltage is low. The drain current approaches saturation once the drain voltage has been increased to a specific amount. Additionally much more than that of a general purpose tunnelling device is the output current of a line tunnelling device.

Conclusion :

We defined numerous words associated with our theory in this chapter. The TFET has the potential to significantly reduce subthreshold swing, hence reducing supply voltage and power dissipation, according to an assessment of the technology. The development of sophisticated methods for nanoscale III-V transistors presents several technical hurdles, including gate alignment, low-interface-trap-density gate stacks, precise and abrupt tunnel junctions, and low-resistance contacts.

Simulation

Silvaco Atlas TCAD : Simulation Basics

Atlas is a physically-based 2-D and 3-D device simulator. It anticipates the electrical behavior of specified semiconductor structures using some algorithms and models and provides idea into the device physics mechanisms associated with device operation. Atlas can be used standalone or as a core tool in Silvaco's Virtual Wafer Fab simulation environment. In the sequence of predicting impact of method variables on circuit performance, device simulation fits between method simulation and SPICE model extraction.Their functions are explained below:

1) Optimization across various simulators can be provided by Optimizer..

2) DeckBuild puts forward the condition for runing Atlas command language.

3) TonyPlot the outputs which are actually the electrical characteristics of device and the structure files generated for the designed device can be seen.

4) IC layout correction is done by MaskViews.

Tony Plot provides scientific visualization capabilities. Dev Edit provides an interactive tool for structure and mesh specification and refinement. Mask Views provides an IC Layout Editor. The Optimizer supports black box optimization across multiple simulators. Atlas, however, is often used with the Athena process simulator.

Atlas may also be known as as a physically-based machine for devices because it is capable of conniving all the characteristics related to a specific device with such that structure and voltage biases at the electrodes. the total device space is split by these simulators with grids known as known as and with mesh points known as known as. By applying differential equations that area unit derived from Maxwell‟s laws, current physical phenomenon and electrical parameters at every location through the structure is set. this kind of physically primarily based simulation has several benefits like, they supply a deep insight of the attributes of a tool while not through an experiment making the device, calculation of

terribly advanced parameters area unit done terribly simply and quickly, estimation of the trends with the varied properties of the device in step with its totally different bias conditions are often calculable through these simulations.

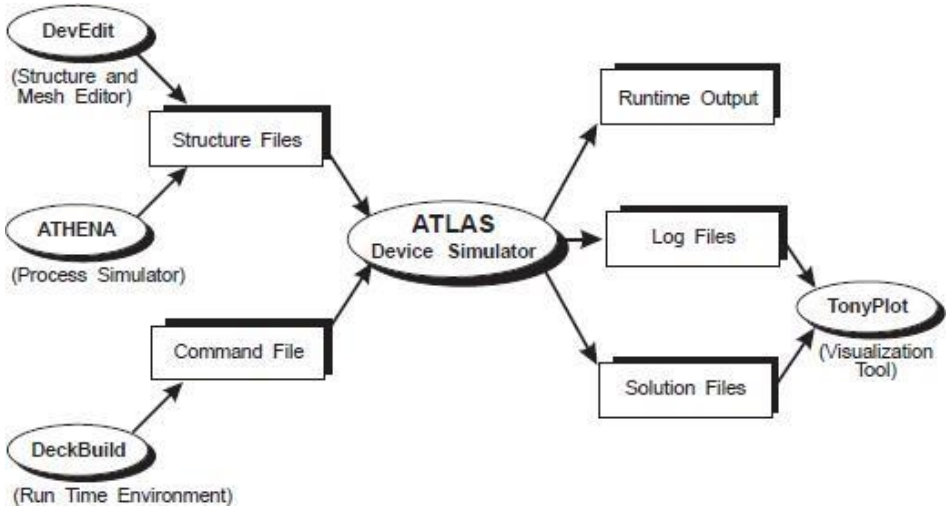


Figure : Inputs and Outputs of Atlas device simulator

Information flowing through Atlas device simulator can be seen in above diagram (in the Figure). The text file, which contains Atlas command language and structure file, which has the structure on which simulations has to be performed are the two input files to Atlas device simulator. Atlas has three types of output files: runtime output which gives the information being processed at every instant of execution of Atlas commands and simultaneously show the errors and warnings, log files which gives all the electrical characteristics which is specified in the Atlas command language and solution files which has the 2D or 3D data of the device parameters at each and every point in the device.

Steps used for defining a structure

1. Loading structure from Athena –

Atlas and Athena are interfaced for loading a structure which is described and generated by Athena. Hence, initially a structure is created and saved in Athena while it still is active. The command used for storing the device structure is:

STRUCTURE OUTF= <structure name.str> where structure name is the
file MESH INF=<structure name.str>

2. Loading a structure from DevEdit

To load structure from DevEdit the syntax for this operation is as below:

MESH INF=<structure name.str>

3. Using ATLAS Commands to define a structure.

The 1st step is to provide the mesh specification.

The following is the syntax to define meshing in Silvaco
Atlas Syntax:

MESH SPACE.MULT=<some constant value>

After this x.mesh and y.mesh statements are specified as follows X.MESH LOC=<x coordinate>SPACING =<value2> Y.MESH LOC=<y coordinate>SPACING=<value4>

After this we define different regions for the device. We use different regions so that we can dope them differently. We also use regions to create any polygon structure for our region as a single region in Atlas is always rectangular in shape. For specifying the region the following command is used:

REGION NUMBER=<value> X.MIN=< x coordinate >X.MAX=< x coordinate > Y.MIN< y coordinate >Y.MAX=< y coordinate > MATERIAL=<material1>

After that electrodes need to be specified. This is done by the following command. ELECTRODE NAME <electrode1> NUMBER = <value> X.MIN=< x coordinate >X.MAX=< x coordinate > Y.MIN< y coordinate >Y.MAX=< y coordinate > MATERIAL=<material1>

Where the name of the electrode is given as electrode 1. The location of the electrode is from x.min to x.max and y.min to y.max.

We define doping for different regions using the following syntax :

DOPING<doping profile>CONC =<value><doping type>REGION=<number>

An alternative way to define different doping for same or different regions is : DOPING<doping profile>CONC =<value><doping type> X.MIN=< x coordinate >X.MAX=< x coordinate > Y.MIN< y coordinate >Y.MAX=< y coordinate >

Contacts are very essential in any design as they are the interface between the device regions and external current or voltage sources:

CONTACT NAME<contact name>WORKFUNCTION=<value>

Contacts like N.Polysilicon, P.Polysilicon, Aluminium, Tungsten, etc. The statements used for this type of contacts are:

CONTACT NAME<f.gate> N.Polysilicon.

Specification of models

Usually the statements for MODELS are used to indicate the physical models which are required for simulations. This is excluding the impact ionization which can be specified by the IMPACT statements. The selection of the MODELS is according to the physical phenomenon occuring inside the considered device. These MODELS be divided to the following 5 categories:

1. Mobility Models
2. Recombination Models
3. Tunneling and Carrier Injection Models
4. Impact Ionization Models
5. Carrier Statistics Models

Common Models

1. Concentration-Dependent Low-Field Mobility Model:

To activate this model, CONMOB is used in the MODELS statement. This model provides the data for low field mobilities of electrons and holes at 300K for silicon and gallium arsenide only.

2. Lombardi CVT Model:

CVT in the models statement are used for activating this model. This model‟s priority is much more then all other mobility models. In this model, Matthiessen‟s rule is used for combining the components associated with mobility dependent on transverse field, temperature and doping. On activating this model by default, Parallel Electric Field Mobility Model will also get activated.

3. Shockley-Read-Hall Recombination Model:

The SRH parameter is used in the statement MODELS for activateing this model. There are a few user-definable parameters that used in the MATERIAL statement, like TAUN0 and TAUP0 the electron and hole lifetime parameters.

4. Fermi-Dirac Model

This model follows Fermi-Dirac statistics. It is usually in those regions which are heavily doped but with reduced concentrations of carrier. To activate this model FERMI is used in the statement MODELS.

Tunneling models

1. Standard Band To Band Tunneling-Model:

For high electric field, present in the considered device, tunneling of electrons can be caused by the localized electric field such that there is a bending of energy bands at the junction of tunneling. For such kind of situation standard band to band tunneling model can be used.

$$G_{BBT} = D_{\text{BB.A}}\, E^{\text{BB.GAMMA}} exp\left(-\frac{\text{BB.B}}{E}\right)$$

Where E is electric field, D is the statistical factor, BB.B, BB.A, and BB.GAMMA are user- definable parameters with default values.

BB.B= 3e7 V/cm BB.A = 9.66e18 cm-1 V-2 s-1 BB.GAMMA= 2.0

This model can be transformed to Klaassen model. For that BBT.STD needs to be replaced by BBT.KL in MODELS statement. The values of user definable parameters changes for this model. They are

BB.B = 2e7 V/cm BB.A = 4.e14 cm-1/2 V-5/2 s-1 BB.GAMMA= 2.5.

Schenk Band to Band Tunneling-Model

Phonon assisted band to band tunneling is considered for this type of model. This is a local model which contemplates constant electric-field throughout the tunneling length. Its generation recombination rate can be calculated by:

$$G_{BBT}^{SCHENK} = A\_BBT\_SCHENK F^{7/2} S \left(\frac{(A^{\mp})^{-3/2} exp\left(\frac{A^{\mp}}{F}\right)}{exp\frac{(HW\_BBT\_SCHENK)}{kT} - 1} + \frac{(A^{\pm})^{-3/2} exp\left(\frac{A^{\pm}}{F}\right)}{1 - exp\frac{(-HW\_BBT\_SCHENK)}{kT}} \right)$$

where ,

$A^{\pm}$ =B.BBT.SCHENK($\hbar\omega \pm$ HW.BBT.SCHENK)$^{3/2}$,

$\hbar\omega$ is the phonon"s energy

In this equation S depends on concentrations of the carrier.

3. Kane Band-To-Band Tunneling Model

Another local field band-to-band tunneling model is based on the work of Kane. In this model, tunneling generation rate is given by :

$$G_{BBT} = \frac{D\_BBT\_A\_KANE}{\sqrt{E_g}} F^{BBT\_GAMMA} \exp\left(-BBT\_B\_KANE \frac{E_g^{\frac{3}{2}}}{F} \right)$$

where Eg is the position dependent bandgap and F is the magnitude of the electric-field. It is similar to the standard models.

4. Non-local Band-to-Band Tunneling Model

The band-to-band tunneling models described so far in this section calculate a recombinationgeneration rate at each point based solely on the field value local to that point. For this reason, we refer to them as local models. To model the tunneling process accurately, you need to take into account spatial variation of the energy bands. You also need to take into account that the generation/recombination of opposite carrier types is not spatially coincident. Figure illustrates this for a reverse biased p-n junction where it is assumed that the tunneling process is elastic. For degenerately doped p-n junctions, you can obtain tunneling current at forward bias and consequently can obtain negative differential resistance in the forward I-V curve.

The Atlas Non-local Band-To-Band tunneling model, BBT.NONLOCAL, allows modeling of the forward and reverse tunneling currents of degenerately doped p-n junctions. It is less suitable for lightly doped p-n junctions. It is not suitable for application to the unipolar, high-field regions of a device. It is currently only available in Atlas2D. The first step in using BBT.NONLOCAL is in defining the areas where it will be applied. These areas must each contain a single p-n junction, which may be either planar or nonplanar. They have a mesh that interpolates data from the underlying device mesh and performs the band-to-band tunneling calculations on the interpolated data.

BBT.NONLOCAL thus assumes that the tunneling takes place on series of 1D slices through the junction, each slice being locally perpendicular to the junction. The slices themselves will be approximately parallel to their neighbors. Atlas has two methods of setting up these areas of slices. The first method is only applicable to planar junctions parallel to the x or y-axes. It allows you to set up a rectangular area using the QTX.MESH and QTY.MESH statements. You also specify the number of tunneling slices and the number of mesh points along the slices.

For example:

```
QTX.MESH                LOCATION=0.0
SPACING=0.25            QTX.MESH
LOCATION=1.0            SPACING=0.25
QTY.MESH LOCATION=0.99

SPACING=0.0005          QTY.MESH
LOCATION=1.01 SPACING=0.0005
```

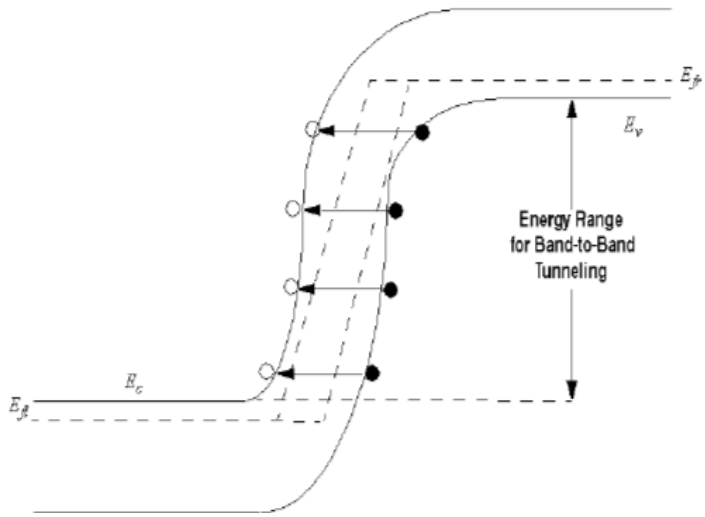


Figure : Schematic of non-local band to band tunneling.

Figure shows the tunneling of electrons from valence-band to conduction band. Tunneling of holes can also be considered. The probability of tunneling is given by WKB approximation

Numerical methods

The numerical methods are specified in the METHODS statement. To find solution there are three different types of techniques:

1. Gummel
2. Newton
3. Block

The first method finds solution for one unknown variable while the rest of the variables are constant. This process will continue until a stable solution has been obtained. Unlike the gummel method, newton method solves and finds all the unknowns at the same time. Block method is in between newton and gummel methods as it solves a few unknowns at the same time gummel is generally used for the device studied in this project i.e. the tunnel FET.

Methods to obtain solutions

To calculate current as well as other parameters such as carrier concentrations and electric fields, the device electrodes needs to be supplied with voltages. At first, electrodes are provided with zero voltages, after that the bias voltage applied is varied in small steps.

These needs to be specified in the SOLVE statements.

1. DC Solution

A fixed DC bias can be applied on the electrode by using the DC solve statements.

SOLVE <v.electrode name>=<value>.

According to this statement the required electrode, „electrode name“ is supplied with DC voltage „value“.

For sweeping the bias of a particular electrode from „value1“ to „value2“ in a particular order of steps „step1“, the following command is used.

SOLVE <v.electrode name>=<value1> VSTEP=<step1> VFINAL=<step2> NAME=<electrode name>.

Convergence can be obtained for the used equations by supplying a good original presumption for the variables that need to be evaluated at each bias point. Initial solution can be achieved by the given statement,

SOLVE INIT.

2. AC Solution

A simple extension of the DC solution syntax can specify the AC simulations. A post-processing operation to a DC solution leads AC small signal analysis. SOLVE VBASE=0.7 AC FREQ=1e9 FSTEP=1e9 NFSTEPS=10

Prediction of results

The output files of Atlas are of three different types. They are:

1. Run-Time Output

The output seen at the bottom of the Deck Build Window is the run-time output. Any errors occurring during this output will be displayed in the run-time window.

2. Log Files

These files are required for storing the terminal characteristics calculated by Atlas. It consist of the current and voltages for each electrode during the DC simulations. In transient simulations, the time is saved. Whereas for AC simulations, the conductance, capacitances and the small signal frequency are stored.

3. Extraction of parameters In Deck Build

For this the EXTRACT command is introduced inside the Deck Build environment. Thus extracting the various parameters of the device. The command has a flexible syntax that allows us to construct specific EXTRACT routines. EXTRACT can operate on the earlier solved curve or structure file.

Extract Statements used

Extract Statements	Description
extract name = "subvt" 1.0/slope(maxslope(curve (v."gate",log10(abs(i."drain")))))	To find the minimum Sub-Threshold Swing
extract name = "gm" curve(v."gate",dydx(v."gate",i."drain")) outf = "gm_curve_best_dev.dat"	To get the graph of transconductance
extract name = "Ioff" y.val from curve(v."gate",i."source") where x.val =0	To get the value of I_{OFF}
extract name = "Ion" y.val from curve(v."gate",i."source") where x.val =1	To get the value of I_{ON}
extract name = "Ion_Ioff" $Ion_n/$Ioff_n	To get the value of I_{ON}/I_{OFF}
extract name = "gm_slope" deriv(v."gate",log10(abs(i."drain"))) outf="gm_slope_best_dev.dat"	To get the graph of Sub-Threshold Slope
extract name="vt" (xintercept(maxslope(curve(abs(v."gate"), abs(i."drain")))) - abs(ave(v."drain"))/2.0)	To get the graph of threshold voltage

Chapter 4

Double Gate TFET (DG-TFET)

This chapter provides detailed explanation about our proposed TFET structure.

Proposed Structure

For the innovative two source TFET, we have developed a double gate structure to boost its ON current and demonstrate that it supports both line tunnelling and point tunnelling. In order to enhance the Ion of the TFET, our construction consists of single metal, two drain electrodes, and two gate electrodes. Better gate control and thus less substrate leakage current are provided by the dual gate arrangement. This DG-TFET has an extremely low Ioff of orders of magnitude 10^{18}. To get the best results for our threshold voltages (VT), subthreshold slope (SS), and ION/IOF F ratio, we have optimised this structure. Figure displays the 2D model of our DG-TFET.

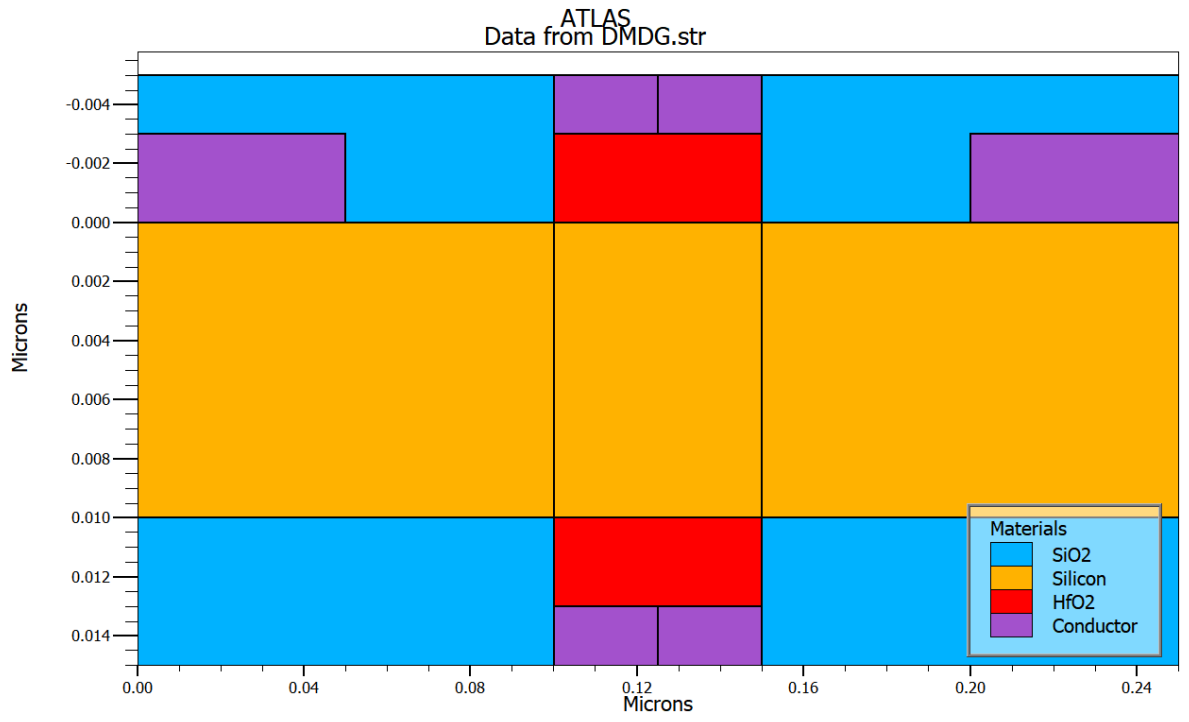


Figure : Proposed DG-TFET 2D model

The DG-TFET is uniformly doped, with high doping in the source and drain regions and moderately low doping in the channel region.

Device Simulation Setup:

The Deckbuild v-4.6.2.R programme provided by Silvaco was used to build the DG-TFET structure depicted in Figure. ATLAS 2D simulator was used to model it. The device simulator receives input from the physical models and device structure. The transfer and output characteristics of the device indicated above are then obtained by iteratively solving the Poisson and carrier continuity equation (using the Newton-Raphson method). In order to simulate the device and determine its Id-Vg, C-V, electricfields, electron concentrations (both when the device is ON and OFF), electron tunnelling, potentials, energy band diagrams, and sub-threshold slope, non-local band to band tunnelling models, Fermi statistics, and constant mobility models are used.

Electric Field vectors

The locations where the tunnel meshes should be densely populated in order to provide a clear picture of the tunnelling current are indicated by the electric field vector lines. The electric field vector lines for a on device are shown in the figure (Vgs =0.8V and Vds=0.8V).

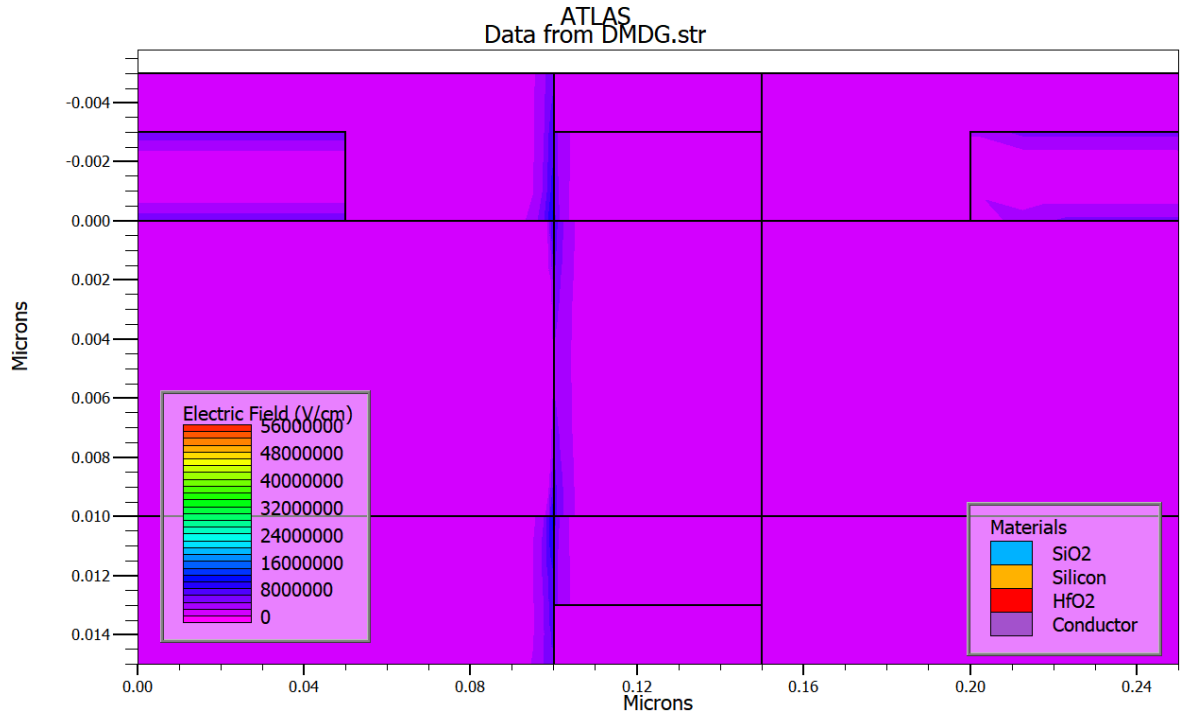


Figure. - Electric Field

As we can see, the electric field lines show the route that electrons can take to travel from source to channel. Point tunnelling from source to channel under the gate region is a possibility due to the densely populated lines towards the boundaries.

Please take note that the drain electrodes are hidden in all of the constructions since the meshing around those areas requires the drain electrode sizes to be kept at 0.

Electric Field Variations

Figure illustrates the size of the electric field fluctuation along the line while the device is ON (Vgs = 0.8 V and Vds = 0.8 V). We can observe that the electric field only exists at the channel in order to facilitate the tunnelling of electrons from the source to the channel.

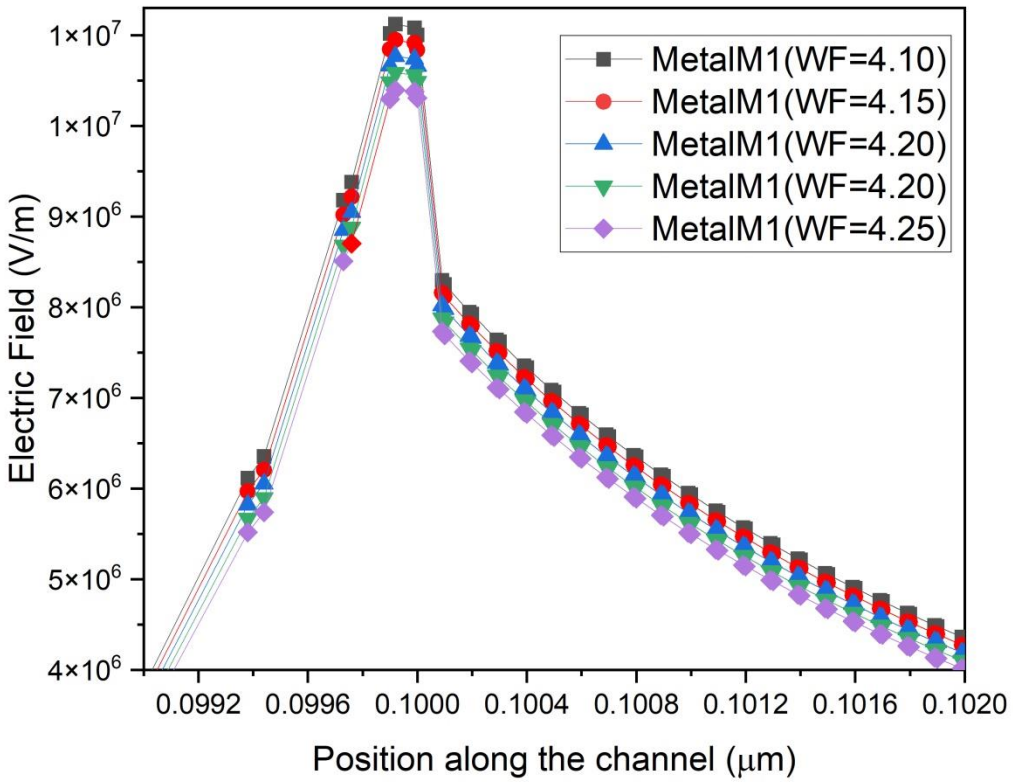


Figure : Electric Field Variation with different work functions at gate oxide width of 2nm.

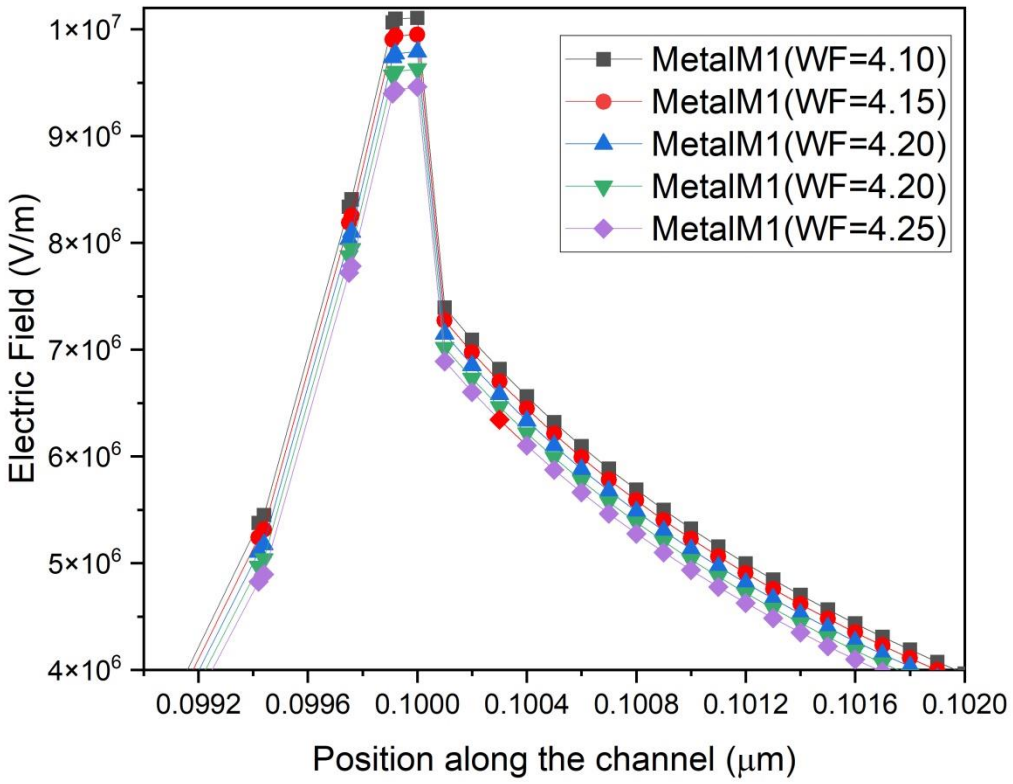


Figure : Electric Field Variation with different work functions at gate oxide width of 3nm.

Electron Concentration Variations :

Figures 1 and 2 depict the electron concentration for the device at ON (Vgs = 0.8 V and Vds = 0.8 V) and OFF (Vgs = 0 V and Vds = 0.8 V).

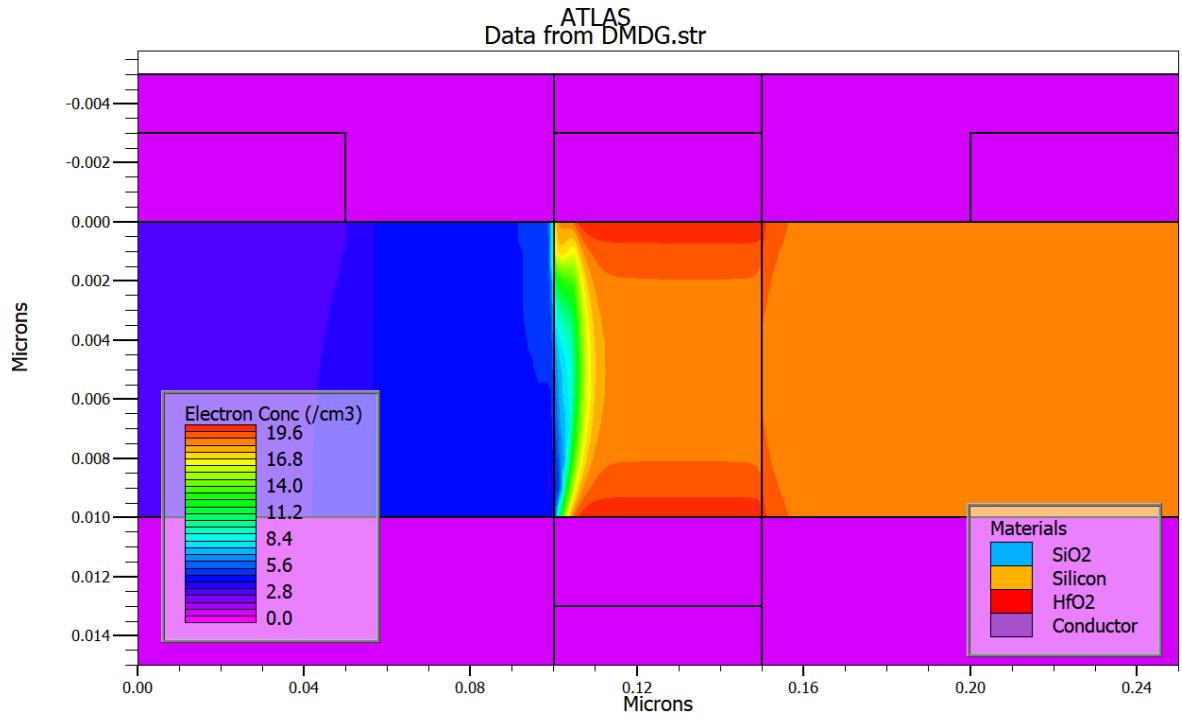


Figure : Electron Concentration when DG TFET is ON.

Potential Variations :

The potential variation near the gate oxide - channel interface is shown in Figure

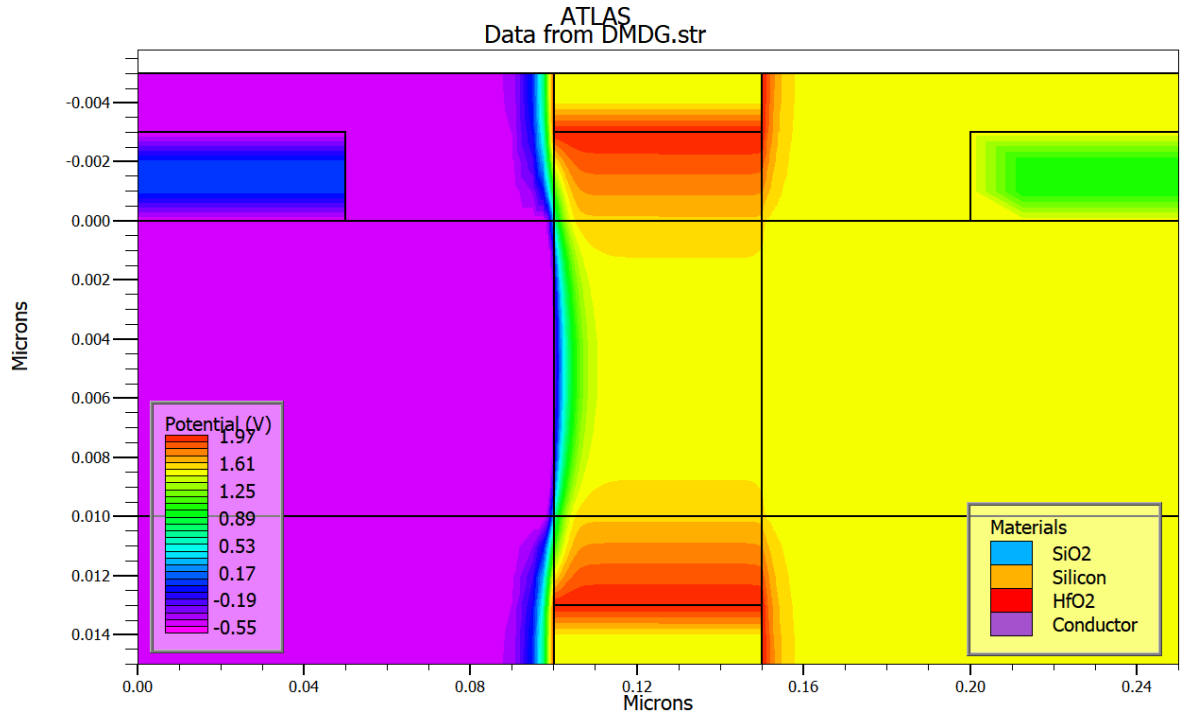


Figure : Potential Variations

Energy band diagrams :

The energy band diagrams for different work functions is shown in Figure

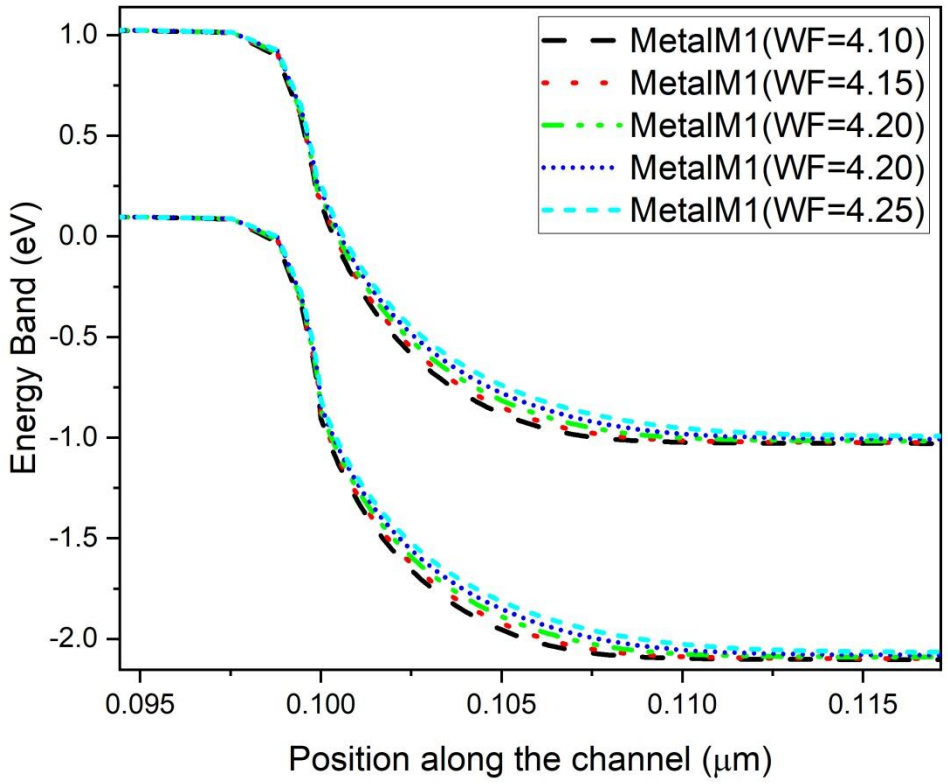


Figure : Energy Band Diagram

The graph clearly shows that when the Conduction Band (channel) and Valence Band overlap more, the risk of tunnelling increases (source). In order for electrons to tunnel from source to channel,

Tunneling :

Both point and line tunnelling are visible on DG-TFET. It is seen from Figure 1, which depicts hole tunnelling. Figure 2 depicts the DG-electron TFET's tunnelling.

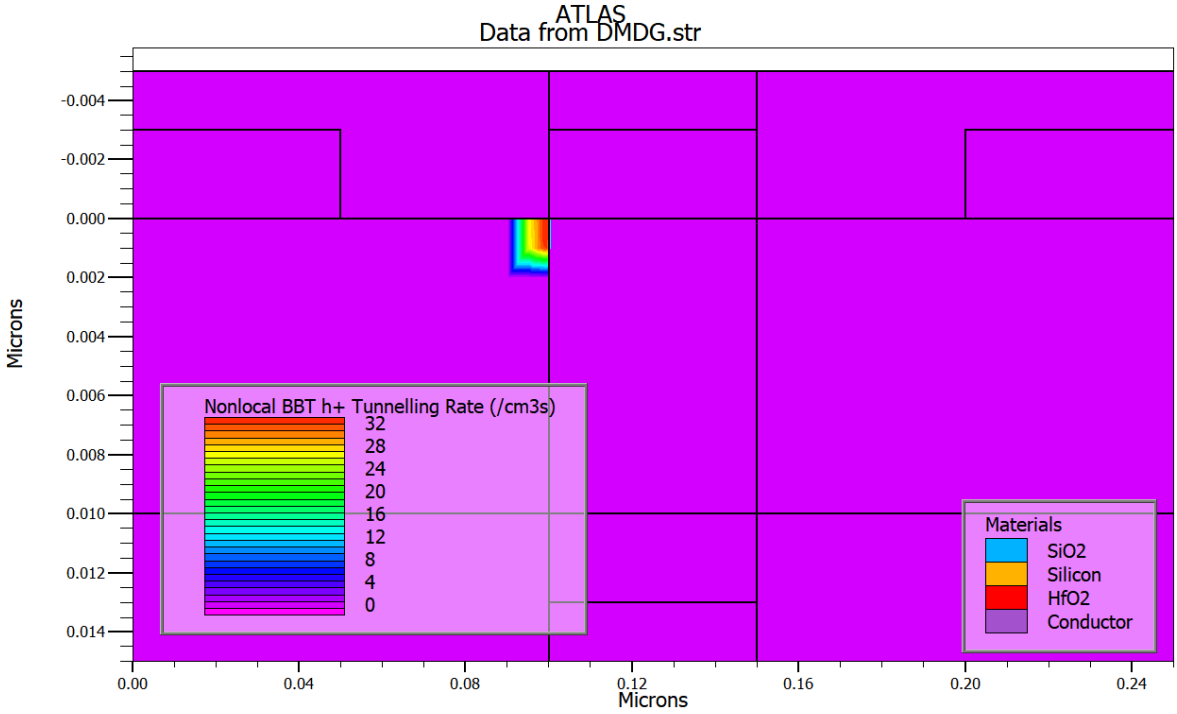


Figure 1: Hole Tunneling in Double Gate TFET

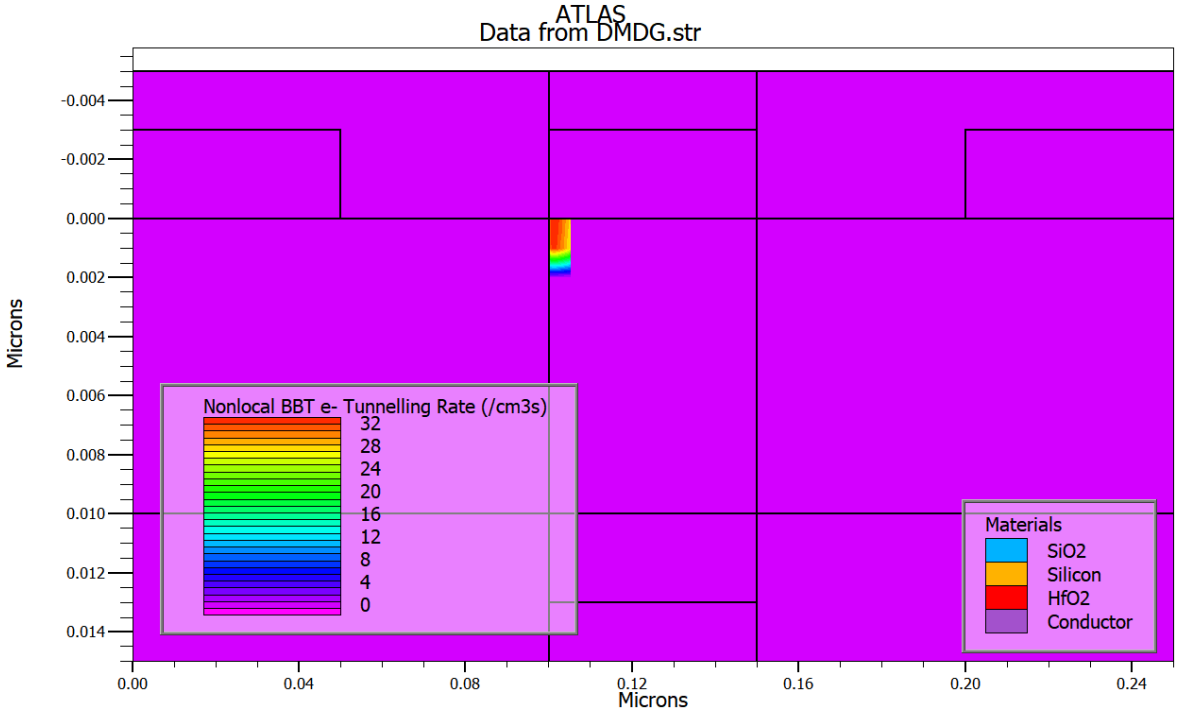


Figure 2 : Electron Tunneling in DG TFET

Subthreshold Swing :

The parameter where TFETs outperform MOSFETs is this one. In ideal circumstances, MOSFET SSs are restricted to 60 mV/decade. Nearly 90 mV/decade is the value for planar structures. Additionally, the value for devices like FinFETs might be closer to but still higher than 60 mV/decade. TFETs are capable of having far lower subthreshold slopes than MOSFETs. The device may transition from ON to OFF and vice versa faster if it has a low subthreshold swing because it can have a lower Ioff.

The Silvaco TCAD ATLAS tool's device extract command is listed below:

extract name = "ss" 1.0/slope(maxslope(curve(v."gate",log10(abs(i."drain")))))

Through simulation, we were able to arrive at the SS value of 17.55 mV/decade. The threshold voltage, which is the topic of our chapter's next part, can be used to justify this value.

Threshold Voltage :

Threshold voltage of a TFET s de ned as the V_{gs} value which when applied marks the onset of tunneling in the TFET, i.e the Conduction band of the channel and the Valence band of the source has aligned themselves.

To finnd out the threshold value for our proposed DG-TFET, we have used this device extract command in the Silvaco TCAD ATLAS tool :

extract name = "vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))

- abs(ave(v."drain"))/2.0)

Figure shows the onset of tunneling at $V_{gs} = V_T$. We have achieved a V_T of 360 mV at 2nm. This Figure shows the variation of Threshold Voltage with different Gate Metal Work Function.

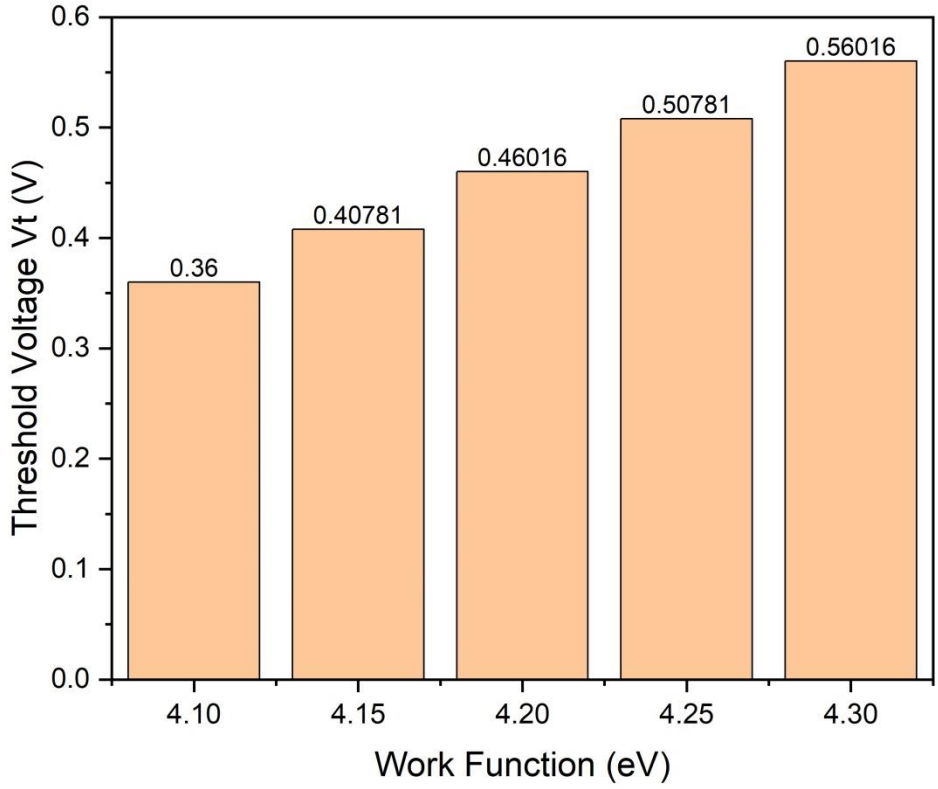


Figure : Threshold Voltage Variation with different Gate Metal Work Function at Gate Oxide width of 2nm.

Tunneling Rate :

Fig shows the Non Local Band to Band tunneling rate of Hole as well as electron.

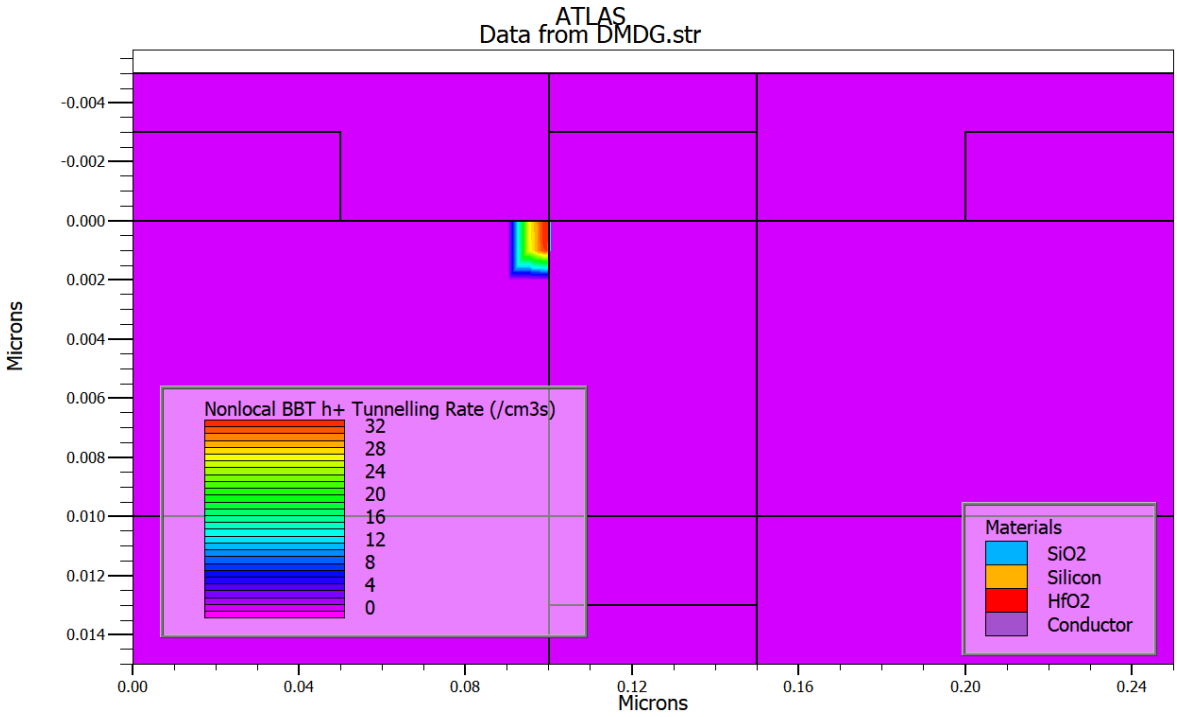


Figure : Non-Local Band to Band Tunneling of Hole.

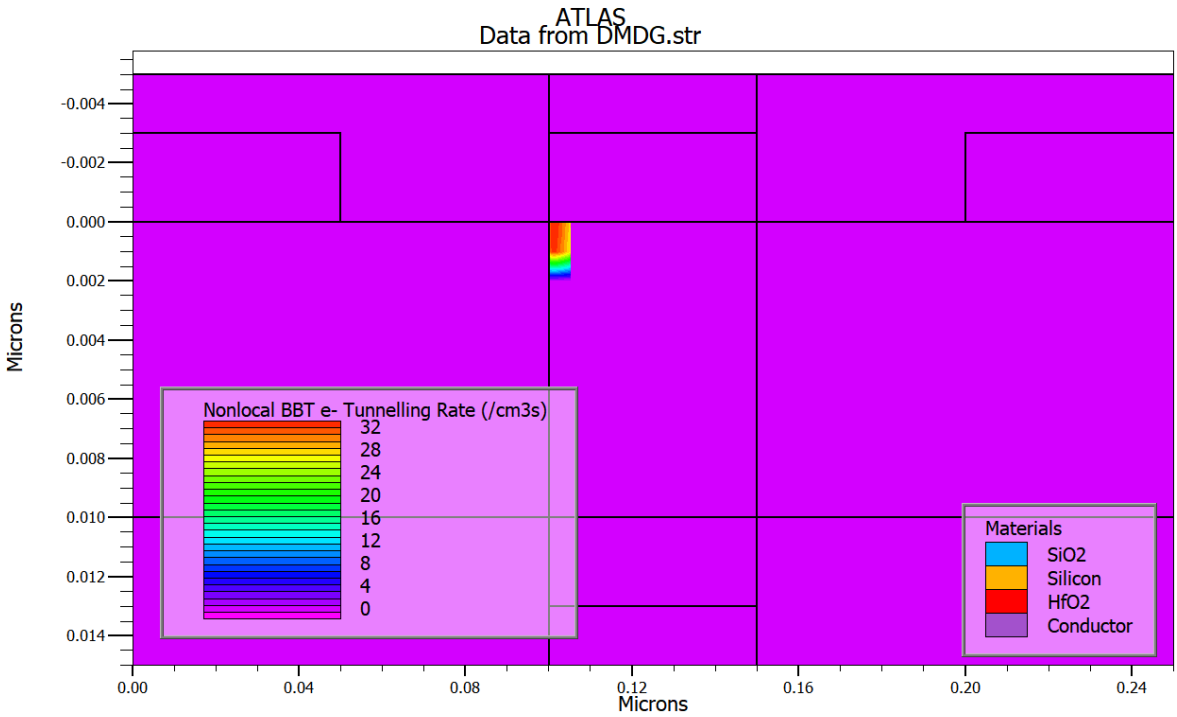


Figure : Non Local Band to Band Tunneling of Electron.

ON Current and I_{ON} /I_{OFF}

Figure shows the variation of ON Current and I_{ON} /$I_{OF\ F}$ with different Gate Metal Work Function at Gate Oxide Width of 3nm.

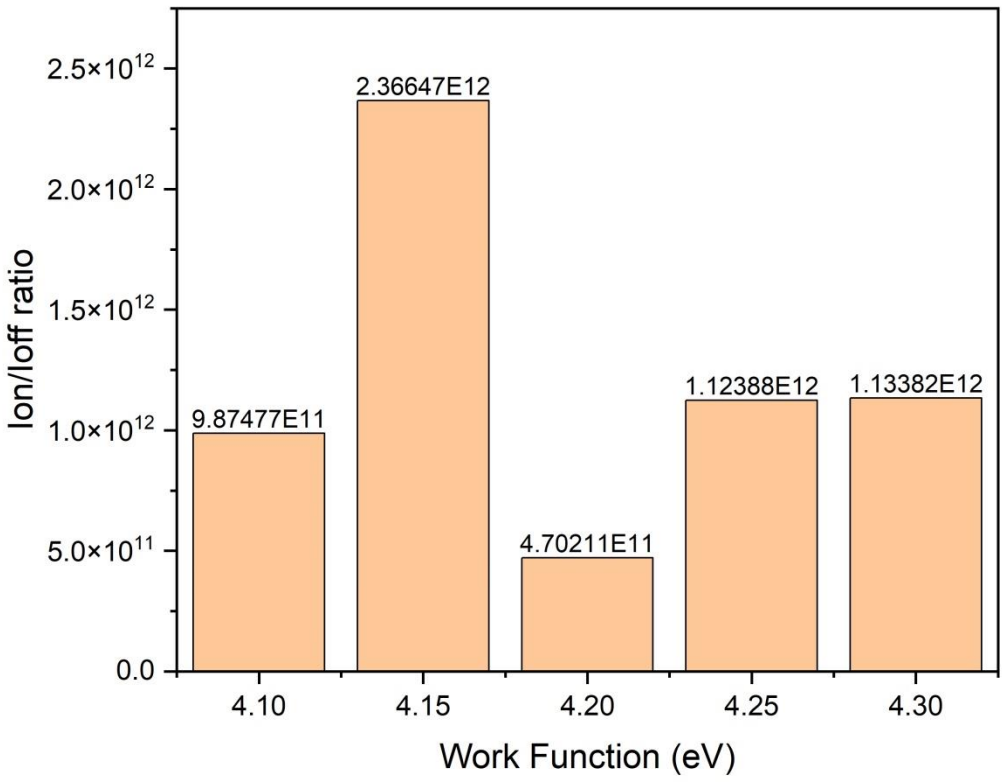


Figure : Ion/Ioff ratio Variation with different Gate Metal Work Function at Gate Oxide width of 3nm.

Conclusion

This chapter provided details of DG-TFET working and the simulation results obtained. Also the simulation results are being justified along with optimization of the Gate Metal Work Function height. We also discussed the necessity of incorporating double-gate in our structure and how it helps improving the device performance.

Chapter 6

Analog/RF Performance of DG-TFET

In this chapter, we have presented the analysis of Analog/RF performance of the proposed TFET structure. We simulated the transconductance, g_m.

Introduction

Transconductance (or transfer conductance), also known as mutual conductance, is the electrical property relating the output current to the input voltage applied.

Transconductance of DG-TFET

Figure shows the variation of g_m with V_{gs} for various Gate Metal ork Function for the DG-TFET. It is evident from the plot that the proposed DG-TFET exhibits greater g_m at a gate metal work function of 2nm.

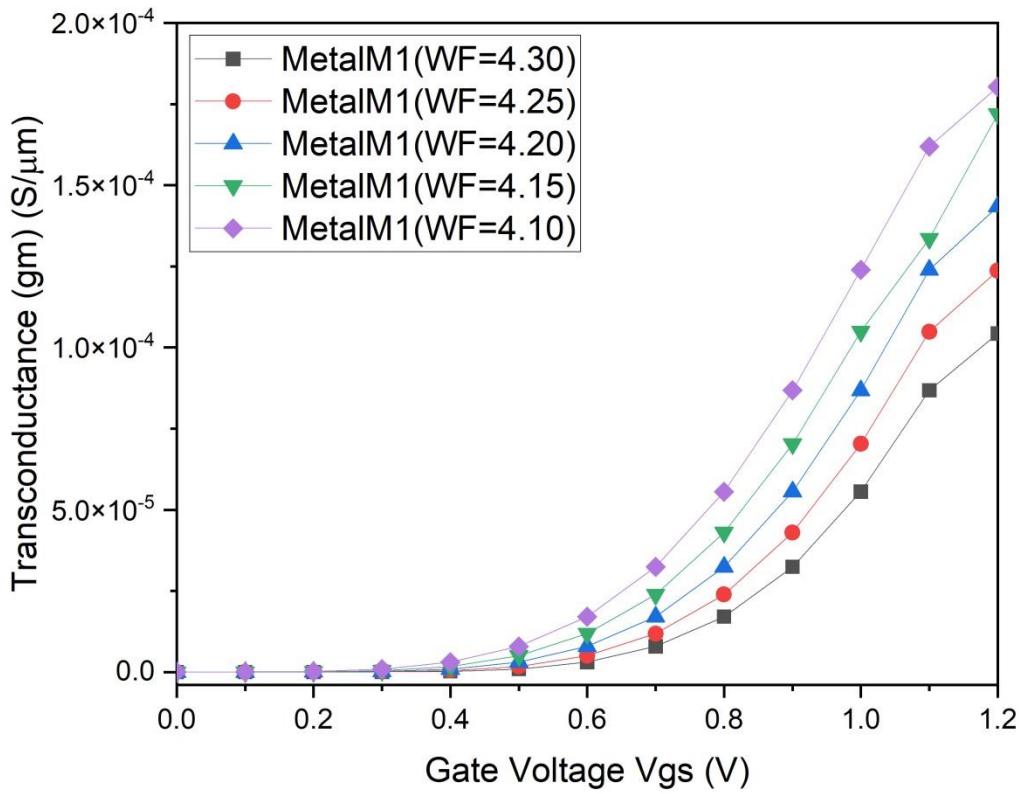


Figure: g_m vs V_{gs} for various gate metal work function.

The DG-TFET attains a maximum value of g_m, which is significantly higher than the reported TFETs in the past.

Capacitances of DG-TFET:

The higher frequency response of the device is affected by its g_m and the total capacitance (C_{gg}). For TFET, the capacitances are quite different than MOSFET due to presence of Band to Band tunneling at the source-channel junction in the TFET.

The C_{gg} is a sum of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}).

Figure depicts the dependence of C_{gg},C_{gs} and C_{gd} on V_{gs} for the DG-TFET.

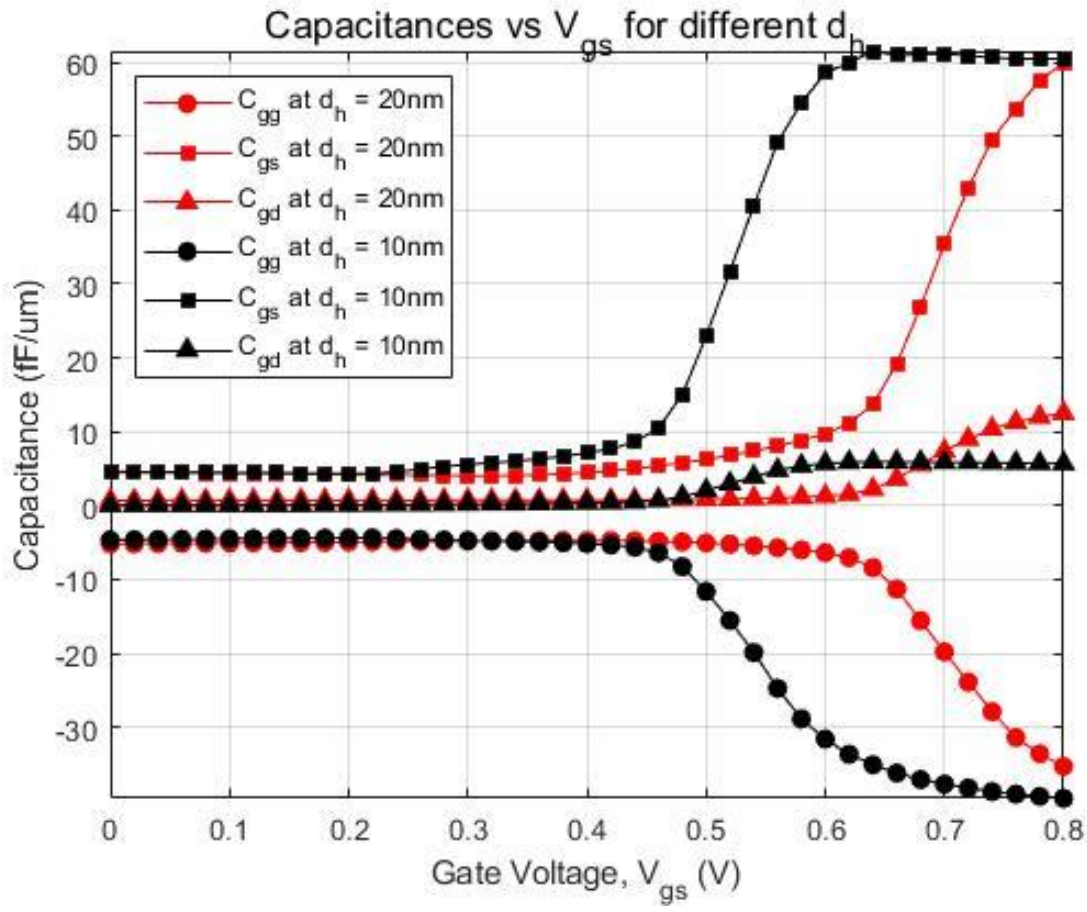


Figure. - C_{gg}, C_{gs} and C_{gd} vs V_{gs}

Unity Gain Bandwidth Product of DG-TFET

The cut-off frequency (f_T) and the gain bandwidth product (GBP) are crucial parameters to evaluate the analog/RF performance of the DG-TFET. For high-frequency circuits, f_T and GBP the higher the better so that the device can be used for numerous applications. The f_T of the device is dependent on g_m and C_{gg}, whereas GBP is measured at a fixed gain of 10 using the expression GBP = $g_m/(2\ 10C_{gd})$. The variation of f_T and GBP vs V_gs is plotted in Figure at optimum drain height, d_h (20 nm).

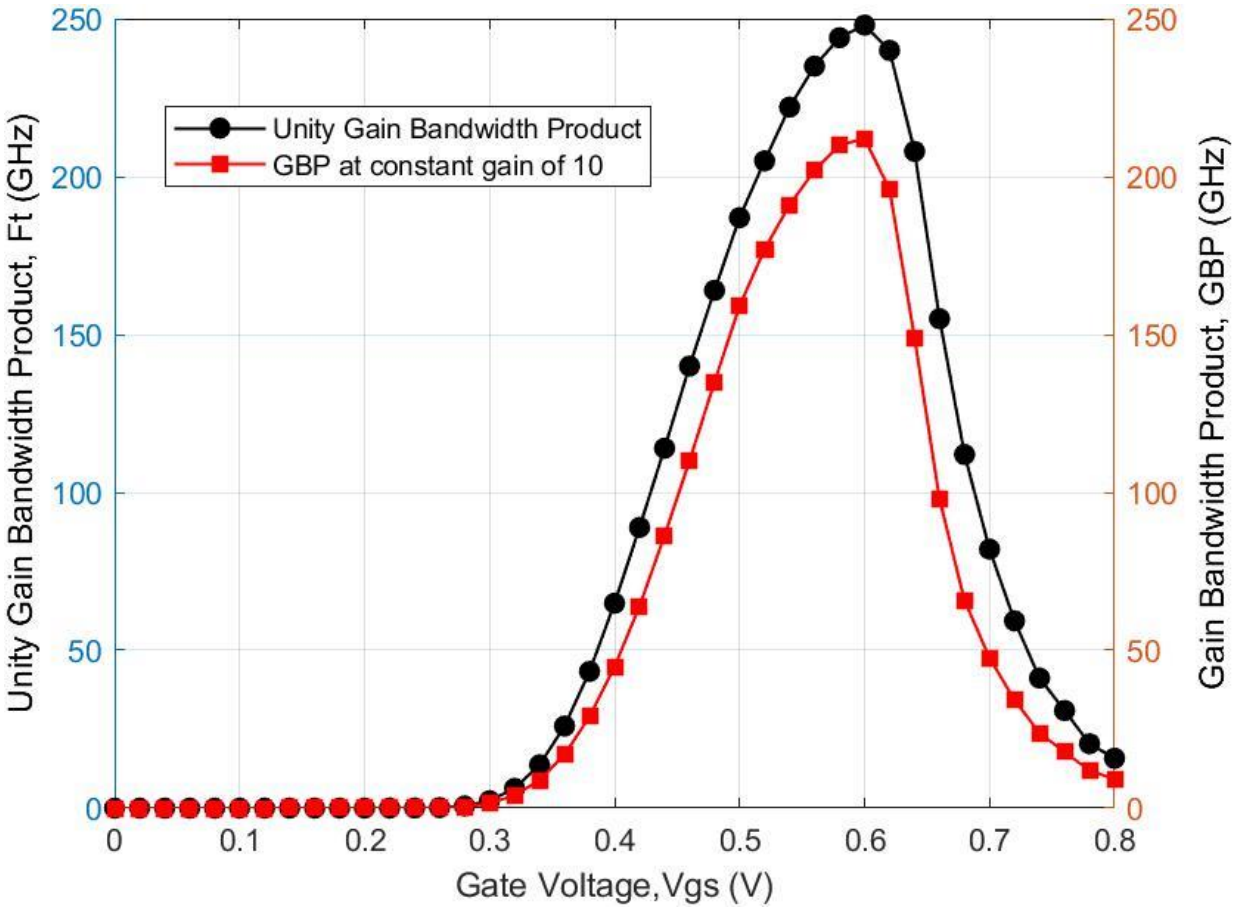


Figure - Variation of f_T and GBP with V_{gs} for d_h = 20 nm

It is quite evident from the Figure shows that f_T increases up to V_{gs} = 0.6 V due to the rapid increase in g_m. The proposed structure achieves a maximum f_T of 248 GHz. Similarly, the GBP of the proposed device reaches its peak value (212 GHz) at V_{gs} = 0.6V

Figure shows the impact of d_h on g_m and f_T of the DG-TFET. It is observed that both g_m and f_T increase gradually with the increase in d_h until 20 nm and then f_T degrade thereafter. Thus, from the analog/RF analysis, it is evident that DG-TFET provides optimum performance at d_h at 20 nm.

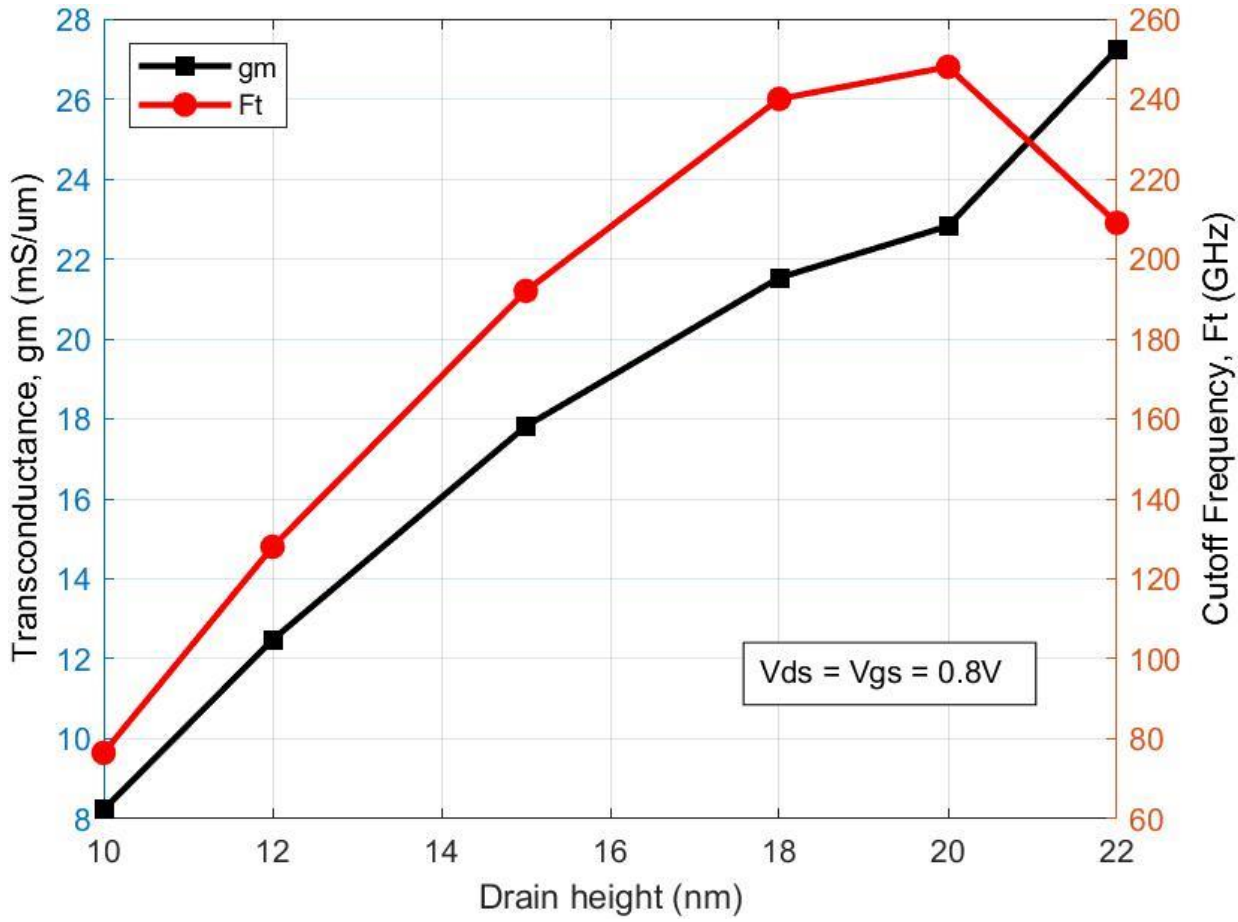


Figure. - Impact of d_h on g_m and f_T of the DG-TFET

Transfer Characacteristics of Double Gate TFET :

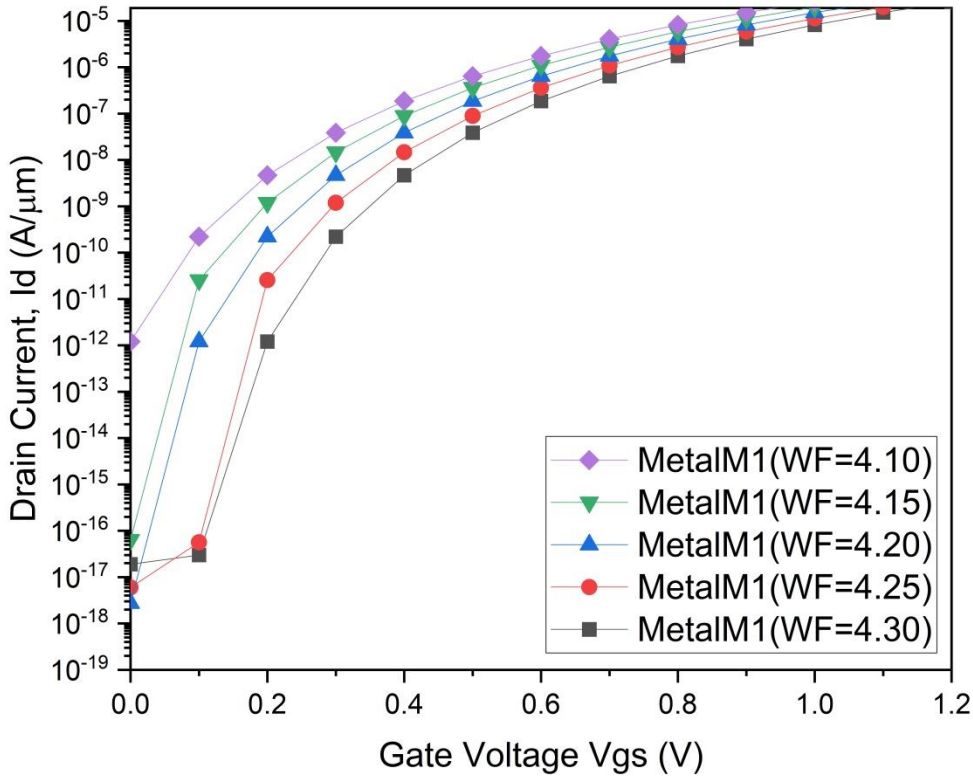


Figure : I_D vs V_{GS} of DG-TFET at different Gate Metal Work Function

Conclusion

In this chapter, we have depicted the analog/RF performance of the proposed DG-TFET. We have shown that our proposed DG-TFET has nearly 100 times better g_m than the recently reported TFET . Also, the cut-off frequency, f_T has seen a 6 times increase. Therefore, the DG-TFET is a better candidate for low-power switching as well as analog/RF applications.

Conclusion and Future Work

Conclusion :

In this thesis, we have proposed a structure engineered Double Gate (DG) TFET which was simulated in Silvaco TCAD 2D Atlas tool. We have also reasoned the factors

influencing its high I_{ON} /$I_{OF\ F}$ ratio. Our proposed DG-TFET has a very low subthreshold swing, SS_p and threshold voltage, V_T in comparison to its recent counterparts. It also has high analog/RF characteristics which makes this device viable for analog/RF applications. We have also paved a pathway to implement basic circuits using this device and used a lookup table approach to model it's characteristics. This model though not analytical but provides nearly accurate results through simulation.

Future Possibilities :

Coming to the end of our work, still there are some areas unexplored. In the near future, We can decrease gate oxide width thickness i.e 1 nm (because in our propose structure, we shows the variations of gate metal work function for different parameters considered of gate oxide width thickness at 2nm and 3nm). The ambipolar current of DG-TFET can be improved to an extent. The analytical analysis can be achieved to explore its credibility and a compact model can be developed.

Evolution of microelectronics industry to keep pace with the growing demands of technology driven modern society unlocks several opportunities for upgrading the existing systems. The outcomes of the present research dissertation also show that there still exists room for improvement and possible extensions can be aimed as future work.

The following points indicate few such areas where future research endeavors can be recommended:

1. Quantum mechanical effects can be incorporated while developing the analytical modeling of different reformed field effect transistors. From the basic principles of quantum theory, when the linear dimensions of the device are comparable to wavelength of carriers, quantum theories are required to be implemented. It has

also been reported that when channel length shrinks to 5nm and channel thickness is scaled below 10nm, quantum mechanical phenomenon cannot be ignored. Thus, for the aforementioned device dimension when significant deviation from classical physics is observed in the behavior of the device, quantum confinement effect is to be considered for accurate analysis of the device characteristics and quantum correction model is also to be included in device simulation framework for subsequent corroboration of analytical results

with simulated data. In addition, for more accurate modeling, 2D Schrodinger equation can be used instead of 1D equation.

2. For computational brevity, scattering effects are not considered in any of the analytical approaches described in preceding chapters. However, backscattering, inter sub-band scattering effect can be incorporated for more precise results. Reliabilty issues including self heating effect and hot carrier injection degradation affecting carrier and lattice heating can also be investigated to analysis the performance of such ultra-scaled devices for low power applications.

3. For each of the proposed structures, simulation based digital performance evaluation can be analyzed based on their capacitive behavior and transient response. A compact model can be developed implying hardware descriptive language (e.g. Verilog A) which can be implemented in designing basic circuits in SPICE tool and can be utilized for estimating the performance of the proposed device based circuits (in terms of propagation delay, peak overshoot voltage and power dissipation) to ensure the device reliability in future era low power VLSI circuits, which is the ultimate aim of device research.

4. An improved version of small signal model of proposed TFET structures can be developed by incorporating parasitic elements for high frequency operation of the devices. The high frequency operation introduces several spurious elements and their impact on matching network is significant and cannot be ignored. As determination of different scattering parameters is often used to characterize the device and its power gains, their variation with frequency for different parasitic elements and subsequent investigation of the stability factors can be some possible extension of the present work.

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