M.TECH. VLSI AND MICRO ELECTRONICS
SECOND YEAR, SECOND SEMESTER EXAM 2024
VLSI ARCHITECTURE AND SYSTEM DESIGN

Full Marks : 100 Time : 3 Hrs

Answer any 5 questions. Make and state all the assumptions (wherever made).
ALL PARTS OF A QUESTION SHOULD BE ANSWERED TOGETHER

(Q1) (a) A program runs in 10 seconds on computer A, which has a 2 GHz clock. It is required to design a computer B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? [5]

(b) State Amdahl and Little's Law. State where it is used [5]

(c) What is the propoed Von Neumann ISA architecture for the design of a processor? Explain the parts in short [10]

(Q2) (a) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. $[3 + 3 + 4 = 10]$

i. Which processor has the highest performance expressed in instructions per second?

ii. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

iii. We are trying to reduce the execution time by 30%, but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

(b) What is the instruction cycle in a RISC architecture? How is it implemented in a pipeline architecture. [10]

(Q3) (a) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. $[5 + 5 + 5 = 15]$

i. What is the maximum directly addressable memory capacity (in bytes)?

ii. Discuss the impact on the system speed if the microprocessor bus has:

A. 32-bit local address bus and a 16-bit local data bus, or

B. 16-bit local address bus and a 16-bit local data bus.

iii. How many bits are needed for the program counter and the instruction register?

(b) What are zero, one, two and three adressing schemes. Give examples. [5]

(Q4) (a) A two-word instruction is stored in memory at an address designated by the symbol W. The address ield of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at the effective address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is (a) direct; (b) indirect; (c) relative; (d) indexed. $[5 + 5 + 5 = 15]$

(b) Suppose a stack is to be used by the processor to manage procedure calls and returns. Can the program counter be eliminated by using the top of the stack as a program counter? Explain [5]

(Q5) (a) An instruction is stored at location 550 with its address ield at location 551. The address ield has the value 2410. A processor register R1 contains the number 2310. Evaluate the effective address if the addressing mode (a) direct; (b) immediate; (c) relative; (d) indexed with R1 as the index register. [10]

(b) A computer responds to an interrupt request signal by pushing onto the stack contents of the PC and the current PSR. The computer then reads new PSR contents from memory from the location given by the interrupt vector address (IVAD). The irst address of the service program is taken from memory at location IVAD + 1. [5 + 5 = 10]

i. List the sequence of microoperations implementing the interrupt.

ii. List the sequence of microoperations implementing the return from interrupt.

(Q6) (a) A program consisting of a sequence of ten instructions without branch or jump instructions is to be executed in an 8-stage pipelined RISC computer with a clock period of 0.5 ns. Determine (a) the latency time for the pipeline, (b) the maximum throughput for the pipeline, and (c) the time required for executing the program. [9]

(b) Assume an instruction set that uses a fixed 16-bit instruction length. Operand specfiers are 6 bits in length. There are K two-operand instructions and L zero-operand instructions. What is the maximum number of one-operand instructions that can be supported? [5]

(c) How many times does the processor need to refer to memory when it fetches and executes an indirect-address-mode instruction if the instruction is (a) a computation requiring a single operand; (b) a branch? [6]

(Q7) Write Short Notes on any 2 [10 × 2 = 20]

(a) Basic Measures of Computer Performance

(b) Processor organization.

(c) Differences between RISC and CISC addressing architectures

(d) Advantages and disadvantages of using a variable-length instruction format