

M.Tech. (VLSI and Microelectronics) 2<sup>nd</sup> YEAR EXAMINATION, 2024  
( 2<sup>nd</sup> Semester )

EMI/EMC AND SYSTEM TESTING AND TESTABLE DESIGN

Use separate answer scripts for each part.

Time: Three hours

Full Marks 100

PART I

No. of  
questions

Answer Q. no. 1 and any *tree* questions.  
Values of physical constants may be assumed, if necessary.

1. Choose the correct alternative in each case.
  - (a) Wavelength is inversely proportional to
    - i) Frequency
    - ii) velocity
    - iii) power loss
    - iv) attenuation constant
  - (b) A random process can be associated with
    - i) only discrete random variables
    - ii) only continuous random variables
    - iii) either only discrete or only continuous random variables
    - iv) both discrete and only continuous random variables simultaneously
  - (c) SAR stands for
    - i) Specific Absorption Rate
    - ii) Specific Attenuation Rate
    - iii) Special Absorption Rate
    - iv) Spectral Attenuation Rate
  - (d) Proper grounding may reduce
    - i) conducted emission
    - ii) radiated emission
    - iii) all sorts of emission
    - iv) none of the above
  - (e) An antenna is a
    - i) transducer
    - ii) transformer
    - iii) randomizer
    - iv) all of the above
  - (f) An event that is likely to cause tremendous amount of EMI is
    - i) lightning
    - ii) warfare
    - iii) construction
    - iv) all of the above
  - (g) As regards EMI, an antenna can act
    - i) only as emitter
    - ii) only as susceptor
    - iii) both as emitter and susceptor
    - iv) none of the above

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[ Turn over

2. Prove that for a real signal in time domain, the magnitude spectrum is an even function of frequency and phase constant of frequency. 12
3. If  $f(t) \leftrightarrow F(\omega)$ , evaluate the Fourier transforms of
  - (a)  $df/dt$  6
  - (b)  $f(t-at)$  for any real value of 'a' 6
4. Find the Fourier series for a rectangular pulse train of amplitude 'A', pulse width ' $\tau$ ' and time period 'T' 12
6. Consider a transmission line to which a 20V ideal battery is connected at  $t=0$  at the source end. The line has a total length of 400m, velocity of propagation  $200\text{m}/\mu\text{s}$  and characteristic impedance  $50\Omega$ . It is terminated in a  $100\Omega$  resistor. Plot the received voltage against time from 0 to  $12\mu\text{s}$ . 12
7. Write a note on EMC standards in vogue. 12

## M.TECH. VLSI AND MICROELECTRONICS SECOND YEAR SECOND SEMESTER EXAM.-2024

## EMC/EMI &amp; SYSTEM TESTING &amp; TESTABLE DESIGN

( 50 Marks for each Part)

TIME: THREE HOURS

Use separate answer script for each Part

FULL MARKS: 100

## Part – II ( 50 Marks)

*Answer any five questions. Each question carries equal marks. Answers must be brief and to the point. Answer to one question should be at one place.*

1. What are the basic purposes of testing? Discuss the basic principle of testing of a digital integrated circuit.
2. With the help of a flow chart explain where testing process is carried out in traditional digital VLSI design cycle. What are the limitations of the traditional design flow? Explain how the testing process gained interest in the new VLSI design flow.
3. (a) Define (i) fault coverage, (ii) process yield and (iii) defect level in the context of VLSI testing.  
(b) Classify faults according to the way they manifest themselves in time.
4. (a) Define behavioral fault model. Discuss how a statement 'if (Y) then {B1} else {B2}' can fail.  
(b) Define functional fault model. Derive the possible functional fault model for a 2-to-1 multiplexer circuit.
5. What do you mean by fault model? Explain with the help of proper circuit diagrams, the concept of stuck-open and stuck-on fault model? For a 2 input NAND gate, show that logic monitoring technique is not enough to detect all single stuck-on faults. What other method is required therefore?
6. Consider the circuit shown in Figure 1. Show that the faults 'c' s-a-1 and 'f' s-a-1 are equivalent.

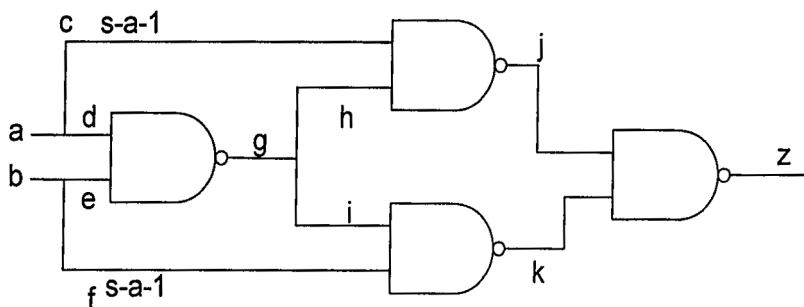


Figure 1:

7. What is meant by ATPG? Discuss the ATPG principle. Find out the test vector for the following circuit with the marked single stuck-at-fault in the circuit.

