Ref. No.: Ex/MECE-635/2024

M.Tech. VLSI Design & Micro Tech. Examination, 2024

(2nd Year, 1st Semester)

Subject : **Algorithms for VLSI Physical Design**

Time: 3 Hours | Full Marks: 100

Answer any ten questions **[10×10]**

1. State the boundary conditions of floorplanning. How overlapping and routability constraints affect floorplanning? Which algorithm tends to determine optimum floorplanning area? Discuss it briefly.

[4+3+3]

2. What are the design criteria for routing? Differentiate between global and local routing. When a problem will be called (i) NP complete, (ii) NP hard? Differentiate between them.

[4+3+3]

3. State the features of spanning tree algorithm. Classify it. How Kruskal's algorithm is different from shortest path algorithm? State the features of Steiner's algorithm.

[4+2+4]

4. State the different types of partitioning and discuss briefly each type. Mention the critical parameters related with partitioning. Name the different classes of partitioning algorithms.

[4+4+2]

5. Briefly describe the Y-Chart in context of VLSI Design flow. Mention the major objectives of portioning and placement in connection with VLSI Design flow.

[6+4]

6. Define grid based routing. What are the key constraints of grid based routing? Mention the different design styles of detailed routing.

[2+3+5]

7. [a] Discuss Lee's algorithm with proper diagram. How Soukup's algorithm is different from it?
[b] What is Detour's number? Explain Hadlock's algorithm in connection with detour's number.

[5+5]

8. State the criteria on which quality of placement depends. How simulated annealing is applied to placement? How simulated evolution is different from it?

[2+4+4]

9. What are the differences between comparability, co-comparability and triangulated classes of graph? What are the types of graph algorithm connected with a given floorplanning area? Discuss any one type with example.

[5+2+3]

10. Briefly discuss the operations required in generalized VLSI algorithm in connection with floorplanning. How could you determine that a given block is inside the floorplan area?

[8+2]

[Turn over

11. What are the major VLSI Design steps? State the characteristics of partitioning and floorplanning in connection with it. How global routing is differentiated with detailed routing?

[2+6+2]

12. What is clock routing? State the different delay criteria for clock routing. Calculate the total time delay for unbuffered tree in connection with clock routing.

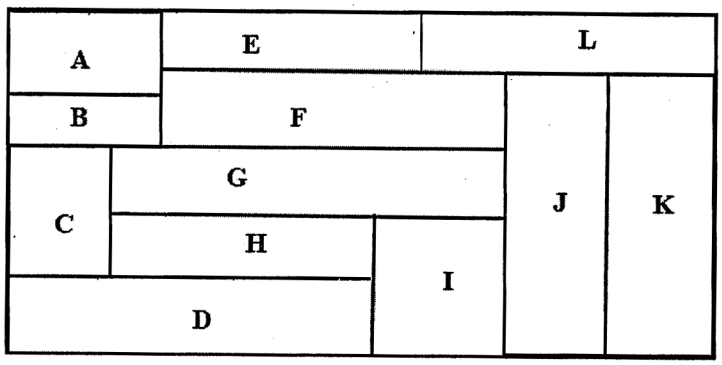
[2+3+5]

13. [a] What are the optimization criteria for floorplanning? Mention the different problems associated with optimization.

[b] Mention two different styles of pin assignment.

[3+4+3]

14. What do you mean by non-sliceable floorplanning? Draw the tree diagram for the flowing floorplanning:



15. [a] State two methods by which length of a graph can be evaluated. Mention the procedure for any of the case.

[b] Briefly discuss the timing driven floorplanning algorithm.

[2+4+4]

16. [a] Define channel routing. What is the objective of it?

[b] Define channel length and channel height. Mention the parameters related with channel routing problems.

[2+2+2+4]