M.TECH. VLSI AND MICRO-ELECTRONICS
FIRST YEAR FIRST SEMESTER EXAMINATION-2024

VLSI FABRICATION TECHNOLOGY

Full Marks: 100 **Time: 3 hours**

Answer **Q.1 (*compulsory*)** and any ***four*** from the rest

(All parts of a question should be answered at a place)

Q.1 **Answer the following questions (*Any ten*)** **2x10**

(a) What is Moore's law in VLSI?
(b) What is the importance of cleanroom in Semiconductor industry?
(c) What is Seed crystal?
(d) Differentiate between Gate oxide and field oxide.
(e) Mention one merit and demerit of dry oxidation.
(f) Draw the typical doping profiles obtained from thermal diffusion and ion implantation.
(g) Write the unit of linear rate and parabolic rate constants of Deal-Grove model.
(h) Name two advanced lithography techniques.
(i) Define resolution and throughput with regard to photolithography.
(j) Differentiate between wet and dry etching.
(k) What is proximity effect in electron beam lithography?
(l) What is the advantage of using doped Polysilicon gate instead of metal gate?
(m) What is electromigration?

Q.2 (a) Define the following terms (i) Electronic Grade Silicon (ii) Segregation coefficient (iii) Frenkel defect **2+2+2**

(b) Explain the Czochralski technique for silicon crystal growth process. **8**

(c) A silicon ingot, which should contain 10^{16} Boron atoms/cm^3, is to be grown by the Czochralski technique. What concentration of Boron atoms should be in the melt to give the required concentration in the ingot? If the initial load of silicon in the crucible is 60 Kg, how many grams of Boron (atomic weight 10·8) should be added? The density of molten Silicon is 2·53 g/cm^3. Assume $k_0 = 0{\cdot}8$. **6**

Q.3 (a) Why the oxidation process is useful in IC fabrication technology? **3**

(b) Derive the Deal-Grove model of oxide growth kinetics. Explain why the oxide growth rate decreases with time. **8+2**

(c) Why dry-wet-dry oxidation technique is used to grow gate oxide of a MOSFET device? **3**

(d) Discuss the different oxide charges. **4**

Q.4	(a)	Discuss the mechanisms of thermal diffusion of dopant atoms in Silicon.	**6**
	(b)	Explain the temperature dependence of diffusion of dopants.	**4**
	(c)	What are the different types of diffusion profiles and discuss how to achieve these. What is diffusion length?	**4+2**
	(d)	Determine the diffusivity from a known impurity profile. Assume that a Boron is diffused into an n-type Si single-crystal substrate with a doping concentration of 10^{15} atom/cm^3. The diffusion profile can be described by Gaussion function for the diffusion time of 60 minutes, a junction depth of 2 μm and surface concentration of 10^{18}/cm^3.	**4**
Q.5	(a)	What is lithography? Compare positive photoresist and negative photoresist in terms of resolution.	**2+2**
	(b)	Discuss the electron beam lithography technique for patterning VLSI circuit.	**10**
	(c)	Why electron beam lithography is a "mask less" lithography technique?	**2**
	(d)	Discuss the merits and demerits of photolithography compared to electron beam lithography.	**4**
Q.6	(a)	Write down the properties of a photoresist.	**3**
	(b)	Mention the factors that affects the resolution of pattern in lithography process.	**3**
	(c)	Discuss the resolution enhancement technique using phase-shift mask.	**6**
	(d)	Discuss the "Lift-off" process using suitable diagrams.	**8**
Q.7	(a)	Compare conventional annealing and RTA.	**5**
	(b)	Show 44 nm of Silicon is consumed for 100 nm SiO_2 growth. Assume molecular weight of Si and SiO_2 are 28.90 gm/mol and 60.08 gm/mol respectively, and their densities are 2.33 gm/cm^3 and 2.21 gm/cm^3 respectively.	**5**
	(c)	Differentiate between raster scan and vector scan with regard to electron beam lithography.	**5**
	(d)	Write a short note on MBE (Molecular Beam Epitaxy).	**5**
Q.8	(a)	What are the advantages of BiCMOS Technology?	**3**
	(b)	Explain the process flow of STI (Shallow Trench Isolation) using suitable diagrams.	**7**
	(c)	Discuss the fabrication steps of n-MOSFET technology using suitable diagrams.	**10**