M. TECH. VLSI DESIGN AND MICROELECTRONICS
1ST YEAR 2ND SEM EXAM-2024
Low Power VLSI Design

Time: 3 hrs Full marks: 100

Answer any ten questions [10×10=100]

1. Why do power dissipation become an important issue in scaled down devices? List out the sources of power dissipation in VLSI circuits and explain them briefly. [4+6]

2. What is dynamic power dissipation? Derive the expression and explain each term. [2+8]

3. What do you mean by leakage power dissipation? Name various sources of leakage components and explain methods to reduce them. [3+7]

4. What is Glitching in static CMOS logic gates? Explain an example to minimize Glitching. [10]

5. Describe Medium cost BiCMOS process with neat sketch. [3+7]

6. Compare BiCMOS with CMOS process technology. Draw the circuit for BICMOS Darlington pair and explain its working. [6+4]

7. Define Peak Power, Average Power and energy related to VLSI circuits. Explain their importance in power dissipation. [10]

8. In Low-Power Gate-Level Design explain technology mapping and phase assignment to reduce power dissipation. [10]

9. Explain Pin-swapping, Pre-computation, clock gating and input gating to reduce power dissipation in Gate-Level Design. [3+7]

10. What do you mean by activity reduction in Algorithmic-Level Design. Explain with a 3 bit counter. [2+8]

11. Why do we need Power Gating? Explain fine and coarse-grained methods of power gating. Describe leakage power reduction through Power Gating in CMOS. [2+4+4]

12. Define signal probability and signal activity. Given signal probability of A is 0.2, B is 0.5, C is 0.3 and D is 0.4. Implement logic function (A+B). (C+B) using two input NAND and find the total signal probability. [4+3+3]

13. Write down the advantages of pseudo nMOS over static CMOS logic. Draw a 2 input NAND gate using Pseudo nMOS logic. [10]

14. Explain dynamic CMOS logic. [10]