M. Tech. VLSI and Micro Electronics Examination 2024
(1st Year, 2nd Semester)
Advanced Digital IC Design

Time: Three hours | Full Marks: 100

Answer any five questions
All questions carry equal marks
Answer all the parts of a question in the same place

1. a) Write the advantages of CMOS logic family.
   b) Draw a 2-input XOR gate using static CMOS logic and verify its truth table.
   c) Sketch the Voltage Transfer Characteristics (VTC) curve of a CMOS inverter and mention the operating regions of nMOS and pMOS transistors. Also explain it briefly.
   d) Write the merits and demerits of pseudo- nMOS logic. Implement the Boolean function F = (AB + AB'C)' using pseudo- nMOS logic.

   (3+6+6+5)

2. a) Draw a static CMOS inverter circuit and explain its operation briefly.
   b) Derive the expression of maximum input voltage which can be interpreted as logic "1" (V_{IH}), and minimum output voltage when the output level is logic "0" (V_{OL}) for a CMOS inverter.
   c) Describe noise margin and propagation delay for CMOS logic family.

   (5+10+5)

3. a) Write the advantages of complementary pass transistor logic. Design a 2-input XOR/XNOR gate using complementary pass transistor logic and explain its operation.
   b) Implement the Boolean function G (A, B, C) = AB + A'C' + AB'C using CMOS transmission gate.
   c) Draw a transistor-level circuit for a JK flip-flop and verify its truth table

   (8+4+8)

4. a) Draw a CMOS Schmitt trigger circuit and briefly explain its operation.
   b) Write the advantages of dynamic logic over static logic.
   c) Explain the cascading problem in dynamic CMOS logic.
   d) Sketch a general NORA CMOS logic circuit and explain its operation. How we can overcome the dynamic charge sharing problem in NORA CMOS logic?

   (7+3+3+7)

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5. a) What do you mean by gate level modeling of a digital circuit in Verilog? Write a gate level Verilog code for a 2-to-4-line decoder.
   b) Write the difference between reg and wire data types. Briefly explain the utility of blocking and non-blocking statements in Verilog.
   c) Write a behavioral Verilog code for a 4:1 MUX.
   d) Write the benefits of FPGA-based design. Also write a complete FPGA-based design flow.

(6+5+4+5)

6. a) Write the advantages and disadvantages of BiCMOS technology.
   b) Draw a general BiCMOS architecture to implement any complex binary logic.
   c) Sketch a transistor level circuit for a 2-input NAND gate using BiCMOS technology and briefly explain its operation.
   d) Write the applications of BiCMOS circuits.

(6+4+7+3)

7. a) What do you mean by flash memory? Why memory address decoders are required?
   b) Design a NOR based ROM array to store the following four 4-bit data.
      W1 = (0 0 1 1), W2 = (0 1 0 1), W3= (0 1 1 0) and W4 = (1 0 0 1)
   c) Draw a single transistor DRAM cell and explain its operation.
   d) Design a 2-to-4 MOS dynamic NOR decoder and use it to design a 4-input pass transistor based column decoder.

(4+6+4+6)