M. TECH. COMPUTER TECHNOLOGY 1ST YEAR 1ST SEMESTER EXAMINATION 2024

HIGH PERFORMANCE COMPUTER ARCHITECTURE

Time: Three Hours Full Marks: 100

Answer any ***four*** questions

[*All parts of a question must be answered together. If answered more than 4 questions, answers of only first 4 questions will be assessed*]

1. a) Define Moore's law. As observed by Moore's law, the number of transistors on a chip in 2025 should be how many times the number in 2015? 5+5

   b) Derive the equation for average memory access time with L1 and L2 caches. Suppose a new enhanced processor is 10 times faster on computation in an application than the original processor. Assuming that the original processor is busy with computation 40% of the time and waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement? 10+5

2. a) How is a block placed in a 4-way set associative L1 cache if the cache is empty? What are the *compulsory*, *capacity* and *conflict* misses? 5+5

   b) Discuss the methods for optimizing the cache performance by reducing the (i) *hit time* and *miss penalty*. 5+10

3. a) Discuss the methods of non-blocking and multi-banked caches for increasing cache bandwidth. 5+5

   b) Explain the mechanism with example for (i) *loop interchange* and (ii) *blocking* 8+7

4. a) What is instruction level parallelism? Discuss the different types of *data dependences* with examples. 5+15

   b) Discuss different types of *data hazards*. 5

5. a) What is *loop unrolling*? Discuss with an example. What are the limitations of *loop unrolling*? 5+5

   b) List all the dependences (output, anti and true) in the following code segment. Indicate the true dependences are loop-carried or not. Show why the loop is not parallel.

```
for (i=2; i < 100; i++) {
        a[i] = b[i] + a[i];       /* S1 */
        c[i-1] = a[i] + d[i];     /* S2 */
        a[i-1] = 2*b[i];          /* S3 */
        b[i+1] = 2*b[i];          /* S4 */
}
```

   15

6. a) Describe the basic vector architecture and its working principle. 10

   b) Write short notes on NVIDIA GPU memory structure. 10

   c) Give a solution to handle variable vector length 5