Ex/PG/PE/T/113B/2024

Jadavpur University

ME (Power Engineering) 1st Year Second Semester Examination, 2024

Digital Systems

Time: 3hrs **Full Marks 100**

Answer all Questions

1. With the help of an FSM design a 3 bit Synchronous Counter and represent its schematic

Or

Represent a Full Adder with Carry as a (i) Moore Machine and (ii) a Mealy Machine 20

2. Draw the schematic for a 555 timer based Astable Multi-vibrator and design the circuit components for the circuit to produce a square wave with a duty cycle of 0.7. 20

3. With the help of a neat schematic explain why a floating input in a TTL Totemplole circuit is considered high.

Or

With suitable assumptions, derive the (i) noise margin and (ii) fan-out for TTL family of logic circuits. Design a suitable circuit to interface an open collector TTL gate with a CMOS logic gate. 20

4. From first principles derive the Z transform of a Unit Ramp for a sample time of T_s. Is there a RoC for this-if so, derive the same. If this signal is delayed by N>0 samples, derive the corresponding Z transform.

Or

From first principles prove that $x[n] * h[n] = h[n] * x[n]$

Express the following difference equation in the form of a branch diagram and hence deduce the Z transfer function $\frac{y(z)}{x(z)}$:

$y[n] = a_1x[n] + a_2x[n-1] + a_3x[n-2] + a_4x[n-4]$ 20

5. Derive the Trigonometric Fourier Series for a Rectangular Pulse Train with Duty Cycle 0.5 and Time Period 2 secs. How does the amplitude spectrum change if the frequency is increased to 4 secs.

Or

State and prove the Sampling Theorem from first Principles 20