Ref. No.: Ex/PG/ETCE/T/112C/2024

Master of Engg. (Electronics & Tele-Comm. Engg.) Exam., 2024
(First Year, 1st Semester Exam. 2023-24 Session)

PROGRAMMABLE LOGIC CONTROLLER (CON)

Time: 3 Hours | Full Marks: 100

Answer All the **FIVE** Modules.
(All parts of the same question must be answered at one place only)

Module I (CO1)

1. (i) Write the Technical Definition of the term PLC as defined by National Electrical Manufacturers Association (NEMA)
(ii) List the specific Characteristic functions of PLC which makes it superior in modern industrial control and communication.
(iii) Draw the simplified Block Diagram of PLC, and List its basic sections with a short description.
(iv) Name the most critical component of the PLC, and provide the reasons for the same. [3+6+8+3]

Module II (CO2)

2. (i) Name the basic Program Format for a PLC, and List its basic Programming Rules.
(ii) A coal handling plant has three coal conveyors C1, C2, and C3. C1 is fed from the output of the Crusher, C2 is the mid-belt, and C3 pushes coal to the bunker. The following conditions are to be satisfied: C1 and C2 can be made ON, only when C3 is ON; C1 can be made ON, only when C2 and C3 are ON; C1 and C2 trip, when C3 trips; C1 trips when C2 trips, but C3 is ON, and C1 trips when C2 and C3 trip. Design a Logic Diagram to meet these conditions.
[5+15]

Module III (CO3)

3. (i) Draw the schematic diagram of a Function Bloc of a PLC Timer, and briefly explain the same.
(ii) Draw the Ladder diagram for the three motor system to meet the following conditions:
Motor 1 (M1) starts as soon as the start switch is ON; after 15 seconds, M1 will be OFF, and Motor 2 (M2) starts. After 10 seconds, M2 will be OFF, and M3 starts. After 15 seconds, M3 will be OFF, and M1 starts, and the Cycle is repeated. [5+15]

Module IV (CO4)

4. (a) (i) The number of available on-chip Ports, Timer / Counter, and the size of the Program Memory (PM), Data Memory (DM) in Intel 8051 Microcontroller Unit (MCU) are ____, _____, _____ and _____, respectively.
(ii) In the 8051 MCU Pin-out, the number of Pins which are dual in nature are _____
(iii) For the Intel 8052 MCU, the memory map of the upper RAM Block is _____, and this block can be accessed only by _____ addressing.
(iv) The Special Function Register (SFR) TCON is partly related to _____, and partly related to _____
(v) The SFR, TMOD register is bit addressable. (State True / False).

(b) List the MCS-51 MCU Bus Control Signals, and explain the same in brief.
(c) (i) Differentiate the Time and Counter Mode operation of 8051 MCU.
(ii) Explain the function of the Gate bit in the TMOD register.
(d) Illustrate the Auto-Reload Mode operation of 8051 MCU on-chip timer. [5+5+5+5]

Module V (CO5)

5. (a) (i) The D4, and D3 bits of PSW are 1,1 respectively. Identify the actual address of the on-chip RAM (Date Memory – DM) register – R7, which will be accessed during the execution of the instruction, MOV A,R7.

(ii) The range of Jump / offset corresponds to the relative addressing is _____

(iii) Let (DPTR) = 2000H. Identify the range of Program Memory – PM, that can be accessed using Indexed Addressing mode.

(iv) Let (A) = 5FH. After the execution of the instruction SWAP A, the content of the register, A = _____.

(v) The carry bit is 1, and the Port status bit P1.0 is reset. What will be the status of the carry bit, and P1.0, after executing the instruction, ANL C, /P1.0?

(b) (i) (DPTR) = 2050H. What will be the content of the DPTR, after executing the following instructions?

```
8000H : XCH A,DPL
        DEC A
        CJNE A,#0FFH, SKIP_DEC
        DEC DPH
SKIP_DEC:XCH A,DPL
```

(ii) In the third instruction, calculate the actual value / relative offset byte value to be substituted in place of the Label, SKIP_DEC.

(c) Write an 8051 Assembly Language Program (ALP) that takes the Character 'A', transmits it, delays for the transmission time, and returns to the calling program. Use Timer-1 to set the baud rate, which is 1200 baud.

[5+5+10]