M. E. ELECTRICAL ENGINEERING 1ST YEAR 2ND SEMESTER EXAMINATION, 2024
(2nd Semester)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEMS (MS)

Full Marks 100
(50 marks for each part)

Time: **Three hours**

No. of Questions	PART I	Marks
	Answer question 1 and any TWO from rest	
1.	Answer any **FIVE** of the following questions. For each of the questions, state clearly whether the statements are TRUE or FALSE. Justify in favour of your comment. a) It is economical to design Application Specific Instruction-set Processors (ASIPs) with Von Neumann architecture. b) In case instructions have insufficient parallelism, code density of VLIW processors may be high. c) The complexity of datapath is maximum for single purpose processors. d) Purpose of using cache memory is to enhance storage capacity for processors. e) For fast execution of Multiply and Accumulate (MAC) instructions General Purpose Processors (GPPs) are preferred. f) SRAM cell is used to implement One Time Programmable (OTP) switch. g) GPP is preferred over Single Purpose Processor (SPP) when NRE cost is low. h) An SPLD can be used to implement the model of a processor.	5x4 = 20
2.	a) What are the different types of IP core available in market? State them	7

	and present a comparative study.	
	b) What is a saturating arithmetic? What is the purpose for implementing this?	3
	c) In what ways are the SoC-based structures different from conventional IC-based structures?	5
3.	a) Explain with appropriate example the method of implementing a Boolean function using 'full-custom' technology.	8
	b) Draw the structure of a programmable AND-matrix and explain its working principle.	7
4.	a) What are the different types of programmable switches available? Explain their working principles and applications with appropriate diagram.	12
	b) What are the causes of failure of device fitting?	3
5.	a) State two methods for managing power dissipation employed in embedded systems. Explain them.	8
	b) Draw the generalized structure of a timer-counter combine. The timer or counter can work with or without terminal count. The timer can be used with or without a prescalar. Explain your solution.	7

Ref No: Ex/PG/EE/T/129B/2024

M.E. ELECTRICAL ENGINEERING (1ST YR 2ST SEMESTER) EXAMINATION, 2024

(1st / 2nd-Semester Supplementary)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEM

Full Marks 100

Time: ~~Two hours~~/Three hours/ ~~Four hours~~/ ~~Six hours~~ (50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART – II	Marks
1.	*Answer question:-1 and any two from the rest.* ***Answer any four:-*** a) Explain the steps of fabrication process using VLSI technology showing necessary diagrams. b) Explain how VTCMOS and MTCMOS transistor works. What advantages can be obtained. c) What are the different types of model for calculating gate delay of CMOS logic gates using parameters as (W/L) ratio, V_{DD}, V_{SS}, channel resistance R_P, R_N and load capacitance C_L d) Explain how cross talk can adverse effect on fabricated CMOS operating under AC condition. e) Discuss how speed-power product decides the operating frequency of CMOS gate. f) Explain the term i) Event driven simulation, ii) simulation time wheel.	**4X5=20**
2.	a) Distinguish between technology dependent and technology independent logic synthesis method. Which process is best suited for FPGA device to be customized. b) Explain the basic difference between SRAM based and CMOS logic gate based lookup table. c) What is meant by path delay and critical path delay. Give example.	**6+5+4**
3.	a) Analyze the delay of the different adders assuming suitable formula. b) Explain why two phase clocks are advantageous than single phase clock for sequential system,	

Ref No: Ex/PG/EE/T/129B/2024

M.E. ELECTRICAL ENGINEERING (1ST YR 2ST SEMESTER) EXAMINATION, 2024

(1st / 2nd-Semester Supplementary)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEM

Full Marks 100

Time: ~~Two hours~~/Three hours/ ~~Four hours~~/ ~~Six hours~~ (50 marks for each part)

	c) What does the term clock-skew mean? Explain why it is required.	5+5+5
4.	a) Explain the operation of different types of interconnect system (e.g. Antifuse, flash configuration and pass transistor).	
	b) In a multiplication process, the multiplicand is -5 and multiplier is 2. Show the steps of multiplication using Booth algorithm.	
	c) Given a two inputs lookup table with input a and b. Write the lookup table contents for the following Boolean functions: i) a AND b ii) NOT a iii) A XOR b	5+4+6
5.	a) A unit control process in a elevator system has the state names as i) Going Up, ii) Going down, iii) Idle and iv) Door open. Draw state diagram, declare all necessary variables, and list all possible transitions and actions. Write down the sequential program for program model of unit control. If two states are added as Fire Going down and Fire Door open, then draw a state diagram adding hierarchy,	
	b) Partition a circuit using Kerninghan-Lin algorithm, into two parts, such that every node is within a prescribed range and number of connections among the nodes is minimized. Show the cost of reduction in each iterative step.	8+7