REF. NO.: EX/PE/PC/B/T/225/2024

# NAME OF THE EXAMINATION: B.E. POWER ENGINEERING SECOND YEAR SECOND SEMESTER - 2024 SUBJECT: DIGITAL AND POWER ELECTRONICS

TIME: 3 HOURS

**FULL MARKS: 100** 

# COURSE OUTCOMES (CO)

- CO1: Explain Number Systems-Binary, Hexadecimal and Decimal, 1's and 2's Complement Representations, Binary Arithmetic, Boolean Logic and Logic Gates, Simplification using K-Maps
- CO2: Describe Sequential Logic and Flip Flops; Registers and Counters; Logic Family Characteristics and their Interfacing; 555 Timers in Different Modes
- CO3: Describe the Working Principle of Semiconductor Devices Such as Thyristor, BJT, JFET, MOSFET etc.
- CO4: Illustrate the Operation of Uncontrolled Rectifiers: Single-Phase, 3-Phase Bridge Rectifiers, Controlled Rectifiers: Single-Phase, 3-Phase Half Wave, Full Wave Bridge Circuits, Dual Converters
- CO5: Illustrate the Principle of Operation of AC Voltage Controllers, Cycloconverter, DC Choppers, 1-Ph, 3-Ph Inverters

### Attempt **ALL** questions

| 1. | Choo   | se the correct option for any TWENTY FIVE (25) questions: (25@1 = 25)                      |       |
|----|--------|--|-------|
|    | (i)    | The 12 bit 2's complement form of (-37) <sub>10</sub> is:                                  | [CO1] |
|    |        | a) 111110011011  |       |
|    |        | b) 110111011011  |       |
|    |        | c) 101101011011  |       |
|    |        | d) 111111011011  |       |
|    | (ii)   | An AND gate  | [CO1] |
|    | ` '    | a) is an any-or-all gate   |       |
|    |        | b) is equivalent to a series switching circuit   |       |
|    |        | c) is equivalent to a parallel switching circuit   |       |
|    |        | d) implements logic addition   |       |
|    | (iii)  | An XOR gate produces an output only when its two inputs are                                | [CO1] |
|    | ` ,    | a) low   |       |
|    |        | b) high  |       |
|    |        | c) different   |       |
|    |        | d) same  |       |
|    | (iv)   | The Boolean equation for a NAND gate is  | [CO1] |
|    |        | a) $C = A + B$   |       |
|    |        | b) $C = \overline{A + B}$  |       |
|    |        | c) $C = \bar{A} + \bar{B}$   |       |
|    |        | d) $C = \overline{AB}$   |       |
|    | (v)    | According to the absorption law of Boolean algebra , expression (A + AB) equals            | [CO1] |
|    |        | a) A + B   |       |
|    |        | b) A   |       |
|    |        | c) B   |       |
|    |        | d) AB  |       |
|    | (vi)   | The simplified form of the Boolean expression $(AB + C) (AB + D)$ can be written as        | [CO1] |
|    |        | a) ABD + ABC   |       |
|    |        | b) AB + CD   |       |
|    |        | c) AB + BCD  |       |
|    |        | d) ABC + CD  | 10001 |
|    | (vii)  | The purpose of a clock input to a flip-flop is to  | [CO2] |
|    |        | a) always cause change in the output states  |       |
|    |        | b) clear the device  |       |
|    |        | c) cause the output to assume a state dependent on the controlling (S - R, J-K or          |       |
|    |        | D) inputs  |       |
|    |        | d) set the device  | [000] |
|    | (viii) | A positive-edge triggered J-K flip-flop with $J = 1$ and $K = 1$ has a 10 kHz clock input. | [CO2] |
|    |        | The Q output is,   |       |
|    |        | a) a 5 kHz square wave   |       |
|    |        | b) a 10 kHz square wave  |       |
|    |        | c) constantly HIGH   |       |
|    |        | d) constantly LOW  |       |

| (ix)      | In a parallel in/parallel out shift register, $D0 = 1$ , $D1 = 1$ , $D2 = 1$ , and $D3 = 0$ . After | [CO: |
|-----------|---|------|
|           | two clock pulses, the data output is  |      |
|           | a) 1000   |      |
|           | b) 0001   |      |
|           | c) 1100   |      |
|           | d) 1110   | [00  |
| (x)       | What is the maximum possible range of bit-count specifically in n-bit binary                        | [CO: |
|           | counter consisting of 'n' number of flip-flops?   |      |
|           | a) 0 to $2^{(n+1)/2}$   |      |
|           | b) $0 \text{ to } 2^{n+1}$  |      |
|           | c) 0 to 2 <sup>n</sup>  |      |
|           | d) 0 to 2 <sup>n-1</sup>  | rco  |
| (xi)      | DTL family employs  | [CO  |
|           | a) diode and resistor   |      |
|           | b) diodes, resistors and transistors  |      |
|           | c) resistors and transistors  |      |
|           | d) diode and transistors  |      |
| (xii)     | An IC555 based astable multivibrator requires:  | [CO: |
|           | a) balanced time constants  |      |
|           | b) no external triggering input signal  |      |
|           | c) a pair of matched transistors  |      |
|           | d) dual J-K flip-flops  |      |
| (xiii)    | A TRIAC is a  | [CO: |
|           | a) 3 terminal bidirectional switch  |      |
|           | b) 3 terminal bilateral switch  |      |
|           | c) 2 terminal switch  |      |
|           | d) 2 terminal bilateral switch  |      |
| (xiv)     | Equalizing circuits are provided across each SCR in series operation to provide uniform             | [CO: |
|           | a) firing of SCRs   |      |
|           | b) voltage distribution   |      |
|           | c) current distribution   |      |
|           | d) heat distribution  |      |
| (xv)      | In a thyristor  | [CO: |
| ` /       | a) The latching current is equal to the holding current   |      |
|           | b) The latching current is greater the holding current  |      |
|           | c) The holding current is greater than latching current   |      |
|           | d) There is no relation between the latching current and the holding current                        |      |
| (xvi)     | In the forward blocking mode, the middle junction (J2) of a SCR has the                             | [CO: |
| ` /       | characteristics of that of a:   |      |
|           | a) transistor   |      |
|           | b) capacitor  |      |
|           | c) inductor   |      |
|           | d) diode  |      |
| (xvii)    | RC snubber circuit is used to limit the   | [CO3 |
| (*****)   | a) rate of rise of voltage across SCR   | -    |
|           | b) rate of rise of current in SCR   |      |
|           | c) conduction period  |      |
|           | d) all of the above   |      |
| (xviii)   | What is the total anode current of SCR in the equivalent circuit from the two                       | [CO3 |
| (*******) | transistors (T1 & T2) analogy of SCR?   | -    |
|           | a) The sum of the base current of T2 & collector current of T1                                      |      |
|           | b) The sum of both collector currents   |      |
|           | c) The sum of both base currents  |      |
|           | d) The sum of the base current of T1 & collector current of T2                                      |      |
| (xix)     |   | [CO4 |
| (XIX)     | If the firing angle in an SCR-controlled rectifier is decreased, the output is  a) increased        | ,    |
|           |   |      |
|           | ,   |      |
|           | a) romain unafforted  |      |
|           | c) remain unaffected<br>d) decreased  |      |

| (xx)      | A free-wheeling diode in phase-controlled rectifiers   | [CO4  |
|-----------|--|-------|
| ` '       | a) is responsible for additional harmonics   |       |
|           | b) improves the line power factor  |       |
|           | c) is responsible for additional reactive power  |       |
|           | d) avoids current chopping   |       |
| (xxi)     | In the circuit given below, when the free-wheeling diode is conducting then the  | [CO4] |
|           | , <b>, , , , , , , , , , , , , , , , , , </b>  |       |
|           | a) SCR has forward bias voltage and the load current is  |       |
|           | <sup>T</sup>   $\xi_R$ positive  |       |
|           | ovs FW0 → b)SCR has forward bias voltage and the load current is zero  |       |
|           | c) SCR has reverse bias voltage and the load current is  |       |
|           | positive   |       |
| (····:    | d)SCR has reverse bias voltage and the load current is zero  | 1004  |
| (xxii)    | - · · · · · · · · · · · · · · · · · · ·  | [CO4  |
|           | <ul><li>a) variable ac with fixed frequency is obtained</li><li>b) variable ac with variable frequency is obtained</li></ul>   |       |
|           | <ul><li>b) variable ac with variable frequency is obtained</li><li>c) variable dc with fixed frequency is obtained</li></ul>   |       |
|           | d) variable de with variable frequency is obtained   |       |
| (xxiii)   |  | [CO4] |
| (****/    | a) two SCRs in anti-parallel   | []    |
|           | b) one SCR is anti-parallel with one diode   |       |
|           | c) one SCR is parallel with one diode  |       |
|           | d) two SCRs in parallel  |       |
| (xxiv)    | In the cyclo-converter circuit given below, conduct in one cycle, while  | [CO4] |
|           | conduct in another cycle to produce equivalent positive and negative   |       |
|           | signal sequences respectively across output load.  |       |
|           | a  |       |
|           | a) T1, T2 T3, T4   |       |
|           | $\begin{array}{c ccccccccccccccccccccccccccccccccccc$  |       |
|           | Input tollage to the tollage tollage to the tollage tollage to the tollage to |       |
|           | ٧ <sub>s</sub> , f <sub>s</sub>  |       |
|           | 11 T3 ,  |       |
|           | b  |       |
| (444,000) | To DC above of the second of t | [COT] |
| (xxv)     | In DC chopper, the waveform for input and output voltages are respectively  a) Continuous, discontinuous   | [CO5] |
|           | b) Both discontinuous  |       |
|           | c) Both continuous   |       |
|           | d) Discontinuous, continuous   |       |
| (xxvi)    |  | [CO5] |
| ( )       | cycle of 50 % and Vs = 240V is:  |       |
|           | a) 120 V   |       |
|           | b) 240 V   |       |
|           | c) 360 V   |       |
|           | d) 480 V   |       |
| (xxvii)   | If T is the time period for a chopper circuit and D is its duty cycle, then the  | [CO5] |
|           | chopping frequency is  |       |
|           | a) D/Toff  |       |
|           | b) Ton/D   |       |
|           | c) D/Ton   |       |
|           | d) Toff/D  |       |
| (xxviii   | ) Single phase half bridge inverters requires  | [CO5] |
|           | a) three wire ac supply  |       |
|           | b) three wire dc supply  |       |
|           | c) two wire ac supply  |       |
| /!. \     | d) two wire dc supply  | [COE1 |
|           | Single-phase full bridge inverters require   | [CO5] |
| (xxix)    |  |       |
| (XXIX)    | a) 4 SCRs and 4 diodes   |       |
| (xxix)    | b) 4 SCRs and 2 diodes   |       |
| (XXIX)    | ,  |       |

(xxx) The output voltage in a single phase half bridge VSI with input DC voltage of Vs, varies between

- a) Vs and -Vs
- b) Vs and 0
- c) Vs/2 and -Vs/2
- d) Vs/2 and 0

## 2 Answer any TWO (2) questions

[2@7.5 = 15] [CO1]

[CO5]

- (a) Convert (105.15)<sub>10</sub> to its binary equivalent using successive multiplication/division as the case may be.
- (b) Subtract (19)<sub>10</sub> from (46)<sub>10</sub> using the 12-bit 2's complement arithmetic.
- (c) Simplify the Boolean expression (A + AB)(B + BC)(C + AB) using laws of Boolean algebra. Draw the simplified logic circuit.
- (d) Expand the expression  $A + B\overline{C} + AB\overline{D} + ABCD$  to min-terms.

## 3 Answer any TWO (2) questions

[2@7.5 = 15] [CO2]

- (a) What is the basic difference between a latch and an edge-triggered flip-flop? Write down the characteristic equation and truth table for S-R flip flop.
- (b) Design a 3-bit Parallel In Serial Out (PISO) shift register using D flip flops.
- (c) Design a Mod-6 Asynchronous counter using T-FF.
- (d) An IC 555 based Astable multivibrator operating at 150Hz has a charging time of 2.5ms. Find Duty cycle of the circuit.

## 4 Answer any TWO (2) questions

[2@7.5 = 15] [CO3]

- (a) Describe the different modes of operation using static V-I characteristics of thyristor. What is the effect of gate current on this characteristic?
- (b) With the help of two transistor model describe the turn-on process of a thyristor.
- (c) Why snubber circuits are used in thyristor circuits? Draw and explain a complete protection scheme for a typical thyristor circuit.
- (d) What is commutation? Where are forced commutation circuits implemented? Explain the class B commutation (self-commutation by LC circuit) method for SCR.

#### 5 Answer any TWO (2) questions

[2@7.5 = 15] [CO4]

- (a) A voltage of 200sin314t is applied to a thyristor controlled half-wave rectifier with a resistive load of  $50\Omega$ . If the firing angle is 30° with respect to supply voltage waveform, find the average power in the load. Derive the necessary expression.
- (b) Explain with proper waveforms, the operating principle of freewheeling diode for single-phase controlled half-wave rectifier circuit (assume that the nature of load is RL and supply voltage is  $V_{m}sin\omega t$ ).
- (c) A single phase half wave AC voltage controller has a resistive load of R = 20  $\Omega$  and the input voltage is Vs = 240 V, 50 Hz. The delay angle of thyristor is  $\alpha = \pi/3$ . Determine:
  - (a) The RMS value of output voltage Vo
  - (b) The average input current
- (d) For a single phase ac voltage half-controller feeding a resistive load, prove mathematically that it produces symmetrical voltage in positive and negative halves, thereby making the average value equal to zero.

#### 6 Answer any TWO (2) questions

[2@7.5 = 15] [CO5]

- (a) Explain briefly the function of a cyclo-converter. With the help of output waveform explain the operation of a single phase controlled cyclo-converter.
- (b) Explain with suitable circuit diagram of waveforms, the operation of a step-down chopper. Derive the expression for output voltage in terms of duty cycle for such a chopper.
- (c) Input to a step-up chopper is 200 V. The output required in 600 V. If the conducting time of the thyristor switch is 200 μs, compute (i) chopping frequency, (ii) if the pulse width is halved for constant frequency operation, find the new output voltage.
- (d) With the help of circuit and waveform diagrams, explain the operation of a single-phase half-bridge type inverter.