Ref. No.: Ex/IEE/PE/B/T/414B/2024

B.E. INSTRUMENTATION AND ELECTRONICS ENGINEERING FOURTH YEAR FIRST SEMESTER EXAM 2024

VLSI DESIGN

Time: Three Hours

Full Marks: 100

Module 1: Answer any two questions [40]

1.a) Consider the MOS structure that consists of a p-type doped Si substrate, a $Si0_2$ layer and a metal (Al) gate. The equilibrium Fermi potential of the doped Si substrate is $q\phi_{Fp}$—0.2eV. Using electron affinity for Si & work function for Al given in figure, Calculate the built in potential difference across MOS system. 5

b) Deduce the expression of thickness and charge density in the depletion region of the MOSFET. 15

2. a) Describe the various capacitances that develop in different regions of the MOSFET. 5

b) Derive the threshold voltage expression of the MOSFET. 15

3. a) Discuss channel length modulation of MOS transistor. 6

b) Discuss substrate bias effect of a MOS transistor. 4

c) Write a short note about BiCMOS. 10

Module 2:[20]

4. Discuss twin tube fabrication process for MOSFET with neat diagram. 20

Module -3: Answer anyone questions [20]

5. a) Design a full adder circuit using CMOS. 6

b) Discuss cascading problem of dynamic logic gates. 4

c) Design domino logic for the expression $Y = \overline{A + (B.C)}$ 5

d) Describe the operation of a pass transistor. 5

6. a) Describe the CMOS stick diagram design rules and draw the stick diagram for the expression $Y = \overline{(A.B + C.D + E)}$ 5

b) Design positive edge-triggered master-slave register. 5

c) Design 16x1 MUX using pass transistor. 5

d) Design D flip-flop using pass transistor. 5

[Turn over

7. a) Write a short note about lamda (λ) and micron (μ) rules. 4
   b) Discuss Shannon's expansion theorem. 3+3
   $f(w,x,y,z) = \sum(0,1,2,3,4,11,12,15)$. Using the residue map, find the residues of $f(w,x,y,z)$ with respect to $Y = \{w,x,y\}$. 10

Module -4: [20]

8. a) What is 'Design for Testability', and why do we need it? 5
   b) What is the difference between Verification and Testing? 5
   c) What is Fault Modeling? Why is Fault Model needed? 5+5