Ref. No: EX/IEE/PC/B/T/314/2024

BIEE 3rd YEAR EXAMINATION, 2024
(1st Semester)
SUBJECT: Microcontrollers

Time: Three hours | Full Marks 100

Question		Assume that the 8051 μC uses a 12 MHz crystal	Marks
		UNIT-I (Answer all three)	
1.	(i)	With examples explain the working of RL and RLC instructions.	5
	(ii)	With examples explain the working of the DAA instruction.	5
	(iii)	Explain the usage of the bank registers of the 8051 μC.	5
	(iv)	What is a power-on reset (POR)? How is it implemented using a simple RC network?	5
		UNIT-II (Answer any two)	
2.		Eight unsigned integers are stored in bank registers R0-R7. Write an assembly language program that generates the integer average of the aforesaid eight integers and stores it in location 30H of the on-chip memory.	12
3.		Write an assembly language program that multiplies a two-byte unsigned integer stored in R0-R1 by a one-byte unsigned integer stored in R2, and stores the result back in R0-R1-R2.	12
4.		Write an assembly language program that compares the two-byte unsigned integers stored in R0-R1 and R2-R3 and sets the CY flag if the content of R0-R1 is greater than that of R2-R3. Calculate the execution time of the program.	8+4
		UNIT-III (Answer all three)	
5.		Write an assembly language program that configures Timer-1 in auto-reload mode and uses the timer overflow interrupt to generate a 100 Hz pulse train of 25% duty cycle at P1.0.	10
6.		How do you enable/disable the 8051 interrupt inputs? What are the interrupt priority levels and how do you set them? How the μC resolves the issue of concurrent interrupts?	4+4+2
7.		Write an assembly language program that configures the serial port in mode-1 with the receiver disabled and sets the baud rate at 9600 baud. Calculate the exact baud rate generated. Write another stretch of code that generates the 2's complement of the data in R0-R7 and transmits them through the serial port.	3+2+5

[Turn over

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Question.	Assume that the 8051 μC uses a 12 MHz crystal	Marks
	UNIT-IV (Answer all questions)	
10	Draw the complete connection diagram of a DAC0800 chip with an AT89C51 μC where: • P1 is used as the data-bus • The DAC uses a 10V V_{REF+}, V_{REF-} is grounded • The output swings between ± 10V (approximately) Write an assembly language program that repeatedly generates a bit pattern of 11000011 at the output of the DAC ('1' corresponds to +10v and '0' corresponds to -10v) such that the width of each bit is 100 μsec.	4+6
11.	Draw the complete connection diagram of an ADC0808 chip with an AT89C51 μC where: • P1 is used as the data-bus • P0.0 drives the SC/ALE pin; P0.1 drives the OE pin • P2.0 reads the EOC pin Write an assembly language program that reads the analog channel 2 at a 10 kHz rate and stores the converted data in location 30H of on-chip memory.	4+6
12.	For the ICM7218B LED display controller: (i) Explain the protocol for transferring data from the microcontroller to the display RAM. (ii) Display data format when an internal data decoder is selected.	4+2

80C51 Instruction Set

Arithmatic operations		
mnemonic	byte	m/c cycle
ADD A, Rn/@Ri	1	1
ADD A, direct,#data	2	1
ADDC A, Rn/@Ri	1	1
ADDC A, direct/#data	2	1
SUBB A, Rn	1	1
SUBB A, direct	2	1
SUBB A, @Ri	1	1
SUBB A, #data	2	1
INC A/Rn/@Ri	1	1
INC direct	2	1
DEC A/Rn/@Ri	1	1
DEC direct	2	1
INC DPTR	1	2
MUL AB	1	4
DIV AB	1	4
DA A	1	1
Logical operations		
mnemonic	byte	cycle
ANL A, Rn/@Ri	1	1
ANL A, direct/#data	1	1
ANL A, #data	2	1
ANL direct, A	2	1
ANL direct, #data	3	2
ORL A, Rn/@Ri	1	1
ORL A, direct/#data	2	1
ORL direct, A	2	1
ORL direct, #data	3	2
XRL A, Rn/@@Ri	1	1
XRL A, direct/#data	2	1
XRL direct, A	2	1
XRL direct, #data	3	2
RL A	1	1
RLC A	1	1
RR A	1	1
RRC A	1	1
SWAP A	1	1
Program branching		
mnemonic	byte	m/c cycle
ACALL addr11	2	2
LCALL addr16	3	2
RET	1	2
RETI	1	2
AJMP addr11	2	2
LJMP addr16	3	2
SJMP add8	2	2
JZ/JNZ rel	2	2
CJNE A, direct, rel	3	2
CJNE A, #data, rel	3	2
CJNE Rn, #data, rel	3	2
CJNE @Ri, #data, rel	3	2
DJNZ Rn, rel	3	2
DJNZ direct, rel	3	2
NOP	1	1
Data transfer		
mnemonic	byte	m/c cycle
MOV A, Rn/@Ri	1	1
MOV A, direct/#data	2	1
MOV Rn, A	1	1
MOV Rn, direct	2	2
MOV Rn, #data	2	1
MOV direct, A	2	1
MOV direct, Rn	2	2
MOV direct, direct	3	2
MOV direct, @Ri	2	2
MOV direct, #data	3	2
MOV @Ri, A	1	1
MOV @Ri, direct	2	2
MOV @Ri, #data	2	1
PUSH direct	2	2
POP direct	2	2
XCH A, Rn	1	1
XCH A, @Ri	1	1
XCHD A, @Ri	1	1
Boolean variable manipulation		
mnemonic	byte	m/c cycle
CLR C	1	1
CLR bit	2	1
SETB C	1	1
SETB bit	2	1
CPL C	1	1
CPL bit	2	1
ANL C, bit	2	2
ANL C, /bit	2	2
ORL C, bit	2	2
ORL C, /bit	2	2
MOV C, bit	2	1
MOV bit, C	2	2
JC/JNC rel	2	2
JB/JNB bit, rel	3	2
JBC bit, rel	3	2