

## BACHELOR OF INSTRUMENTATION AND ELECTRONICS ENGG

EXAMINATION 3<sup>RD</sup> YEAR, 1<sup>ST</sup> SEMESTER, 2023

## COMPUTER ORGANIZATION, ARCHITECTURE AND NETWORKING

Time: (0.5+3+1) hours

Full marks: 70

**PART A (35 MARKS)****CO1 :**

1. a) A computer system has a cache memory of size 512KB, Block size is 1KB and each Tag size contains 1bits. Calculate main memory size and tag directory size.

b) In a 3-level memory hierarchy, the access time of cache, main memory and virtual memory is 5nano seconds, 100nano seconds and 10milli-seconds respectively. If the hit ratio is 80% for the cache and 99.5% for the main memory, then what is the closest average access time of memory hierarchy in nano seconds?

c) Consider a 4-stage pipelining processor. The number of cycles needed by the 4 instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

|    | S1 | S2 | S3 | S4 |
|----|----|----|----|----|
| I1 | 2  | 1  | 1  | 1  |
| I2 | 1  | 3  | 2  | 2  |
| I3 | 2  | 1  | 1  | 3  |
| I4 | 1  | 2  | 2  | 2  |

What is number of cycles needed to execute following loop:  
For (i= 1 to 2) {I1; I2; I3; I4}

[6+6+5=17]

**CO2 :**

2. a) Consider the following set of processes with the given burst time and arrival time in millisecond as follows.

| Process no. | Priority | Arrival time | Burst time |
|-------------|----------|--------------|------------|
| 1           | 2        | 0            | 4          |
| 2           | 4        | 1            | 2          |
| 3           | 6        | 2            | 3          |
| 4           | 10       | 3            | 5          |
| 5           | 8        | 4            | 1          |
| 6           | 12       | 5            | 4          |
| 7           | 9        | 6            | 6          |

Give the sequence of processes as they get share of CPU in preemptive priority scheduling algorithm and RR algorithm with time quantum 2ns, using GNATT chart. Hence calculate the average waiting time, Turn around time of all these.

b) Consider a system with Byte addressable memory, 32bit logical addresses, 4KB page size and page table entries of 4B each. What is the size of page table in MB, what are sizes of physical address space, page offset and no. of pages and frames?

[ Turn over

c) A file system with 300 GByte disk uses a file descriptor with 8 direct block addresses, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. What is the maximum possible file size in this file system?

[8+6+4=18]

### **PART B (35 MARKS)**

#### **CO3:**

1. Difference between Selective Repeat and Go Back N flow control algorithms
2. Consider a token ring network with a length of 2km having 10 stations including a monitoring station. The propagation speed of the signal is  $2 \times 10^8$  m/s and the token transmission time is ignored. If each station is allowed to hold the token for 2  $\mu$ -sec, what is the minimum time for which the monitoring station should wait (in  $\mu$ -sec) before assuming that the token is lost?
3. The message 11001001 is to be transmitted using CRC polynomial  $X^3+1$  to protect it from errors. What is the message that should be transmitted?
4. What is the minimum frame size required for a CSMA/CD based computer network running at 1Gbps on a 200m cable with a link speed of  $2 \times 10^8$  m/s?

[4+4+4+4=16]

#### **CO4 :**

5. Explain problem and solution of Distance Vector Routing algorithm
6. Difference between packet switching and circuit switching.
7. 2 computers C1 and C2 are configured as follows. C1 has IP address 203.197.2.53 and netmask 255.255.128.0. C2 has IP address 203.197.75.201 and netmask 255.255.192.0. Check what both C1 and C2 assume whether they are on same networks or not?
8. The address of class B host is to be split into subnets with a 6bit subnet number. What is the maximum number of subnets and maximum number of hosts in each subnet?

[5+4+5+5=19]