Ref. No.: Ex/IEE/PE/B/T/324A/2024

B. INS. & ELEC. ENGINEERING 3RD YEAR 2ND SEMESTER EXAMINATION 2024

ANALOG MOS CIRCUIT DESIGN

TIME: 3 HOURS **FULL MARKS: 100**

List of Course Outcomes (CO):

CO1: Classify and analyze different types of MOS amplifiers (K4, A1-recognize)

CO2: Explain and interpret the importance of differential amplifiers (K3, A1)

CO3: Describe and explain the behavior of current mirrors (K2, A1)

CO4: Explain and analyze the frequency response of MOS amplifiers (K4, A1)

Instructions to the Examinees:

- Each module is mapped with the corresponding CO
- Attempt questions from **ALL** the modules
- Alternative questions exist within a module, not across the modules
- Different parts of same question should be answered together
- Clearly state any assumption and derive the necessary equation(s) for calculation
- Unless otherwise stated, use the device data shown in Table I and assume $V_{DD} = 3\,V$ where necessary

Table I

Symbol	Value	Unit
$V_{th,n}$	0.7	V
$V_{th,p}$	−0.8	V
γ_n	0.45	$V^{1/2}$
γ_p	0.4	$V^{1/2}$
$\mu_n C_{ox}$	50	$\mu A/V^2$
$\mu_p C_{ox}$	25	$\mu A/V^2$
λ_n	0.1	V^{-1}
λ_p	0.2	V^{-1}

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MODULE 1

(ATTEMPT **ALL QUESTIONS** FROM THIS MODULE)

1. Sketch I_X and trans-conductance of the transistor as a function of V_X for **any one** of the circuits in Fig. 1 as V_X varies from 0 to V_{DD}.

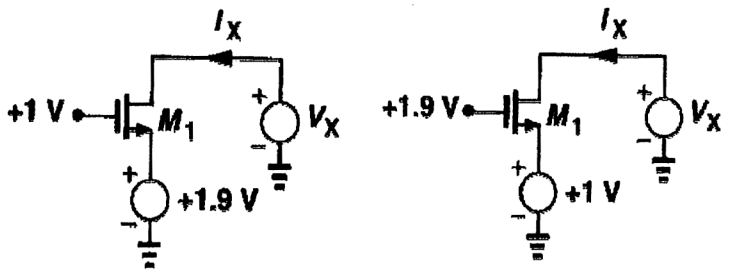

Fig. 1

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2. Sketch v_{out} versus v_{in} for **any one** of the circuits in Fig. 2 as v_{in} varies from 0 to V_{DD}. Identify the important transition points.

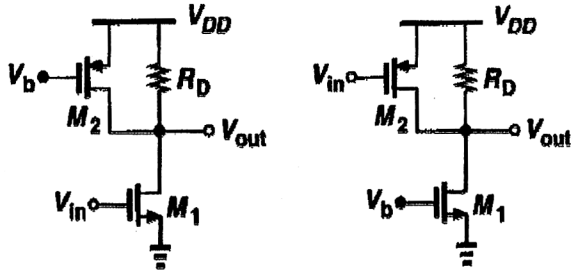

Fig. 2

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3. Assuming all MOSFETs are in saturation, calculate the small signal voltage gain for **any one** of the circuits in Fig. 3. ($\lambda \neq 0,\ \gamma = 0$)

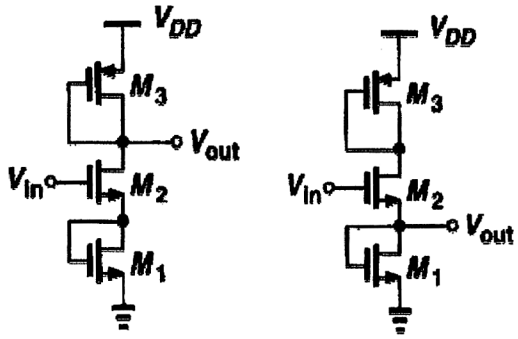

Fig. 3

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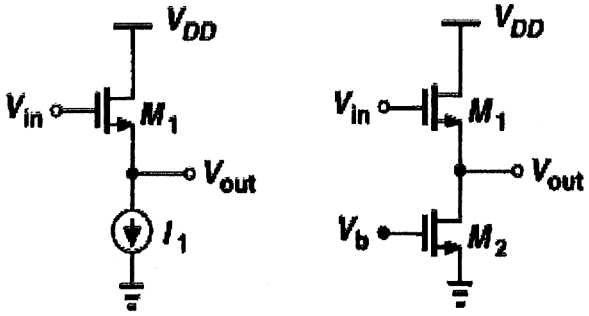
4. Suppose in the source follower of Fig. 4(a), $\left(\frac{W}{L}\right)_1 = 40, I_1 = 200\,\mu A, V_{th,0} = 0.6\,V, 2\varphi_F = 0.7\,V$. Calculate v_{out} for $v_{in} = 1.2\,V$. If I_1 is implemented as M_2 in Fig. 4(b), find the minimum value of $\left(\frac{W}{L}\right)_2$ for which M_2 remains saturated.



(a) **(b)**

Fig. 4

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MODULE 2

(ATTEMPT **Q. NO. 5** AND ANY **ONE** FROM THE REST)

5. A differential pair uses input NMOS devices with $\left(\frac{W}{L}\right) = 100$ and a tail current of 1 mA. What is the equilibrium overdrive voltage of each transistor? How is the tail current shared between the two sides if $V_{in,1} - V_{in,2} = 50\,mV$? What is the equivalent G_m under this condition? Assume $\left(\frac{W}{L}\right) = 100$ *and* tail current of 1 mA.

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6. What is the significance of CMRR? Calculate the value of CMRR of an assymetric differential amplifier stage with non-ideal tail current source.

3+12

7. Assuming the circuit shown in Fig. 5 is symmetric, sketch V_{out} as $V_{in,1}$ *and* $V_{in,2}$ are (i) equal and vary from zero to V_{DD} & (ii) vary differentially from zero to V_{DD}

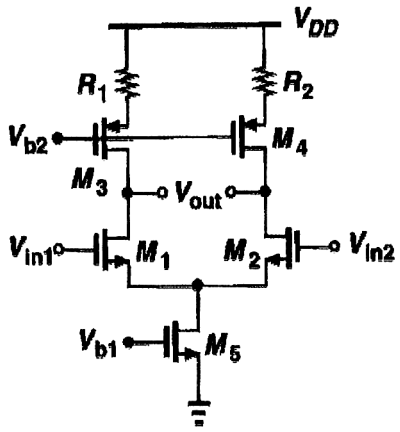

Fig. 5

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MODULE 3

(ATTEMPT **Q. NO. 8** AND ANY **TWO** FROM THE REST)

8. Select **one or more** correct option(s) from the choices given below:

(a) Current mirror circuits can be constructed using

(i) n-MOS only

(ii) p-MOS only

(iii) Both n-MOS and p-MOS in the same circuit

(iv) Both n-MOS and p-MOS in different circuits

(b) Cascode current mirror circuit is used to

(i) Suppress the effect of channel length modulation

(ii) Improve the voltage headroom

(iii) Minimize the requirement of MOS transistors

(iv) Reduce the power consumption

(c) Active current mirrors are those which

(i) Carry bias current only

(ii) Carry time varying current

(iii) Do not carry any current through it

(iv) None of the above

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9. Assuming perfect symmetry, sketch the output voltage of the circuit in Fig. 6 as V_{DD} varies from 3 V to 0. Assume that for $V_{DD} = 3\ V$, all of the devices are saturated.

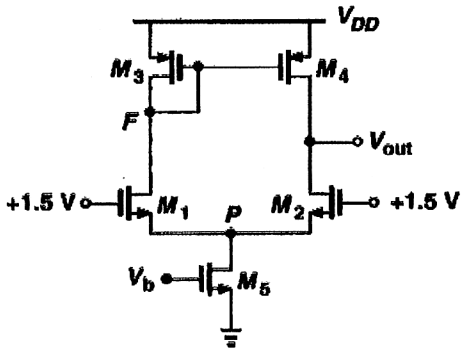

Fig. 6

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10. Assuming all the transistors are identical, sketch V_X and V_Y as a function of V_{DD} for the circuit in Fig. 7.

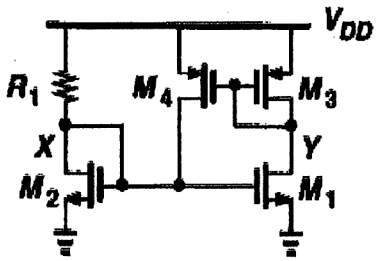

Fig. 7

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11. Show that the common-mode gain of the circuit in Fig. 8 with g_m mismatch is approximately given by:

$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{(g_{m1} - g_{m2})r_{o3} - \left(\frac{g_{m2}}{g_{m3}}\right)}{1 + (g_{m1} + g_{m2})R_{SS}}$$

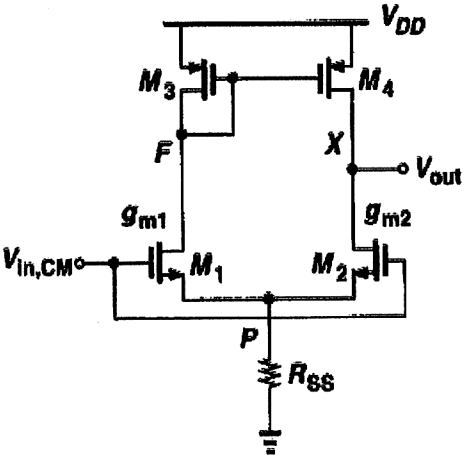

Fig. 8

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MODULE 4

12. Calculate the input impedance of **any one** of the circuits in Fig. 9.

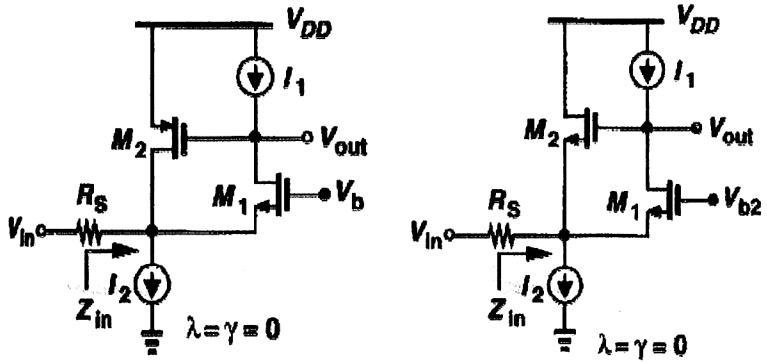

Fig. 9

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