Bachelor of Instrumentation and Electronics Engineering, 2024
2nd year, 1st semester
DIGITAL ELECTRONICS

Time : Three hours **Full Marks : 100**

ANSWER ALL MODULES

Module – I (4 Marks)

Q1. What decimal number corresponds to the binary pattern **11001000**, when it is in (a) **Excess-3 BCD** format, (b) **2's complement** format, and (c) **Gray** format. Can this pattern represent a decimal number in Normal BCD format ? If Yes, what is that decimal number ? If Not, why ? (4)

Module – II (6 Marks)

Q2. Perform the following arithmetic operations (**Represent the final results in decimal**) :

(a) **(-27) + (-101)** using **8-bit 1's** complement number system.

(b) **(786) + (295)** using **Excess-3 BCD** numbers.

(3+3)

Module – III (40 Marks)

(Answer Q3 and ANY ONE from Q4 and Q5)

Q3. (a) What are the advantages of **CMOS transmission gates** over both **n-MOS and p-MOS pass transistors** for connecting signals to a bus ?

(b) Why outputs of two CMOS gates should never be shorted together ?

(b) Draw the circuit of a **2-input TTL NOR** gate with totem-pole output.

(c) Draw the nMOS circuit to realize a **Full-Subtractor**. (4 + 3 + 5 + 8)

Q4. (a) Use **Karnaugh Map** technique to obtain the minimized expressions for the following functions as indicated :

(i) $f(A,B,C,D) = \sum m(0, 2, 4, 5, 8, 10, 13, 15)$ **(using POS format)**

(ii) $f = A'B'D' + B'D + AB'D' + A'BC'D + ABD + ACD + ABC'$ **(using SOP format)**

(iii) $f(W,X,Y,Z) = \prod M(3, 4, 11, 12, 13, 14)$ **(using NAND gates only)**

(b) Establish that **Multiplexers** can also be used as **Universal Logic Components.**

(3 x 5 + 5)

Q5. (a) Using suitable **Multiplexers** realize a **Full-Subtractor. Draw necessary diagram.**

(b) In the circuit shown in **Fig. P5(b)**, the final output produced is **F = (AB)'.(C'D)'**. What **type of gates** are **G1 and G2** ?

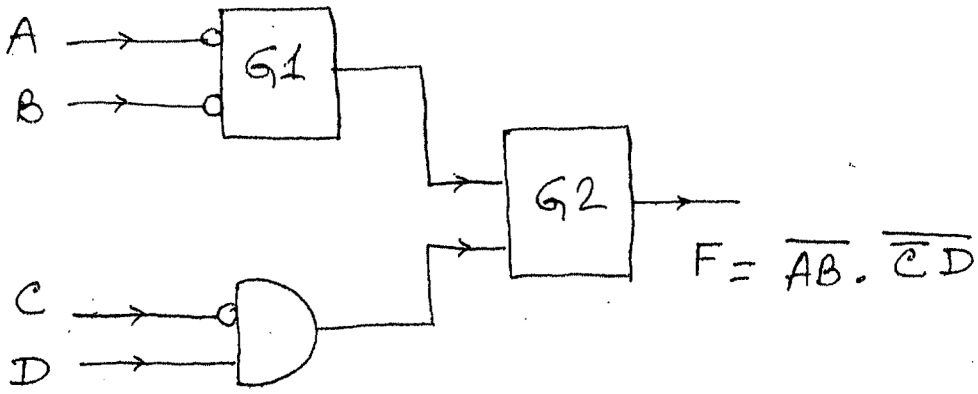


Fig. 5(b)

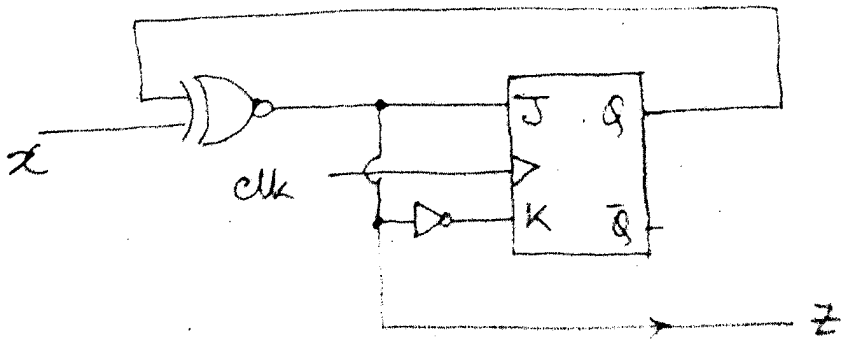
(c) Realize a **3-input Priority Encoder** using a suitable **Decoder** of **minimal configuration** and necessary **logic gates in minimum number**. Explicitly mention the priority order chosen for the inputs and corresponding output codes. **Draw** the **necessary diagram.**

(6 + 4 + 10)

Module – IV (50 Marks)
(Answer Q6 and ANY ONE from Q7 and Q8)

Q6. (a) Using **D Flip-flop** as the memory element, realize a **JK flip-Flop**. (10)

(b) For the circuit shown in Fig. **P6(b)** realize and draw the **State Transition Diagram**. Input to the circuit is **A** and the output is **Z**. What do we achieve from this circuit configuration? Is it a **Moore** machine **or** a **Mealy** machine ? (6 + 3 + 1)



Input : x

Output : z

Fig. P6(a)

Q7. Design a **Sequence detector** which detects the presence of input sequence "**010**" by raising an **output flag by 1**. The output **remains 0 otherwise**. Use **T-FFs** as memory elements. Is there **any lock-out possibility** in your design ? Justify. (18 + 2)

Q8. (a) Design a **sequence generator** which generates the sequence "**0100110**" repeatedly. Use **minimum number** of **D-FFs**.

(b) Using **D-FFs** as memory elements, realize **a Modulo 6 Gray down counter**. (10 + 10)