Bachelor of Instrumentation and Electronics Engineering, 2024
2nd year, 1st semester Supplementary

DIGITAL ELECTRONICS

Time : Three hours **Full Marks : 100**

Answer *ANY FIVE*

Q1. (a) With the help of an example, explain how the occurrence of overflow in 1's complement arithmetic is detected. Design a logic circuit for this overflow detection.

(b) Distinguish between (i) Moore Machine and Mealy Machine; (ii) Latch and Flip-Flop.

(c) Outputs of two CMOS gates should never be shorted together. Explain.

((3 + 7) + 6 + 4)

Q2. Design a **MOD-6** synchronous **lockout-free Gray code counter** which counts from **1 to 6** repeatedly in Gray format. Use **JK-FFs** as memory elements.

(20)

Q3. Design a synchronous sequential **Moore machine that detects the presence of input sequence "101" without overlapping. Use T**-FFs as the memory elements.

(20)

Q4. (a) Realize a **2:1** multiplexer using logic gates.

(b) Cascading the 2:1 multiplexers realize one **8:1** Multiplexer.

(c) Using two 2:1 multiplexers realize one **2-input XOR** function.

(d) Implement the following function using **one 8:1** multiplexer and **one 2:1** multiplexer **(if needed)** :

$$F(W, X, Y, Z) = WX'Z' + W'XZ' + WX' + YZ$$

(2 + 2 + 2 + 14)

Q5. (a) Design a sequence generator which generates the sequence **"0011010"** repeatedly.

(b) What is the **race-around problem** in JK-Latch ? How is it avoided ?

(15 + 5)

Q6. (a) Use **Karnaugh Map** technique to obtain the minimized expressions for the following functions as indicated :

(i) $F(W, X, Y, Z) = \prod M(1, 4, 6, 7, 9)$; **in minimized SOP form**

(ii) $F(A, B, C, D) = AB'D + A'B'D' + AB' + B'C$; **in minimized POS form**

(iii) $F(A, B, C, D) = \prod M(3, 4, 5, 6, 7, 9, 13, 15)$; **in minimized NAND-NAND form**

(b) Realize a **T-FF** using **one SR-FF** as the memory element.

(4 + 4 + 4 + 8)

Q7. Write **short technical notes** on : (4 x 5)

(a) Advantages of CMOS logic family.

(b) Use of tri-stated TTL logic.

(c) Use of NAND latch in switch debouncing.

(d) Use of NOR gates as Universal Logic Gates.

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