Ex/IT/PC/B/T/215/2024

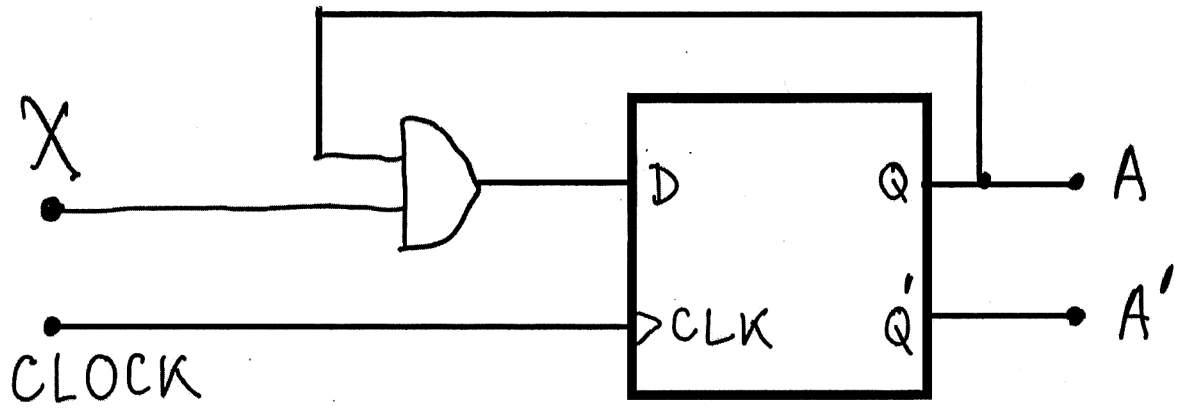
BE INFO TECH 2nd YEAR 1st SEMESTER EXAMINATION, 2024

Computer Organization and Architecture

Time: 3 Hours Full Marks: 100

Answer All 10 Questions

1.a) Study the following sequential circuit. Write down the Equation, State Table and State Diagram of this circuit.



b) Write down the steps taken to process an Interrupt. (6+4)[CO1]

2.a) Write down -5 and -7 in Two's Complement form of 4bits. Now add them and analyze the results.

b) Write down 253 in 8 bit binary format. Convert this number to Octal and Hexa-Decimal format. Now, sign-extend this number to 16 bit binary fomat.

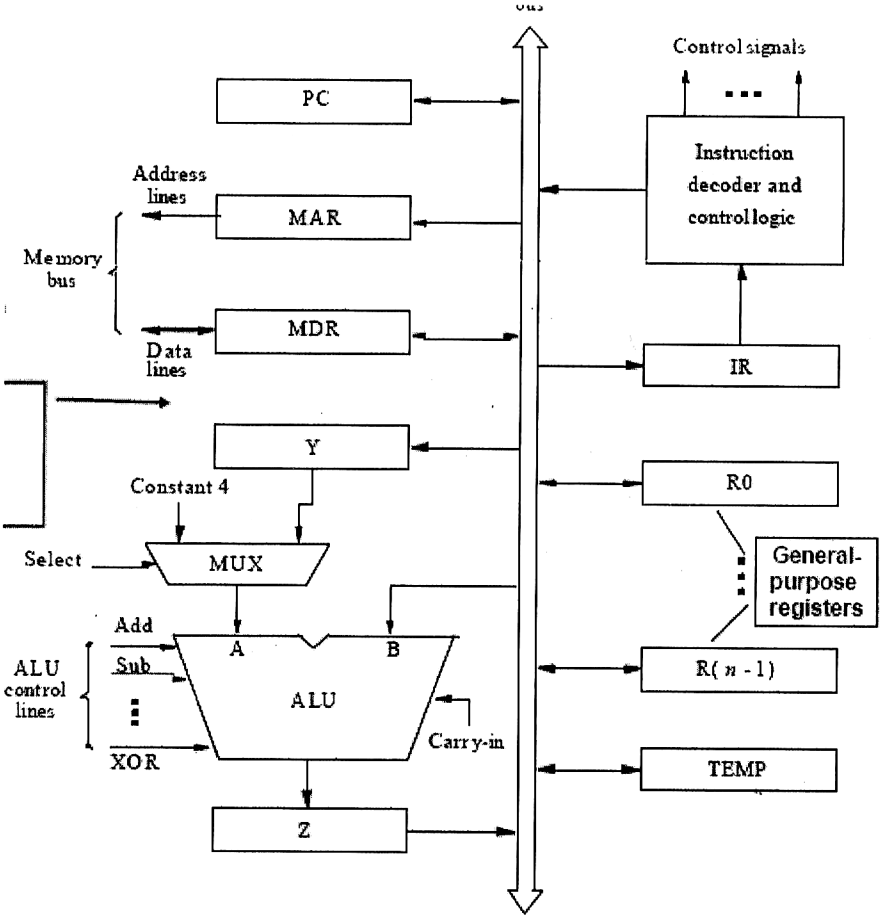
c) What are the differences between Ordinary Binary Multiplication and Booth Multiplication. (3+4+3)[CO2]

3.a) With proper examples, explain different types of IEEE 754 Rounding Modes.

b) Convert the decimal numbers 456789 & 37890 to IEEE 754 Floating Point Number (Half Precision). Now add these two floating point numbers and convert the result back to the decimal number. (4+6)[CO2]

[Turn over

4.a) With respect to the diagram shown below, write down and explain the complete sequence of micro-operations performed by the CPU to execute the instruction "Add R4, R3, (R2)" [R4+R3 → (R2)].



b) List down the methods of generating control signals by the CPU to execute instructions. Briefly explain one of them. (6+4) [CO3]

5.a) Write down the sequence of instructions needed to evaluate the expression "X=A+(B*C)" for a Three-Address, Two Address, One-Address and Zero-Address instruction format CPU.

b) The memory locations 100, 200 and 300 contain 200, 300 and 100 respectively. What will be the contents of the CPU registers R1 after executing the Assembly Language Instructions "Mov R1, #150; Add R1, (200); Add R1, #50". Justify your answer.

c) List down 4 different Addressing Modes of CISC CPU. (4+4+2) [CO3]

6.a) Using proper Research Data, justify how a RISC CPU gains because of the Large Number of CPU Registers compared to a CISC CPU.

b) List down those Characteristics of a RISC CPU which helps better Pipelining performance of a RISC CPU. (5+5) [CO3]

7.a) A sequence of 8 bytes (in Hex) 3A, 2B, 1E, F0, 22, FA, 78 and 2C are stored starting from memory address 100. Let's assume that the byte storage order in the memory is as per Little Endian format. A "long long" variable and an "Unsigned Short" variable are defined starting from the memory location 100 and 104 respectively. What will be the value of these variables in Hex? Justify your answer.

b) With regard to Question 7a; if the byte storage order is as per Big Endian Format, what will be the values of those two variables? Assume, variable locations remain the same.

c) With regard to the 4 way set associative mapping cache (byte addressable memory); the size of the cache is 16KByte, the size of one Cache block is 32Byte and the size of the memory 256 Kbyte. What will be the size of the TAG field and the Set field (in bits)? Justify your answer precisely. (4+2+4) [CO4]

8.a) An approximate specification of a Toshiba P300 Hard Drive (HDWD130 3.5") is given below.

No of Surfaces = 6
Individual Sector Size = 4096 byte
No of Sectors per track = 256
Average No of tracks per surface = 345078
Rotational Speed = 7200RPM
Maximum seek time = 20ms
Average seek time = 10ms
Track-to-track seek time = 2ms

What is the Storage Capacity of a Single Track, A Complete Cylinder and The Entire Disk? [Show all computations properly]

b) With respect to the disk mentioned above, answer the below questions.

i) What is the total time required to read a single track?
ii) What is the total track-to-track seek time?
III) What is the total time required to read all the tracks?
iv) What is the total time required to read a single cylinder?
v) What is the total time required to read the entire disk, assuming that the starting position of the Read/Write Arm is at the outermost track?

c) With proper examples, explain the differences between Level 0 and Level 1 RAID. (3+5+2) [CO4]

9.a) For a Binary Tree of Depth 5, answer the following.
i) How many processor nodes?
ii) How many switch Nodes?
iii) What is the Diameter?
iv) What is the Bisection width?
v) How many Edges per node?
vi) Whether this kind of tree has constant edge length.

b) Draw the complete diagram of UMA, NUMA and Multicomputer architecture with proper labeling. (5+5) [CO5]

10.a) With proper Numerical Examples, explain the concept of Speedup, Algorithmic Scalability and Architectural Scalability.

b) With proper examples, show how Sorting can be done in parallel. (5+5) [CO5]