Ex/IT/PC/B/T/215/2024(S)

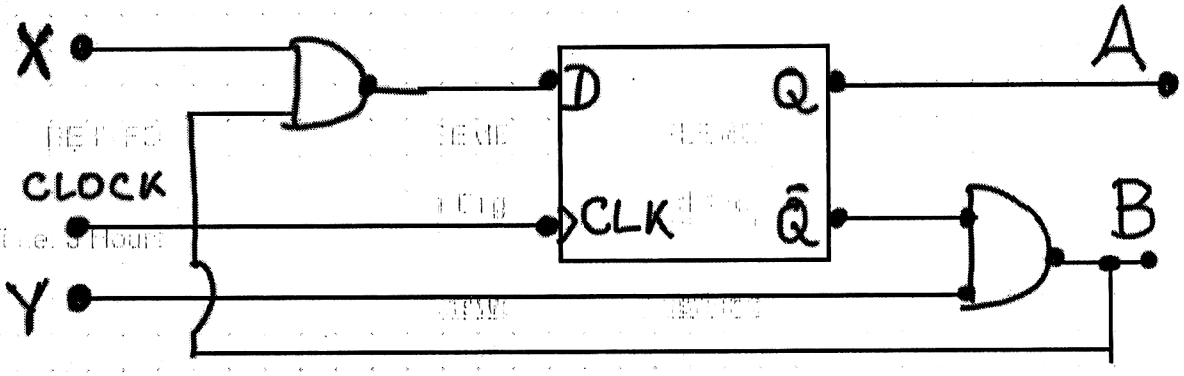
BE INFO TECH 2nd YEAR 1st SEMESTER SUPPLEMENTARY EXAMINATION 2024

Computer Organization and Architecture

Time: 3 Hours Full Marks: 100

Answer All 10 Questions

1.a) Study the following sequential circuit. Write down the Equation, State Table and State Diagram of this circuit.



b) What are different situations under which Internal Interrupts can occur.

(6+4)[CO1]

2.a) Convert the number $(78564981)_{10}$ to Binary, Octal and Hexa-Decimal Number.

b) Write two 8 bit Binary numbers in 1's Complement Format. Choose the numbers such a way that, adding them gives Overflow Condition.

c) With proper examples (one should be positive and the other should be negative), show how a 2's Complement number can be sign-extended. (3+4+3)[CO2]

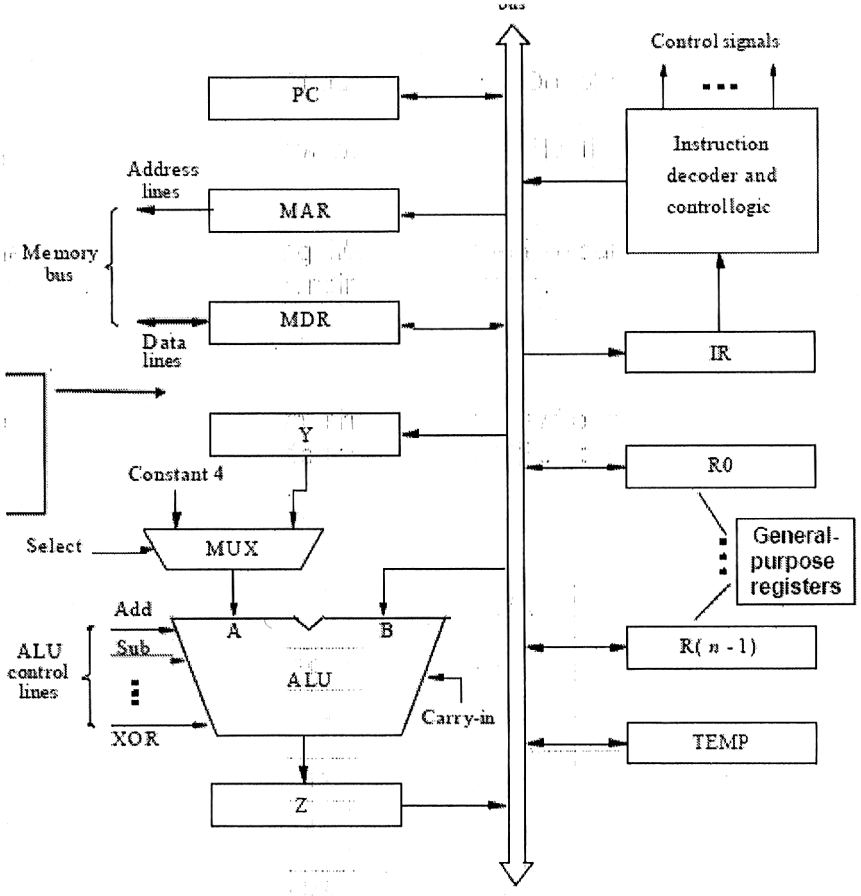
[Turn over

3.a) Convert the decimal number 10000 to IEEE 754 Double Precision Floating Point number.

b) With proper examples, show how two IEEE 754 Floating Point Numbers (Half Precision) can be added.

c) One of the IEEE 754 Rounding Mode is called "Round to the Nearest". With proper examples, show how this kind of rounding mode works. (4+4+2)[CO2]

4.a) With respect to the diagram shown below, write down and explain the complete sequence of micro-operations performed by the CPU to execute the instruction "Add R3, <Mem>" [R3 + <Mem> → <Mem>].



b) What is Control Word (CW), Microroutine & Microinstruction? (7+3) [CO3]

5.a) Using proper Assembly Language Instruction, explain Three-Address, Two-Address, One-Address and Zero-Address instruction format of a CPU.

b) With proper examples explain different categories of Instruction Types.

c) List down the names of the various condition codes. (4+4+2) [CO3]

6.a) What could be the reasons behind the large number of registers in the RISC CPU? Explain and Illustrate.

b) With proper examples and diagrams, explain how Pipelining is done in a RISC CPU. (5+5) [CO3]

7.b) Differentiate between Memory Access Time and Memory Cycle Time.

c) How many bytes will be reserved for the following Definitions made in "C Programming Languages"? "Unsigned Char", "Unsigned Short", "Unsigned Int" and "Double".

d) With regard to the 4 way set associative mapping cache (byte addressable memory); the size of the cache is 16KByte, the size of one Cache block is 32Byte and the size of the memory 256 Kbyte. What will be the size of the TAG field and the Set field (in bits)? Justify your answer. (3+4+3) [CO4]

8.a) An approximate specification of a Toshiba P300 Hard Drive (HDWD130 3.5") is given below.

No of Surfaces = 6
Individual Sector Size = 4096 byte
No of Sectors per track = 256
Average No of tracks per surface = 345078
Rotational Speed = 7200RPM
Maximum seek time = 20ms
Average seek time = 10ms
Track-to-track seek time = 2ms

What is the capacity of the Disk?

b) With respect to the disk mentioned above, what will be the total time required to read the entire disk one cylinder at a time? [Assume that the starting position of the Read/Write Arm is at outer most track]

c) If 6 disks (of 1.5TB each) are arranged in a RAID configuration of Level 0, 1, 4, 5 and 6 successively; what will be the total usable capacity for each of these configurations? Justify your answer. (3+4+3) [CO4]

9.a) Draw 2D Mesh Network of dimension 2, 3 and 4. For each case compute Diameter and Bisection width.

b) Illustrate the differences between UMA and NUMA architecture. (5+5) [CO5]

10.a) With proper numerical examples, explain the concept of Speedup, Algorithmic Scalability and Architectural Scalability.

b) With proper examples, show how Sorting can be done in parallel. (5+5) [CO5]