Ref. No.: Ex/ET/PE/B/T/424J/2024

Bachelor of Engg. (Electronics and Telecommunication Engg.) Exam., 2024
(Final Year, 2nd Semester Examination, 2024)

Introduction to ARM7TDMI Architecture

(Elective Paper #2)

Time: Three Hours Full Marks: 100

Answer ALL the Questions

(All Parts of the same question must be answered at one place only)

Module I (CO1)

1. (A) (a) ARM has incorporated ___________ ___________ __________within the Processor so that software engineers can view what is happening while the Processor is executing code.
(b) The ARM Processor has ________ registers assigned to a particular task or special functions, and they are ____________
(c) The ARM core uses the register, ____________ to monitor and control internal operations; this register is divided into _______ fields.
(d) There are _______ Processor mode in total; System mode is a special version of user mode that allows full read-write access to the ___________
(e) EmbeddedICE Macrocell is the _________ _________ built into the Processor that allows Breakpoints and Watchpoints to be set. (5X2=10 Marks)
(B) With suitable Figure, illustrate the use of Pipeline with Program Counter, PC, and other characteristics of the Pipeline that are worth mentioning. (5)
(C) How many types of Memory Management Hardware that the ARM core supports? Explain in brief about the same. (5)

Module II (CO2)

2. (A) (a) The Data Processing Instructions manipulate data _______ ________. Most Data Processing Instructions can process one of their operands using the _________ __________.
(b) Let (r0) = 0x00000000; (r1) = 0x00000005. After the execution of the instruction, **ADD ro, r1, r1, LSL #1** What will be (r0) and (r1)?
(c) Let (r1) = 0b1111 and (r2) = 0b0101. After the execution of the instruction, **BIC r0, r1, r2** What will be (r0)?
(d) The Pre-conditions are as follows: Mem32[0x9000] = 0x12345678; (r0) = 0x00000000; (r1) = 0x11112222; (r2) = 0x000090000; What will be the contents of these Memory location and the registers, after the execution of the instruction, **SWP r0, r1, [r2]** ?
(e) The LDR pseudo-instruction either inserts an _______ or ______ instruction to generate a value (if possible), or generates an LDR instruction with *pc-relative address* to read the constant from a ________ _________ - a data area embedded within the code. (5X2)

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(B) Write an ARM Assembly Language Program (ALP) to find the sum of **3X + 4Y + 9Z**, where X = 2, Y = 3, and Z = 4. (10)

Module III (CO3)

3. (A) (a) On Average, a Thumb implementation of the same code takes up around ____________ less memory than the equivalent ________ implementation.

(b) In the THUMBv2 architecture used in the ARMv5TE architecture, only the *Branch relative* instruction can be __________ executed.

(c) THUMB REGISTER USAGE : Only the registers ____________ are fully accessible. The registers ____________ are only accessible with MOV, ADD, or CMP instructions.

(d) This example shows a Thumb ADD instruction.
Pre-Conditions are : cpsr = nzcvIFT_SVC; (r1) = 0x80000000 (r1) = 0x10000000.
What will be (r0) and cpsr, after the execution of the instruction
ADD ro, r1, r2 ?

(e) Indicate the operation performed when the Thumb instruction, **CMN Rn, Rm** is executed. (5X2)

(B) The Pre-conditions are : (r1) = 0x00000001, (r2) = 0x00000002, (r3) = 0x00000003, (r4) = 0x9000. **Write the Thumb instruction** that saves (r1), (r2), and (r3) to memory addresses 0x9000 to 0x900c and also update the base register r4 (5)

(C) List the specific characteristics of Thumb Stack Instructions. Show with example, how the Thumb Stack instructions provides support for subroutine entry and exit. (5)

Module IV (CO4)

4. (A) (a) For ARM Processor, a number of Peripheral are added ________________ so as to make it a 'Microcontroller Unit (MCU)'.

(b) The number and kind of peripherals needed depends on the application, but there are some peripherals which are more or less a standard feature in some MCUs, examples of such Peripherals are ____________, ________________, __________

(c) For LPC2146/48 only, an ______ SRAM block intended to be utilized mainly by the USB, can also be used as a general purpose RAM for data storage, and code storage and execution.

(d) For LPC214x series of MCU, the total memory space is _________. It is a "___________________________" in which peripherals and memory share the same memory space.

(e) There are two ways of resetting : A Hard Reset using the _______ _________ reset pin, and a Soft Reset on account of _________ . __________. (5X2)

(B) Name the Low Power Modes available for LPC214x MCU and briefly explain the same. (5)

(C) How many Buses with different Protocols and Speeds have been defined for the different kind of Peripherals on-chip? Explain with a suitable Figure. (5)

Module V (CO5)

5. (A) (a) In LPC2148 MCU, _____ Pins of Port 0 can be used as general purpose bi-directional digital I/Os, while the Port 0 Bit ______ provides digital output function only.

(b) The purpose of the 'Pinselect' Block is to configure the pins to the __________ function. This acts like a __________.

(c) For any Pin, the bit configuration '_ _ ' of the corresponding Pinselect Register bits Program the Pin to act as a General Purpose I/O Pin.

(d) (i) To make Lower 16 GPIO pins to be the output pins, Then (IODIR) = ___________

(ii) To send zeros to all these pins, then (IOCLR) = _________________

(B) Write an Embedded C Program for the LPC214x MCU, to generate a square wave at the GPIO P1.16. Explain the configuration of the all the SFRs – Special Function Registers associated with this Port bit. (5)

(C) Explain the various SFRs associated with Timer0 with the simplified Block Diagram Illustrating the operation of the Timer unit. (5)

CO1: Illustrate the architecture of the ARM7TDMI Processor (K2, A1)
CO2: Understand the Instruction set of ARM Processor and write Assembly Language Program (ALP) (K2, K3, A2)
CO3: Compare and Analyze the advantages of ARM Thumb Instruction Set (K4, A2)
CO4: Describe the ARM Processor as a Microcontroller Unit with appropriate On chip Peripherals (K2, K4, A1)
CO5: Understand and write the Peripheral programming in C language(K2, A3)