Ref : Ex/ET/PE/B/T/414/C/2024

BETCE 4th Year, 1st Semester Examination 2024

Subject: Electronic Design Automation (Elective paper)

Time : 3hrs **Full Marks: 100**

Answer all questions from Q.1to Q.5. Each Question(Q.1 –Q.5) carries two options

Answer all the part of the question in same place. Different part of question at different sections will carry no marks.

All the programme should use proper syntax. Any kind of syntax error (semicolon , comma error, mismatch in identifier, wrong statement etc.) will carry no marks

Q.1A **8+6+3+3=20**

a. Write and explain briefly the steps of VLSI design cycle.

b. Explain the flow of logic design with figure and how technology mapping is carried out

c. Explain the significance of component library

Or

Q. 1B **6+6+8=20**

a. Explain the differences between validation and verification?

b. Explain the difference between Full custom and semi-custom design.

c. What is logic synthesis and how it is carried out, Explain with diagram.

Q.2A **10+5+5=20**

a. Write the code for resolution function and its Output for multiple signal driver assignment inside a data flow statement

b. What are the output of signal driver inside the process statement for inertial and transport delay

Or

Q.2B **10x2=20**

a. Write a VHDL code of a two bit magnitude comparator using data flow statement. Draw the gate level circuit

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b. Suppose a factory has a VAT with a sensor that output 1 when the VAT is empty, 0 otherwise. The VAT also has a pump to empty it and a control switch to active the pump. Devise a circuit that turns the pump on when the switch is set to activate the pump and the VAT is not empty. Design the code using VHDL behavioral model for the circuit you have drawn.

Q. 3A **10x2= 20**

a. Write a VHDL code for 4 bit parallel adder.

b. Write VHDL code for a mod 10 counter

Or

Q.3B **10x2= 20**

a. Write a Test bench of 4 input XOR gate. Also write the main programme of the XOR gate.

b. Write a VHDL programme for edge triggered master slave J- K flip flop.

Q. 4A **7+7+6=20**

a. How zero bias threshold voltage is modeled in SPICE level 1? Draw clear diagram of equivalent circuit of MOSFET for AC noise analysis

b. Write down the advantages and disadvantages between Empirical model and Physical model

Or

Q. 4B **5+5+10=20**

a. What are the drawbacks of scaling of interconnects?

b. What are the different components in Power dissipation characteristic?

c. Explain the condition of MOSFET gate capacitance, Device density, Power Density, Power Dissipation, Intrinsic Gate delay and Saturation current for constant field scaling?

Q.5A **5+5+5+5= 20**

a. What are the designable and noise parameters? Explain with an example of inverter circuit.
b. Draw the PVT corner diagram and explain.
c. What are the front end line corner parameters in timing corner?

Or

Q.5B

4+6+10 = 20

a. Briefly explains ANOVA and justifies the usage of ANOVA in Surface model

b. Draw the flowchart to generate response surface model (RSM) in comparison to SPICE model. Write down the multi variable equation for RSM with inner products.

c. In the following circuit X_4 has a s-a-0. For a test vector 1001 that detects error findout stage outputs without and with fault.