Ref. No. : Ex/ET/PC/B/T/413/2024

Name of the Examinations: B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

FOURTH YEAR FIRST SEMESTER – 2024

Department of Electronics and Telecommunication Engineering, Jadavpur University

Answer question no1 which is compulsory and any five questions from the rest (from Q2 to Q9).

The figures in the right hand margin indicate marks. *Symbols carry usual meaning.*

Time: Three hours Subject: VLSI Design and Algorithms Full Marks: 100

Q1. Choose the correct answer(s) out of four given answers [0.5x10 = 5]

(i). Load Capacitance in CMOS inverter is function of:

(a) fan-out, wire length & transistor size (b) fan-out, frequency & transistor size

(c) How often, on average, do wires switch? (d)none of a, b or c

(ii). Find the percentage reduction in the channel length if the bias voltage V_{DS}= 5V and V_{SB}= 0V for a channel length of 3.0 μm.

(a) 35.38% (b) 39.67% (c) 37.37% (d) 41.47%

(iii). Another component of leakage currents which occurs in CMOS circuit is the subthreshold current, which is due to:

(a). carrier diffusion between the source and the drain region of the transistor in weak inversion

(b). carrier diffusion between the source and the drain region of the transistor in strong inversion

(c). carrier drift between the source and the drain region of the transistor in weak inversion

(d). carrier drift between the source and the drain region of the transistor in strong inversion

(iv). Shot circuit power dissipation(in CMOS inverter) , Psc is eliminated

(a). If $V_{DD} < V_{THn} + |V_{THp}|$, (b). If $V_{DD} < (V_{THn} - |V_{THp}|)$,

(c). If $V_{DD} > (|V_{THp}| + V_{THn})$, (d). none of the a, b or c

(v). When the uncertainty principle is considered, it is not possible to locate a photon in space more precisely than about one wavelength. Consider a photon having wavelength 1μm and determine the uncertainty in the energy of photon. (a). 0.192eV , (b). 0.198eV , (c). 0.164eV , (d). None

(vi). For the n- channel enhancement type MOSFET of Fig A gate current is negligible, I_{DON} = 10mA and V_T = 4V. If R_S = 0 , R_1 = 50KΩ , V_{dd}= 15 V, V_{GSQ} = 3V, and V_{DSQ} = 9V. Determine R_2

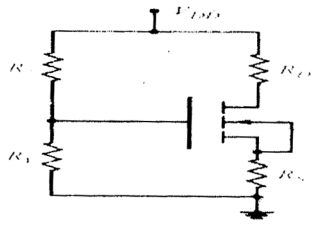

Fig. A

(a) 200 KΩ (b) 440KΩ (c) 225KΩ (d) 294KΩ

(vii). In a charge sharing circuit shown in Fig.B, Q_T during switched on condition of transmission gate depends on

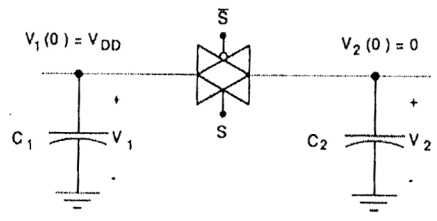

Fig. B

(a). C_2 and C_1 (b). C_2 (c). C_1 (d). does not depend on C1 and C2

(viii): The built in potential in a *p-n* junction increases with
(a) band gap energy of the semiconductor employed (b) fall in temperature
(c) doping levels of two sides (d) all of the above factors.

(ix). In active load nMOS inverter :
a). load transistor is depletion type and switching transistor is enhancement type
b). load transistor is enhancement type and switching transistor is depletion type
a). load transistor is depletion type and switching transistor is also depletion type
d). load transistor is enhancement type and switching transistor is also enhancement type

(x). If donor concentration is doubled in a p^+-n junction with all other parameters remaining unchanged, the Junction
capacitance, Built-in potential and Breakdown voltage for the resulting junction respectively
(a) increases, decreases and decreases (b) increases, increases and decreases
(c) increases, decreases and increases (d) increases, increases and increases

Q2(a). Why low power has become an important issue in the present day VLSI circuit realization?
(b) Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.
(c). What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?
(d). What is noise margin? Find out the noise margin from the actual characteristics of an inverter. 3+ 7 +5+4=19

Q3.(a) How one nMOS and one pMOS transistor are combined to behave like an ideal switch?
(b) What is glitching power dissipation? Explain with two examples how can it be minimized?
(c) List various sources of leakage currents , Briefly discuss various mechanisms responsible for this leakage current? 5 +6 + 8 = 19

Q4 (a). With the help of an example explain how gray coding helps to reduce power dissipation?
Q4(b).Prove that the charging of a capacitor C in *n* steps to a voltage Vdd instead of a conventional single-step charging reduces the power dissipation by a factor of *n*.
(c) Implement two-input(i) XOR and (ii) NOR gates with GDI logic. Explain their operations. 6+5+ (4+ 4)= 19

Q5(a) How is a CMOS inverter different from a resistive load inverter? Which is preferred and why?
(b). For inverter design, why depletion load n-MOS inverter is preferred?
(c). What is pass transistor? Write its advantages and disadvantages. Realize a NAND and a XOR Gates using Pass transistors and explain their operation. 4+ 2 + 13 = 19

Q6(a) What are different power dissipations in a CMOS circuits? Write the names of different parameters that control those power components. Explain how those parameters can be adjusted to reduce various power dissipation
b). Describe with necessary diagram, how will you reduce the propagation delay of an inverter? 15 + 4 = 19

Q7(a) Explain pseudo and Ganged CMOS logic. Realize some (two for each type) Logic functions using them.
b). Using equivalent NOT gate, drive the threshold voltage of a two-input NAND gate.
c). Describe single-rail and dual –rail logic circuits 10 +6+3 = 19

Q8 Give the justification with proper explanation and diagram if any (related to Low power VLSI) for the following comments:
i). "Minimize activity on long bus"
ii). "Dynamic Power Consumption is Data Dependent"
iii). "Use reduced supply voltage in sleep mode."
IV). "Low Vth for speed critical circuits"
V). "Lost performance can be compensated by parallelism" 3+4+4+4+4 = 19

Q9 (a) Why NAND is preferred over NOR?
(b) Write notes on any four:
(i) Transient Electronics, (ii) Organic Semiconductors , (iii) ASIC
(iv) Microfluidic Biochips and their applications, (v) Nonthreshold logic
(vi) Double Pass Logic(DPL) 3+ 4x4 =19