B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR FIRST SEMESTER SUPPLEMENTARY EXAM - 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 hours **Full Marks: 100**

Answer any five questions

1. a) State and explain Amdahl's law. **3**
   b) Using this law obtain an expression for performance improvement using a particular feature. **4**
   c) Suppose 50% of a calculation can be parallelized. Find the maximum speedups that can be achieved with 10, 100, 1000 and 10000 processors respectively. Ignore communication overhead among the processors. State the importance of your result. **8+2**
   d) What does CUDA stand for? State its utility. **1+2**

2. a) Write the CPU performance equation and properly explain all the terms involved in this equation. **2+3**
   b) Define a performance measure which is alternative to execution time. Discuss some potential advantages and disadvantages of this measure. **2+3**
   c) Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s., while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s. **5+5**
   i) Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
   ii) How the above performances will be affected if clock cycle time is doubled?

3. a) Explain different addressing modes in MIPS with examples (instructions follow respective modes). **10**
   b) Explain what is meant by *Stored Program Concept* in MIPS programming. **2**
   c) Write MIPS code to perform: C[i] = A[i] + B[i], where i = 1, 2, …, 100. Assume that the variable *i* is stored in $s1 and the constant 100 is stored in $s2. Further assume that the base addresses of the arrays A, B, and C are stored in $s3, $s4 and $s5 respectively. **8**

4. a) Show the IEEE 754 binary representation of 0.25_{ten} in single precision. **4**
   b) Draw a flowchart for multiplying two 4-bit binary numbers. **4**
   c) Show a block diagram for multiplying two 4-bit binary numbers. **4**
   d) Show step-by-step multiplication of 4_{ten} by 2_{ten} using the flowchart in b) and the block diagram in c). **8**

5. a) What is an ALU? **2**
   b) Design a step-by-step 32-bit ALU which can realize *Addition, Subtraction, AND, OR, NOR* and *set-less-than* operations. **8**
   c) Differentiate between a ripple carry adder and a carry-lookahead adder. Compare their performance for 64-bit addition. **2+3**
   d) Briefly explain how a carry-lookahead adder can achieve faster addition. **5**

6. a) Draw a neat schematic showing the basic implementation of a processor for MIPS subset. Clearly discuss the roles of the basic blocks in your figure. **3+7**
   b) Differentiate between RISC and CISC processors with two examples from each class. **3+2**
   c) Discuss how you can implement MIPS R-format instructions in a processor. **5**

7. a) What is a cache memory? Differentiate between direct mapped, 2-way set associative and fully set-associative caches. **2+8**
   b) Consider the following sequence of block addresses: 8, 8, 4, 0, 0, 6, 6, 6, 4. Compare the performance of three small caches each consisting of four one-word blocks – a direct mapped, a 2-way set associative and a fully set-associative. **10**