BACHELOR OF ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR FIRST SEMESTER SUPPLEMENTARY EXAMINATION, 2024

Analog CMOS Design and Technology

TIME: **3 HOURS** FULL MARKS: **100**

Answer ALL the four Segments below
(All parts of the same question must be answered together)

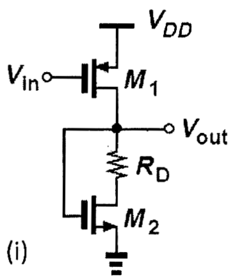
Any approximation used in solving problems need to be properly justified

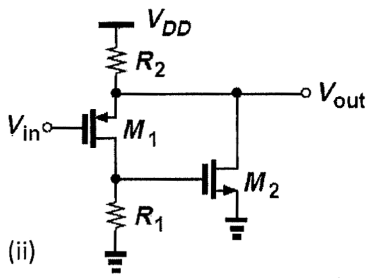
SEGMENT – I (*Answer any ONE question*) [CO1]

Q1.a) Discuss the effect of the following on the threshold voltage of a MOSFET: (i) increase in substrate doping density, (ii) increase of ambient temperature, and (iii) reduction of gate-oxide thickness. 6

b) Compare the various performance aspects of BJT and MOSFET? 4

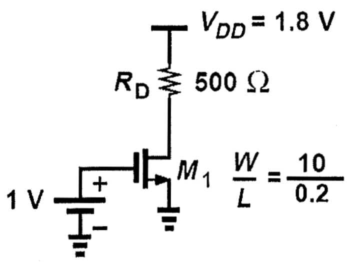
c) Construct the low-frequency small-signal model of the following circuits (i) and (ii). Consider $\lambda \neq 0$ and $\eta = 0$. 10





Q2.a) Draw the small-signal model of MOSFET including the internal capacitances. 5

b) For the following circuit, determine the minimum possible value of the supply voltage so as to keep the transistor in saturation region. Assume $\lambda = 0$, $\mu_n C_{ox} = 250\ \mu A/V^2$, and $V_{TH} = 0.6$ V. 5

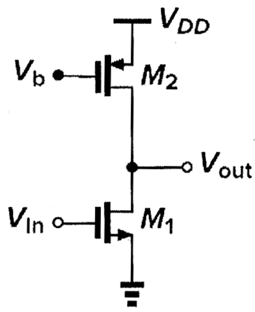


c) Derive the small-signal expressions of (i) transconductance and (ii) output resistance of a common-source amplifier with source degeneration. Do not neglect channel-length modulation and body effect. 10

SEGMENT – II (*Answer any TWO questions*) **[CO2]**

Q3.a) Draw and briefly discuss the advantages of a cascode structure. 5

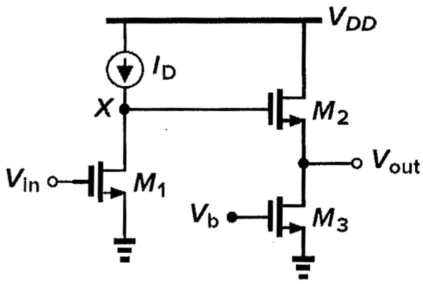
b) Considering both *thermal* and *flicker* noise, derive the expression of the output voltage noise spectrum for the following common-source amplifier. Hence find the rms noise voltage referred to the input terminal. 10



c) Discuss how distortion and noise are generated in an analog circuit. 5

Q4.a) Draw a representative layout for ensuring matching in a 1:4 current mirror, clearly indicating the MOSFET terminals and the different layers as utilized. 10

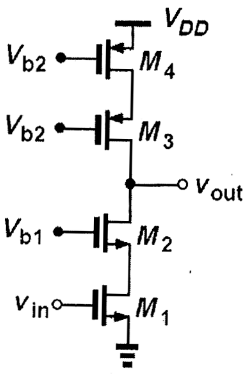
b) For the following circuit, derive expressions of: (i) low-frequency voltage gain (for λ and $\eta \neq 0$), (ii) permissible minimum level of voltage swing at the node X, and (iii) maximum tolerable swing of V_{out}. 10



Q5.a) Discuss on the input refereed offset of an opamp. 4

b) Draw the topology of a Telescopic cascode opamp. 4

c) For the following amplifier, quiescent current = 0.25 mA, $(W/L)_1 = (W/L)_2 = 30$, and $(W/L)_3 = (W/L)_4 = 50$. Given, $\mu_n C_{ox} = 100\ \mu A/V^2 = 2\mu_p C_{ox}$, $\lambda_n = 0.1\ V^{-1}$, $\lambda_p = 0.15\ V^{-1}$, and $V_{THn} = 0.5\ V = |V_{THp}|$. Calculate the (i) voltage gain and (ii) maximum permissible voltage swing supported at the output. 12



SEGMENT – III (*Answer any ONE question*) **[CO3]**

Q6.a) Describe the various steps of photolithography. 10

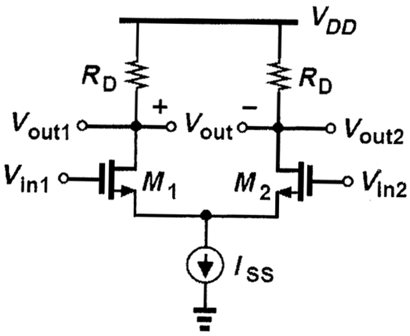
b) Discuss the important steps involved in a typical CMOS process flow for fabricating NMOS and PMOS FETs on wafer, with representative schematics. 10

Q7.a) Explain the short channel effect of *velocity saturation.* 10

b) Discuss two commonly used methods for the doping of semiconductors. 10

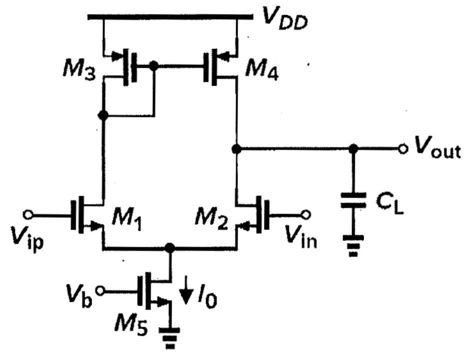
SEGMENT – IV (*Answer any ONE question*) **[CO4]**

Q8.a) (i) Design the diff-amp for a power consumption of 4 mW and V_{OV} of 100 mV. (ii) For input common-mode of 1 V, find the value of R_D to place M_1 and M_2 at the edge of saturation. (iii) Find the voltage gain obtained from the resulting design. Assume $V_{DD} = 2$ V, $\mu_n C_{ox} = 300\ \mu A/V^2$, $V_{TH} = 0.5$ V, $\lambda = 0$ and $\eta = 0$. 12



b) If a fabrication induced mismatch of 5% occurs between the two R_D resistances in the above circuit, derive the (i) expression and (ii) value of resulting CMRR. Consider that the current sink I_{SS} is realized by a suitably biased NMOSFET having $\lambda_n = 0.1\ V^{-1}$. 8

Q9.a) Find the values (in Hz) of 3-dB BW and GBW of the below OTA. Given $V_{DD} = 2$ V, $V_{THn} = 0.5$ V $= |V_{THp}|$, $\mu_n C_{ox} = 200\ \mu A/V^2 = 2\mu_p C_{ox}$, and $\lambda_n = 0.1\ V^{-1} = 0.5\lambda_p$. Also, $(W/L)_{1,2} = 20$, $(W/L)_{3,4} = 40$, $C_L = 3$ pF and $I_0 = 0.2$ mA. 10



b) Determine the expressions and values of the input common mode range (both $ICMR_+$ and $ICMR_-$) of the above amplifier. Consider $V_{OV,5} = 100$ mV. 10