# B. E. Electronics and Telecommunication Engineering 2nd Year 1st Semester Examination- 2024

## Digital Logic Circuits

**Time: 3 Hours** **Full Marks: 100**

*Answer all the parts of a question in the same place*

**Module-I [Answer question no. 1 (1×10) = 10] CO1**

1. a) Convert $(1E0.2A)_{16}$ into Decimal
   b) Find the decimal equivalent of the binary number 10001110 expressed in the 2's complement format.
   c) Perform the subtraction using 2's complement method 00001100-11110111
   d) Write one advantage and disadvantage of 1's complement method.
   e) How do you convert gray code numbers to corresponding binary numbers?

(2+2+2+2+2)

**Module-II [Answer *any three* questions (3×10) = 30] CO2**

2. a) What do you mean by decoder? Write the truth table for a BCD-to-Decimal decoder.
   b) Design the gate level circuit for a 1:4 De-multiplexer with active high outputs and briefly explain its operation.

(5+5)

3. Write the output expressions for a 4-bit carry look-ahead adder. Draw the circuit using logic gates. Compare the propagation delay of 4-bit carry look-ahead adder and 4-bit ripple-carry adder.

(4+5+1)

4. a) What do you mean by register and universal shift register?
   b) Draw a 4-bit serial-in and serial-out shift register circuit. Also draw the waveforms at the output of each stage for an input sequence 111010 and which is synchronous with the clock input.

(4+6)

5. a) Draw a D-type positive-edge triggered flip-flop using NAND gates only and briefly explain its operation when D =1 and clock changes from 0 to 1.
   b) What do you mean by strobing time in a counter? Determine the maximum clock frequency of an n-stage synchronous serial counter and synchronous parallel counter.

(6+4)

**Module-III [Answer *any four* questions (4×10) = 40] CO3**

6. a) Draw the circuit diagram of a 3-input XOR gate using minimum number of 2:1 multiplexers and single NOT gate.
   b) Implement the following four Boolean expressions using three half adders only.

   D = A⊕B⊕C
   E = A'BC + AB'C
   F = ABC'+ C(A'+B')
   G = ABC

   c) Simplify the Boolean expression $xy + y'z + xz + xyz$

(4+4+2)

7. a) For the following Boolean function, find the simplified expression using Quine McClusky method

   F (A, B, C, D) = Σ m (3, 4, 9, 13, 14, 15) + Σ d (5, 7)

   b) Implement a full adder circuit using minimum number of two input NOR gates.

(6+4)

8. Design a Mod-6 synchronous down counter using minimum number of J-K flip-flops and logic gates. The counter resets if an unused state is reached. Also sketch the corresponding counter circuit.

(8+2)

9. a) What do you mean by logic families? Write the advantages of TTL logic family. Write the merits and demerits of CMOS logic family.
   b) Draw a 2-input XOR gate using CMOS logic.

(6+4)

10. a) A logic function F (A, B, C, D) = Σm (0, 2, 3, 5, 6, 7, 8, 9) and Σ d (10, 11, 12, 13, 14, 15). Find the simplified SOP expression of F. Design the circuit using minimum number of two input NAND gates.
    b) Verify that XOR operations are commutative and associative; on the other hand, NOR operations are commutative but not associative.

(6+4)

**Module-IV [Answer *any two* questions (2×10) = 20] CO4**

11. a) Explain the operation of a 4-bit binary weighted resistors Digital to Analog Converter (DAC) with a neat sketch. Also write the limitations of binary weighted resistors DAC.
    b) An 8-bit DAC has a resolution of 10 mV/bit. Find the analog output voltage for inputs: i) 10001010 ii) 01010110

(7+3)

12. a) Explain the working principle of successive approximation ADC with a neat block diagram.
    b) A system employs a 16-bit word for representing the input signal. If the maximum output voltage is set for 2 V, calculate the resolution of the system.
    c) What are the merits and demerits of tracking type ADC over counter type ADC?

(6+2+2)

13. a) The output of a 3-stage free running up ripple counter is connected to a 3-bit DAC. Draw the corresponding DAC output waveform.
    b) Draw the logic diagram of a negative edge-triggered Jhonson counter which will divide input by 10. Write the number of unused states.
    c) Draw the block diagram of a 3-digit digital voltmeter based on dual-slope ADC. Label each block of your diagram.

(3+3+4)