B. E. Electronics and Telecommunication Engineering 2nd Year 1st Semester Supplementary Examination- 2024

Digital Logic Circuits

Time: 3 Hours **Full Marks: 100**

Answer all the parts of a question in the same place

Module-I [Answer question no. 1 (1×10) = 10] CO1

1. a) Given that $(16)_{10} = (100)_b$, find the value of b.
   b) Convert $(A0F9.0EB)_{16}$ to decimal.
   c) Convert $(756.603)_8$ to Hex.
   d) Convert (110101.10101011) to Octal.
   e) Subtract 14 from 46 using the 8-bit 2's complement arithmetic.

(2+2+2+2+2)

Module-II [Answer *any three* questions (3×10) =30] CO2

2. a) Write the truth table of a full-subtractor. Draw the logic diagram of a full-subtractor using 2-input NAND gates only.
   b) What is a parity generator? Draw a 4-bit even parity generator circuit.

(6+4)

3. a) What is a master-slave flip-flop? Describe the working principle of a master-slave J-K flip-flop.
   b) How J-K flip-flop must be connected to function as a divide-by-two circuit? How many J-K flip-flops are required to design a divide-by-64 circuit?

(7+3)

4. a) What do you mean by set-up time and hold time?
   b) Draw the logic diagram of a 4-bit twisted ring counter using J-K flip-flops and write corresponding sequence table.
   c) How do you test the lock-out problem of a counter?

(3+5+2)

5. a) Write the truth table of a 2-bit magnitude comparator circuit, draw its gate level circuit and explain its operation

(4+4+2)

Module-III [Answer *any four* questions (4×10) = 40] CO3

6. a) Simplify the Boolean expression F (w, x, y, z) = Π M (2, 8, 9, 10, 11, 12, 14) and implement it using minimum number of universal logic gates.
   b) Prove that $w'y'z' + wz + y'z + xyz = w'y' + wz + xz$

(4+3+3)

7. a) Obtain the set of essential prime implicants for F (A, B, C, D) = Σm (1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15) using Quine-McClusky method and implement the simplified expression using minimum number of basic logic gates.

(7+3)

8. a) Draw the gate level circuit of a 2-to-4 lines decoder with active low outputs.
   b) Implement the following multiple outputs combinational logic circuit using a 4-to-16 lines decoder.
   $F_1 = \Sigma m(1,2,4,7,8,11,12,13)$
   $F_2 = \Sigma m(2,3,9,11)$
   $F_3 = \Sigma m\ (10,12,13,14)$
   $F_4 = \Sigma m\ (2,4,8)$

(4+6)

9. Design a synchronous BCD counter using minimum number of J-K flip-flops and logic gates. Also sketch the corresponding counter circuit.

(8+2)

10. a) Define propagation delay and noise margin for a logic family. Write the advantages of CMOS logic family.
    b) Draw a 2-input XNOR gate using CMOS logic.

(6+4)

Module-IV [Answer *any two* questions (2×10) = 20] CO4

11. a) Explain the operation of a 4-bit R-2R ladder type Digital to Analog Converter (DAC) with a neat sketch.
    b) An 8-bit DAC produces V_{out} = 0.05 V for a digital input of 00000001. Find the full-scale output. What is the resolution? What is the analog output voltage for input 00101010?

(7+3)

12. a) Draw a 3-bit comparator type ADC circuit to represent output in sign magnitude form and explain its operation.
    b) An 8-bit successive approximation type ADC is driven by a 2 MHz clock signal. Find the required conversion time.
    c) What are the merits and demerits of successive approximation type ADC over comparator type ADC?

(6+2+2)

13. a) Draw a 5-stage ring counter circuit. Write the merits and demerits of the counter circuit.
    b) The output of a three stage Johnson counter is fed to a DAC. Assume that the counter initially at reset state. Draw the waveform at the DAC output.
    c) Draw a simplified logic diagram of a 12-hour digital clock and briefly explain its operation.

(3+3+4)