B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
SECOND YEAR SECOND SEMESTER EXAM 2024
DIGITAL CIRCUITS AND SYSTEMS

Time: Three Hours | Full Marks: 100

Answer all the sub-parts of a question altogether

Module 1 (CO1)

Answer any 4

1. a) Design a hazard-free circuit to implement the following function.

F (A, B, C, D) = Σm (1, 3, 4, 5, 6, 7, 9, 11, 15).

b) Minimize the following Moore machine using the implication table

PS	NS		Output
	X=0	X=1	z
A	D	C	0
B	F	H	0
C	E	D	1
D	A	E	0
E	C	A	1
F	F	B	1
G	B	H	0
H	C	G	1

c) Design a synchronous sequential circuit that takes a one-bit stream $x_0x_1x_2$ ... as input, and outputs a one-bit stream $y_0y_1y_2$ .... The i-th output bit y_i is 1 if and only if the four most recently read input bits $x_i{-}3x_i{-}2x_i{-}1x_i$ have odd parity. Here is an example. At the beginning of the input, four bits are not read. Assume that the missing bits are 0 (that is, $x_{-3} = x_{-2} = x_{-1} = 0$).

Input: 0100110100111010...

Output: 0111000101001110...

d) Design a 4-bit binary ripple counter (asynchronous) that has one count-enable input and one control input. If the control input is 0, the counter increments by 1 modulo 16. If the control input is 1, the counter increments by 2 modulo 16. Use negative-edge triggered T flip-flops. The count-enable input is (negative) edge-sensitive, whereas the control input is level-sensitive.

e) Design a Mealy machine N that, given the output of M, produces the corresponding input for M. Specify the start state of N. (Treat M as a message-encoding circuit. Then, N is the corresponding message decoding circuit.)

5+5+5+5 = 20

Module 2 (CO2)

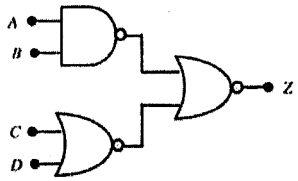
Answer any 4

2. a) Justify with an example – "Why Testing is Considered Difficult".

b) What is Built-In-Self-Test? Discuss the issues and benefits of BIST. Describe BIST architecture and its operation.

c) Consider a LFSR based pattern generator where the feedback network is a single XOR gate before the first stage. If the number of (feedback) inputs to the XOR is odd, is it possible for the LFSR to generate maximal length sequence? Justify or contradict.

d) Obtain the test faults in the following circuits using Boolean difference method:



e) Briefly describe the various Processes during Testing. Compare between Verification and Testing.

5+5+5+5 = 20

Module 3 (CO3)

Answer any 2

3. a) What is the difference between wire and reg? What is the difference between $monitor and $display. What is Verilog Module? Write a Verilog code of an 8-bit adder.

b) What are the advantages of using programmable logic over discrete digital logic ICs? Give two examples of where it would be more beneficial to use a PLD.

c) Give two examples of where it would not necessarily be beneficial to use a PLD over discrete digital logic ICs.

(3+3+1+3) +/ (5+5) + / (10) = 20

Module 4 (CO4)

Answer any 2

4. a) Draw and briefly explain 74121 single TTL.

b) Draw and briefly explain 74123 dual TTL.

c) By using 74122 and external components, design a retriggerable one-shot to circuit to produce a Pulse of 80 nano-sec after each trigger signal. Draw the Circuit and label all components. Show your calculations. 10+10 = 20

Module 5 (CO5)

Answer any 1

5. a) Implement a standard LFSR for the characteristic polynomial f(x) = x8 +x7 +x2 +1. Multiply the two numbers (23) and (-9) by using the Booth's multiplication algorithm. Multiply the two numbers (1 0 1 0) and (0 1 1 0) by using the Partial Sum Approach.

b) Briefly describe Booth's algorithm with a flowchart. Find BCD Addition of 974 and 599.

(4+3+3) / (8+2) = 10

Module 6 (CO6)

Answer any 1

6. a) Draw the structure of a 4096-bit ROM. Draw and briefly explain an SRAM sell using Six-transistor NMOS RAM Cell.

b) Draw and briefly explain an SRAM sell using CMOS RAM Cell. Draw the structure of Decimal to Binary diode-matrix encoder. (5+5) / (5+5) = 10