#### Ex/ET/PC/B/T/215/2024(S)

# B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING SECOND YEAR FIRST SEMESTER SUPPLEMENTARY EXAM - 2024

ANALOG CIRCUITS- I

Time: Three hours

Full Marks: 100

(All parts of the same question must be answered together)

## Module I [Answer any one (1×10=10)] CO1

| 1.  | <ul><li>a) Explain the working of negative clamper circuit. Draw the required waveforms.</li><li>b) Explain the working of series clipping circuit to clip the input sinusoidal signal above reference level. Draw the waveforms and transfer characteristics.</li></ul>   | [3+2]<br>[5]      |  |
|---|--|-------------------|--|
| 2.  | <ul><li>a) Draw full-wave rectifier circuit and explain its operation.</li><li>b) Find the approximate expression for ripple factor of half wave rectifier without capacitor filter.</li></ul>   | [2+4]<br>[4]      |  |
| Module II [Answer any one (1×10=10)] CO2  |  |                   |  |
| 3.  | a) Consider symmetrical square wave input applied to a low-pass RC circuit. Sketch the input and output waveforms and obtain the expression for maximum and minimum values of output voltage.  | [8]               |  |
|   | b) Explain low pass filter as an integrator.   | [2]               |  |
| 4.  | Describe the problem of uncompensated attenuator and find condition for perfect compensation.  Draw output waveforms for over, under and perfect compensation.   | [3+4+3]           |  |
| Module III [Answer any two (2×20=40)] CO3 |  |                   |  |
| 5.  | <ul> <li>a) What do you understand by transistor biasing? Draw load line on output characteristics and show operating point.</li> <li>b) For an emitter bias circuit, derive an expression for stability factors S<sub>Ico</sub>, S<sub>VBE</sub>, and S<sub>β</sub>.</li> <li>c) Calculate S<sub>Ico</sub>, S<sub>VBE</sub>, and S<sub>β</sub> for R<sub>C</sub> = 3.3kΩ, R<sub>B</sub> = 220kΩ, R<sub>E</sub> = 1kΩ, V<sub>CC</sub> = 10V, β = 150.</li> </ul> | [5]<br>[9]<br>[6] |  |
| 6   | <ul> <li>a) Explain the effect of coupling capacitances on voltage gain at low frequency.</li> <li>b) Consider npn BJT in common emitter configuration working with self bias, bypassed emitter resistance mode. Obtain expressions for input impedance, output impedance and voltage gain. Draw the small signal model(g<sub>m</sub>-r<sub>π</sub>).</li> </ul>   | [3]<br>[9]        |  |
|   | c) Determine voltage gain, input impedance and output impedance of a self bias, bypassed source resistance mode MOSFET amplifier with $R_{\rm D}$ =1 $k\Omega$ , $R_{\rm S}$ = 220 $\Omega$ , $V_{\rm DD}$ = 5 $V$ , $V_{\rm DS}$ = 2 $V$ , $V_{\rm GS}$ = 1 $V$ , Kn=1mA/ $V^2$ and $V_{\rm Th}$ =0.5 $V$ .   | [8]               |  |
| 7.  | <ul> <li>a) Write advantages and disadvantages of MOSFET amplifier over BJT amplifiers.</li> <li>b) The data sheet of N channel JFET gives the following details. I<sub>DSS</sub>=10mA and pinch off voltage</li> </ul>  | [4]               |  |
|   | of -4.8V. Determine i) V <sub>GS</sub> at I <sub>D</sub> =2.5mA and ii) transconductance, g <sub>m</sub> at this drain current. c) Explain Miller effect associated with CS mode FET amplifier with the help of small signal   | [3+3]             |  |
|   | model? Explain Cascode amplifier to avoid Miller effect.   | [5+5]             |  |

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### Module IV [Answer any one (2×15=30)] CO4

| <ul> <li>b) Explain origin of input offset voltage, input bias current of a practical op-amp.</li> <li>c) How do CMRR and Slew rate influence the performance of an op-amp?</li> <li>d) Explain a balanced differential amplifier using BJT</li> <li>a) Analyze the circuit diagram of an Instrumentation amplifier using op-amp. Derive the expression for the output voltage.</li> <li>b) The datasheet of Op Amp gives the following values. Open loop Gain= 175,000, commonmode gain =0.18 and slew rate= 0.5V/µs. Determine the CMRR in decibels.</li> <li>9. a) Define line and load regulation of a voltage regulator.</li> <li>b) Explain the short circuit protection circuit in a series voltage regulator.</li> <li>c) Draw and explain the output waveform of an integrator circuit for a triangular input.</li> <li>Module V [Answer any one(10)] CO5</li> <li>10 a) Design a Zener voltage regulator to provide regulated output voltage of 5.6 V for a variable load resistance that varies from 300Ω to 6kΩ. Zener diode parameters are I<sub>Zmin</sub>= 0.25 mA and P<sub>Z</sub>= 280mW. The input voltage is considered as constant at 15V.</li> </ul> | [3]           |
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|  | [5]           |
| b) Design an Op Amp circuit to get the output according to the given expression. VO =-   | £ 5.1         |
| [0.3V1+3V2+V3] where V1,V2 and V3 are the inputs to op-amp.  | [5]           |
| Design a Voltage divider circuit for a silicon transistor with hfe=100 and S≤8. The desired Q-   | Γ1 <b>Λ</b> 1 |
| point is $V_{CE}=5V$ , $I_{C}=1mA$ . Assume $V_{CC}=10V$ and $R_{E}=1k\Omega$ .  | [10]          |