Ref. No.: Ex/ET/PC/B/T/215/2024

B.E. Electronics And Tele-Communication Engineering Second Year

First Semester Exam, 2024

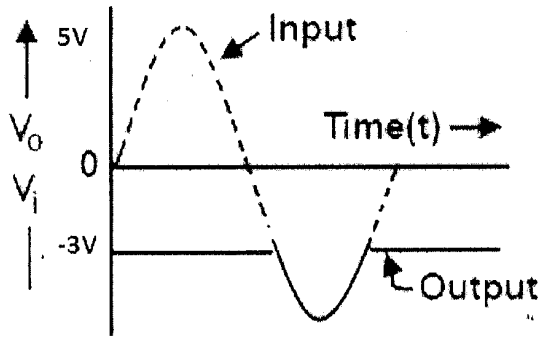
ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

(All parts of the same question must be answered together)

Module I [Answer any one (1×15=15)]

1. i. If a sine wave with V_{pp}=5V applied to the input of a half wave rectifier circuit
   a) Sketch the input and output voltage waveforms in the same scale. [2]
   b) Determine the conduction angle and the output DC voltage. Assume diode drop =0.5V. [4+4]
   c) Calculate the % load regulation. Given that the maximum load R_L=500Ω and dynamic resistance of the diode is 50 Ω. [2]
   d) Find the expression for DC voltage for a half wave rectifier with a capacitor filter. [3]

   ii.
   a) Classify clipper circuits and explain the circuit to obtain the following output. [2+4]



   b) Draw and explain a negative clamper circuit. [6]
   c) Draw a circuit to obtain a output of 4Vp where Vp is the peak value of the input. [3]

Module II [Answer any one (1×10=10)]

2. i. A step input of 5V is applied to a low pass RC filter.
   a) Sketch the output waveform. [2]
   b) Determine the expression for rise time. [4]
   c) Calculate the output voltage at t=2ms and t=5ms. The resistor R is 10 kΩ, and the capacitor C is 100nF. [4]

   ii. Draw a compensated attenuator circuit and explain perfect compensation, under compensation and over compensation conditions. [10]

[Turn over

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Module III [Answer any five (5×7=35)]

3. [5×7]

i. Explain the origin of instability of the operating point of a BJT amplifier. Define thermal stability factors associated with BJT biasing circuits.

ii. Determine the voltage gain of a CE amplifier with partially bypassed emitter resistance (draw). Given that V_{CC}=15V, R_1=36kΩ, R_2=15kΩ, R_C=3.6kΩ, R_{E1}=27kΩ and R_{E2}=1.5 kΩ.

iii. Draw and explain the frequency response of a CE amplifier.

iv. Draw a Darlington pair in CC mode and derive the expression for input and output impedances.

v. Draw the load lines of a source bias JFET circuit for two values of R_S and explain the effect of Rs on stabilizing the operating point.

vi. For a CS amplifier with E-mode MOSFET, find the expression for voltage gain with the help of small signal equivalent circuit using h-parameters.

vii. Determine the operating point of the JFET amplifier. R_D = 6.8kΩ, R_S = 2.7 kΩ, R_{G1} =9 MΩ, R_{G2}= 1 MΩ,R_L = 10kΩ,V_{DD}= 24 V and V_{GS} = - 3V.

viii. Explain Miller effect in CS amplifier. Draw and explain a circuit to avoid Miller effect.

Module IV[Answer any five (5×5=25)]

4. [5×5]

i. Write down characteristics of an ideal OP-Amp.

ii. Define offset voltage, bias current and CMRR of OP-Amp.

iii. Determine common mode gain of differential amplifier if the collector resistances of the two amplifiers are not equal.

iv. Draw a Schmitt trigger circuit and explain the output.

v. Calculate the close loop voltage gain of non-inverting amplifier considering finite open loop gain.

vi. Draw and explain a subtractor using Op-Amp.

vii. Draw and write down advantages of Instrumentation amplifier

viii. Draw circuit to obtain 5xy+2 at the output where x and y are voltages.

Module V[Answer any three (3×5=15)]

5 [3×5]

i. Draw and explain shunt voltage regulator.

ii. Write down the IC name of fixed and adjustable positive, negative voltage regulators. What are the functions of three external capacitances during working of such ICs?

iii. Explain Fold-back current limiting in a series voltage regulator.

iv. In LM317, determine the minimum and maximum regulated voltage. Given that I_{adj}=50μA, R_1=220Ω and R_2 is a 5kΩ pot.

v. Draw and explain a buck switching voltage regulator.