Ref No: **Ex/EE/5/T/311/2024**

BACHELOR OF ENGINEERING (ELECTRICAL ENGINEERING) THIRD YEAR FIRST SEMESTER EXAMINATION 2024

SUBJECT: - ELECTRICAL INSTRUMENTATION

Time:Three hours

Full Marks 100
(50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	Answer any FOUR questions. ***Two marks reserved for neat and well organized answer.***	
1.	(a) For an LVDT with fixed core, show that the direction of displacement of the core is conveyed by its phase information. Draw input and output waveform for different direction of displacement.	8
	(b) What is the residual voltage of LVDT? What are the causes of its appearance at the output?	4
2.	(a) Draw the phase compensating circuit of LVDT using RC network. Derive the condition of phase compensation.	8
	(b) Define sensitivity of LVDT. Show that the sensitivity increases when time constant of the RC network reduces.	4
3.	Draw a circuit for phase sensitive demodulation. Explain its operation with required waveform.	12
4.	Explain the operating principle of variable air-gap type capacitive displacement transducer with appropriate diagram and derivations. How is the effect of fringing of electric field is reduced?	8+4
5.	For an angular displacement capacitive sensor (i) How does the capacitance change when its area of overlap increases.	3
	(ii) If the radius of overlapping area increases, how does its sensitivity alter?	3
	(iii) What is the mechanically ganged arrangement of angular displacement sensor? What is the purpose of its use? Draw the arrangement and justify your comment.	6
6.	Derive the expression of capacitance for a variable air-gap transducer with composite dielectric. Obtain an expression of its sensitivity.	8+4

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B.E.E. (EVENING) 3RD YEAR 1ST SEMESTER EXAMINATION, 2024

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No. of Questions	PART-II	Marks
	Answer any three, 2 marks for well-organized answers	
1.	**Justify and/or correct the following statements with proper explanations:**	(4X4=16)
a)	Quantization error is inherent to all Analog to Digital converters (ADCs).	
b)	Proper probe design is required for oscilloscopes for proper signal representation.	
c)	*Lock-in-range* and *capture range* of a Phase locked loop (PLL) are same.	
d)	Phase locked loop (PLL) cannot be used for fractional frequency multiplication.	
2. a)	Explain the operation of time-base-generator for a Cathode Ray Oscilloscope (CRO)?	5
b)	Find the transfer function of a band pass filter with center frequency 10^3 rad/s. and bandwidth 100 rad/s with passband gain 6. Hence realize the active filter circuit using VCVS.	11
3. a)	What are ***Rounding off*** and ***Truncation*** type Analog to Digital converters (ADCs)?	4
b)	Explain the operation of 3-bit successive approximation type ADC with a flow chart.	7
c)	Obtain a 4-bit binary representation of an analog signal value of 10.75 V using successive approximation type ADC. Reference voltage is 12 V. Find out the conversion time in seconds. The clock frequency is 1kHz.	5
4. a)	The step size of a 4-bit Digital to Analog Converter (DAC) is 8 mV. An offset error of 0.2 mV exists in the DAC. If all zeroes represent 0V without this error, what outputs are produced for input code 10100 **with and without** this offset?	4
b)	Develop a linear model for Phase locked loop (PLL).	7
c)	Explain the operation of PLL as Frequency demodulator.	5
5.	Write short notes on any ***two***	(2X8=16)
a)	Representation of Offset and Linearity errors for ADC and DAC.	
b)	Storage Oscilloscope	
c)	Operation of a 3-bit R-2R ladder network based DAC	