Ref. No.: Ex/EE/PE/B/T/414D/2024(S)

B.E. ELECTRICAL ENGINEERING - FOURTH YEAR - FIRST SEMESTER SUPPLEMENTARY EXAMINATION, 2024

SUBJECT: - ADVANCED INSTRUMENTATION -I

Time: Three hours

Full Marks 100
(50 marks for each part)

Use a separate Answer-Script for each part

Question No.	PART I	Marks
	ANSWER ANY *TWO* QUESTIONS	
1. (a)	**Give a neat sketch of the architecture for a sigma-delta modulator type ADC and explain the working principle with the help of sketches for relevant spectra and mathematical derivations. Indicate the role of the digital decimator in the ADC.**	12+3
(b)	**Trace the sources of error in full Flash analog-to-digital converters.**	10
2. (a)	**Elucidate the motivation for electrostatic shielding of Rogowski coil current transducer. How such a shielding can be implemented and what is its effect?**	6+6
(b)	**Examine the possibility of using a Hall element as an open loop current transducer without any ferromagnetic core. How can the performance of the transducer be improved by introducing a ferromagnetic core?**	6+7
3. (a)	**Determine the expression for the frequency response of force-balance accelerometer Point out clearly the merit of this accelerometer compared to the open-loop varieties.**	10+5
(b)	**Explain the functioning of a PTAT sensor using two matched transistors.**	10

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Question No.	PART I	Marks
4.	Write short notes on any two of the following.	12 ½
(a)	Closed-loop variety of the Hall-effect current transducer.	+12 ½
(b)	PTAT sensor using a single transistor.	
(c)	Subranging ADC.	
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No. of Questions	PART-II	Marks
	Answer any two	**2X25=50**
1. a)	Draw a schematic of a digital vector voltmeter using synchronous detection technique. A phase-locked frequency synthesizer provides all internal references from a common reference source. Explain the principle of operation of such voltmeter.	10
b)	A Rough Set based decision rule generation system uses a real valued data table as given below. Generate the discretized decision table using maximal discernible heuristics. Show the optimum set of cuts.	15
2. a)	What is a lock-in-amplifier? Explain with a basic scheme.	5
b)	How can you employ digital synthesis technique in such a lock-in-amplifier for better performance? What are the importance of such amplifiers in instrumentation?	6+2
c)	A digital frequency synthesizer employs an 8 MHz crystal oscillator and gives a 128 step-sinusoid. Determine the maximum and minimum output frequency if the number of fractional bit is 3. Also find out the frequency control word for these cases.	4
d)	What are orthonormal bases in the context of Wavelet Transform?	3

Objects	Condition Attributes		Decision Attribute
	A	B	
U_1	0.75	5.0	0
U_2	1.25	3.5	0
U_3	2.2	5.0	1
U_4	0.75	2.25	1
U_5	1.8	1.0	0
U_6	1.25	3.5	1
U_7	1.25	2.25	1
U_8	2.2	1.0	1

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(50 marks for each part)

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e)	Samples of a signal is shown as $f = \{4, 4, 8, 8, 0, 0, 1, 2\}$. ↑ Find Wavelet coefficients after Haar Transform for the above signal. Show that energy does not change after Haar transform.	5
3. a)	How is the limitation of Fourier Transform overcome by Short Time Fourier Transform (STFT)?	3
b)	What are the shortcomings of STFT? Justify the application of Continuous Wavelet Transform (CWT) to overcome them.	4
c)	What is/are "*Continuous*" in Continuous Wavelet Transform?	2
d)	Explain the terms "*scale*" and "*translation*" in CWT. What is the importance of the factor $\frac{1}{\sqrt{\lvert s \rvert}}$ in CWT? (all symbols carry their usual meaning)	4+2
e)	What are the properties of a *mother-wavelet*?	4
f)	Write down the algorithm for computing Continuous Wavelet Transform of a one dimensional signal.	6
4.	Write notes on any ***two***	$(2 \times 12\frac{1}{2} = 25)$
a)	Wavelet Transform based denoising technique	
b)	Direct Digital Synthesis (DDS) based Frequency synthesizer	
c)	Different levels of sensor fusion	