B.E. ELECTRICAL ENGINEERING THIRD YEAR FIRST SEMESTER - 2024

Subject: PROGRAMMABLE LOGIC & MICROCONTROLLER

Time: Three hours | Full Marks 100 (50 marks for each part)

Use a separate Answer-Script for each part

PART I

Answer any FIVE:

1. Name different switching tehnologies used in PLD. Describe the structure and functionality of any one of the switch used in MOS memory device with proper diagram. 10

2. a) Develop a circuit by using PLA to implement the full adder. 5+5
   b) How does macrocell add to the versatility of a configurable hardware? Explain with example.

3. Discuss the different steps involved in simulation and synthesis in a typical CAD system. 10

4. a) What is JTAG cable? What is its role in context with device programming? Write the pin details of JTAG cable. 7+3
   b) What are the advantages of FPGAs over CPLDs?

5. Name different types of technologies adopted in FPGA logic blocks. Draw and explain a circuit diagram to implement the logic function $f = ab + \bar{c}$ using transistor pair logic in FPGA. 10

6. Describe with neat circuit diagram, the functionality of a commercially available CPLD chip. 10

7. Write a program in VHDL to develop an XOR gate. Write a testbench program to test it. Draw the timing diagrams for input and output signals. 10

8. How many different states are available as per IEEE standards in VHDL? Write down their names and symbols. Write their priority list. 10

Ref No: EX/EE/PC/B/T/316/2024

B. E. ELECTRICAL ENGINEERING 3RD YEAR 1ST SEMESTER EXAMINATION

SUBJECT: - PROGRAMMABLE LOGIC AND MICROCONTROLLER

Time: **Three hours**

Full Marks 100
(50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART II	Marks
1.	**(a)** (i) How do you recognize and differentiate a microcontroller from a set of available microprocessors?	6
	(ii) State key differences between a ROM and a RAM.	4
	OR	
	(b) Identify the correct option(s) and justify in favour of your answer:	5x2=10
	(i) Most of the microcontrollers with the state of the art technology is a (A) RISC processor of Princeton architecture (B) RISC processor of Harvard architecture (C) CISC processor of Princeton architecture (D) CISC processor of Harvard architecture	
	(ii) Flash memory of a processor is generally used to store (A) Data even when power is off (B) Temporary variable defined in the code (C) Program or opcode (D) Data when power is on only.	
	(iii) The EPROM with quartz window offers (A) Slow erasing and out of board programming (B) Slow erasing and in-system programming (C) Fast erasing and out of board programming (D) Fast erasing and in-system programming	
	(iv) The operation of Memory read is not supported during (A) Refreshing of DRAM (B) The absence of external power supply in NV-RAM (C) Discharge of capacitor in DRAM (D) Interrupt driven execution with SRAM	

	(v) The port pin must carry a logic-1 to turn on LEDs that are connected in (A) Common Anode configuration when common terminal is at +5V (B) Common Anode configuration when common terminal is at 0V (C) Common Cathode configuration when common terminal is at +5V (D) Common Cathode configuration when common terminal is at 0V [CO1-K1]	
2.	**(a)** (i) Write the names of communication interfaces (protocol) that are supported by ATmega2560 microcontroller directly.	3
	(ii) What is a bootloader? What is the most common communication port through which a bootloader interacts with PC?	3+1
	(iii) State differences between a compiler and a programmer.	3
	OR	
	(b) Draw the generalized block diagram that shows the architecture of a microcontroller with all necessary functional components and features. Explain the diagram. [CO2-K1]	10
3.	**(a)** Write a program segment to (i) read bit-3 of PORTB (ii) set bit-2 and reset bit-5 of PORTA keeping other bits unchanged (iii) shift the content of PORTC by a variable amount as decided in program (iv) send the number 6 as a character to PORTA. (v) calculate the time consumed to execute a block of commands	5x2=10
	OR	
	(b) Read pin-0 and pin-1 of PORTD. In reference to the truth table shown in Table-1:	

Pin-1	Pin-0	Duty cycle	Frequency
0	0	80%	4Hz
0	1	80%	50Hz
1	0	50%	4Hz
1	1	50%	50Hz

Table-1

write a program to generate a pulse at pin-7 of PORTD. The duty cycle and frequency of the pulse is shown in Table-1. Write a program accordingly. 10

[CO3-K2]

4. **(a)** Write a program using Timer-5 to generate a pulse of 2Hz at a duty cycle of 50%. Explain your solution stating necessary assumptions, if any. 10

OR

(b) Read an analog channel continuously to receive data. The channel voltage is in the range of 0-5V. Send the data read to serial monitor. Estimate the overall conversion time of analog voltage to its digital equivalent. Write a program accordingly. 10

[CO4-K3]

5. **(a)** Receive a byte of data serially (one bit at a time) via D5 pin of PORTA. The LSB of the data should come in first. The LED connected to PORTB.7 should glow for 2s after receiving a bit and 5s after completion of reception of the entire byte. The received byte should be sent to PORTC. Write a program to implement the requirement. 10

OR

(b) An LED connected to PORTB.7 blinks continuously with a duty cycle of 50% nad frequency of 100Hz. When the main program continues to run, an interrupt is generated by timer-3 at every 1s interval. On appearance of the interrupt, an LED connected to PORTA.7 toggles. Write a program to implement the requirement. 10

[C05-K4]