Ref. No.: Ex/EE/PC/B/T/225/2024

B. E. ELECTRICAL ENGINEERING 2ND YEAR 2ND SEMESTER EXAMINATION, 2024

Subject: SEQUENTIAL SYSTEMS & MICROPROCESSOR Time: 3 Hours Full Marks: 100

(50 Marks for each Part)

Use a separate Answer-script for each Part

Part I (50 marks)

Question 1 is compulsory

Answer ***Any Two*** questions from the rest (2×20)

Question No.		Marks
Q1	Answer ***any Two*** of the following:	
	(a) Explain the PRESET and CLEAR operations with respect to D Flip-Flop.	5
	(b) A fictitious flip-flop with two inputs A and B such that for AB= 00 and 11 the output becomes 0 and 1, respectively. For AB= 01, flip-flop retains previous output while output complements for AB= 10. Draw the truth table and excitation table of this flip-flop.	5
	(c) Starting from the excitation table develop the state diagram for J-K flip-flop.	5
	(d) What are Synchronous and Asynchronous Counters? What are the basic differences between them?	5
Q2	(a) What is Excitation Table for a Flip-flop? With the help of Excitation Table show how SR-flip-flop can be converted to JK-flip-flop.	2+6
	(b) (i) With the help of timing diagram show that the circuit shown in Figure Q2(b) is a Mod-3 counter.	6+6
	(ii) If one connects the B output of the counter to the clock input of another J-K Flip-Flop, with both J and K of the 3rd Flip-Flop connected to $+V_{CC}$, draw the waveforms for the three JK flip-flop outputs.	

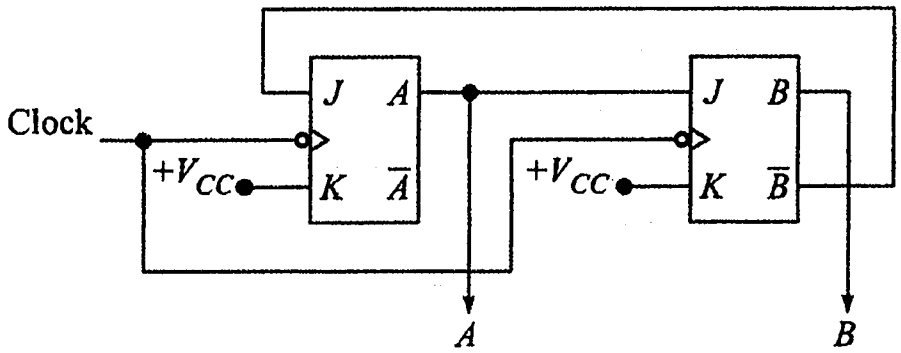
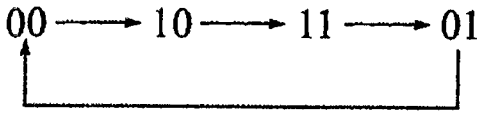


Figure Q2(b)

[Turn over

Q3 (a) Draw the block diagram of a 4-bit Shift-Right Register realized using D flip-flops. Show, with the help of timing diagram, how "0100" can be entered serially into the register. 4+8

(b) Design a modulo-4 irregular counter with the counting sequence as shown in Figure Q3(b) using D flip-flop.



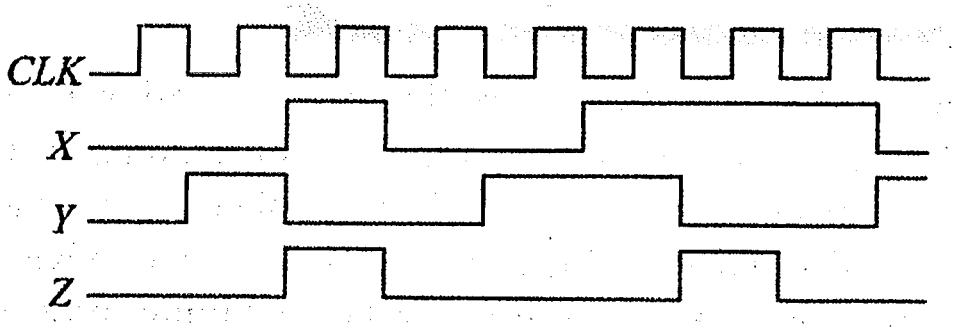
8

Figure Q3(b)

Q4 (a) With the help of a schematic diagrams explain the basic difference between the Mealy and Moore models of Finite State Machine. 6

(b) Consider the timing diagram, as given by Figure Q4(b), for a synchronous sequential logic circuit that has two inputs X and Y and one output Z.

Derive (i) the State Diagram and (ii) the State Synthesis Table for a Mealy Model of the circuit and (iii) realize the circuit with the help of D flip-flops.



4+4+6

Figure Q4(b)

Q5 (a) What is Universal Shift-Register? With the help of a neat diagram briefly explain the different modes of operation for 4-bit Universal Shift-Register. 2+8

(b) Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1s in a string of bits coming through an input line (i.e., the input is a serial bit stream).

(i) Draw the corresponding state transition diagram.

(ii) Obtain, with the help of state table, the logic circuit for the sequence detector realized employing D flip-flops. 4+6

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B.E. ELECTRICAL ENGINEERING SECOND YEAR SECOND SEMESTER EXAM 2024

SEQUENTIAL SYSTEM AND MICROPROCESSORS

Time: Three hours (50 marks for each Part) Full Marks: 100

Use a separate Answer-Script for each Part

PART- II

Group-A

Answer any four questions: **4X5=20**

1) Explain with suitable diagram why de-multiplexing of address and data bus is required?

2) Distinguish the operation between program counter and stack pointer 16-bit registers

3) What do you mean by wait state? Explain the operation of wait state generator showing typical circuit.

4) Explain why image address for memory address decoding will form. How this problem can be eliminated? Giving example.

5) Define instruction cycle, machine cycle and T-state.

6) Distinguish between memory mapped I/O and I/O mapped I/O address decoding method with necessary example.

7) Distinguish between the operation of interrupt service routine (ISR) and subroutine. Give example.

8) Explain how RIM instruction is used to sense the pending interrupts with the help of word format.

Group-B

Answer any three questions: **3X5=15**

1) Draw the timing diagram of a memory read bus cycle. Suppose the READY signal becomes low at the middle of second T state. Draw the timing diagram for the modified memory read bus cycle.

2) Show the timing diagram for STA <16-bit operand> which consumes 3 machine cycles and 10 T states. The hex code for STA is 32H.

3) What are vectored interrupts? How is the address of the Interrupt Service routine calculated in vectored interrupts? Explain with an example.

4) The 8085 CPU is operated with clock frequency 3.77 MHz. Find out the time delay in sec can be produced by following programme:

```
        LXI B, 0FFFH; 10 T-states
BACK:   DCX B          ; 6 T-states
        MOV A, C       ; 4 T-states
        ORA B          ; 4 T-states
        JNZ BACK       ; 10 T-states
```

5) Draw diagram for interfacing RAM of size 2K and I/O with 8085 CPU at address 2000H and 4000H for RAM and 17H and 07H for I/O. Use partial memory and I/O address decoding method.

6) Discuss the control word format of 8255 PPI interfaced with 8085 CPU in BSR mode with suitable example.

7) What is meant the priority of interrupt system? How vector interrupt in 8085 CPU is masked?

Group-C
Answer any three questions: **3X5=15**

1) Write an assembly language programme to form two arrays, one which will store even no and the other which will store odd no from a given arrays N numbers.

2) Write an assembly language programme to sort a given array of N elements in ascending order. Also find the count for repeated no. in the unsorted array.

3) Write 8085 Assembly language program to find the factorial of an 8-bit number. Draw the flow chart of the algorithm used.

4) Write an assembly language program in 8085 microprocessor to find square root of a number.

5) Write an assembly language programme to convert 2-digit BCD number into 8-bit binary number. Draw the flow chart of the algorithm used.

6) Write an assembly language programme to generate a pulse of duration 1 ms via I/O port with address 01H. The pulse must be initiated by pressing a push button connected to RST 7.5 vector interrupt pin of 8085 CPU.