B.E. COMPUTER SCIENCE AND ENGINEERING
SECOND YEAR, FIRST SEMESTER
SUPPLEMENTARY EXAM 2024

Subject: **Digital Logic and Circuits**

Time : Three hours **Full Marks: 100**

CO-1 (20 marks)	1. Convert the following decimal numbers to their binary forms and find the results of the subtraction using 2's complement. Express the results in their decimal equivalent. (i) 100 - 53 (ii) 25 – 54 2. Determine the odd parity bits generated for the messages consisting of BCD equivalents of the numbers from 75 to 80. 3. Define the Hamming distance between two coded words. Find the hamming distances between each pair of the following codes: 11010111, 11000111, 00011110, 00110011. What is the minimum hamming distance? 4. Convert (225.25)10 to binary, octal and hexadecimal. [4+6+4+6=20]
CO-2 (30 marks)	Answer any 3 questions: 5. (a) Minimize the following Boolean function using Karnaugh Map $F(A, B, C, D) = \Sigma (0,1,2,7,13,14) + d (3,5,10,15)$ (b) Express the minimized Boolean function in Sum-of-Product form and Product-of Sum form [6+4=10] 6. (a) Plot the logical expression ABCD + AB'C'D' + AB'C + AB on a 4 variable K-map, obtain the simplified expression from the map. (b) Implement the simplified expression using only AND and NOT gates. [5+5=10] 7. Find the minimal sum of products for the Boolean expression using the Quine- McCluskey method. i) $\sum m (0,2,8,12,13)$ ii) $\sum m (1,3,7,11,15) + \sum d (0,2,5)$ [5+5=10] 8. (a) Reduce the following Boolean expression to four literals: BC + AC' + AB + BCD (b) Implement the expression using 2-input NAND gates. (c) Convert the following to the other canonical form $F(A,B,C) = \Pi (1,3,7)$ [4+3+3=10]
CO-3 (40 marks)	Answer any two questions from this group. 9. (a) Explain the functioning of a multiplexer and a demultiplexer. (b) Construct a 8x1 multiplexer using 2 number of 4x1 multiplexer and any additional logic gates (if required). (c) Using a decoder and external gates, design the combinational circuit defined by the following Boolean functions: (i) F1 = x'y'z' + xz (ii) F2 = xy'z' + x'y (d) What is a ripple counter? Draw the circuit and the timing diagram of a 4-bit +ve edge triggered ripple counter. [4+4+4+8=20] 10. (a) Write the Boolean expressions for a binary full adder. Draw a full adder circuit using AND, OR and NOT gates. (b) What is a synchronous counter? Draw the circuit and the timing diagram of a 4-bit –ve edge triggered synchronous counter. (c) Using D Flip-flops, provide the design of a Parallel In/Serial Out Shift Registers [7+8+5=20]

	11. (a) Show the logic diagram of an SR latch. Show the changes in the output signals for the following changes in inputs: Initially, R=1 and S=0; then R=0 and S=0; R=0 and S=1; R=1 and S=1; and finally R-0 and S=0. (b) What is a Master-Slave J-K flipflop? (c) Design a synchronous counter for a sequence 0 → 1 → 3 → 5 → 7 → 0. Use JK Flip-flop for the circuit. 6+4+10=20
CO-4 & 5 (10 marks)	Answer any one questions: 12. a. Draw the functional diagram of monostable multivibrator using IC 555 timer and explain their operation. b. Draw and explain the operation of 4 bit successive approximation analog to digital converter. [5+5=10] 13. With a neat diagram explain a Binary weighted resistor (1010) configuration for digital to analog conversion. b. Using ECL implement Y= (A+B)' and explain it. [5+5=10]