Ex/CSE/PC/B/T/215/2024

B.E. Computer Science and Engineering 2nd Year 1st Semester Examination 2024

Subject: Computer Organisation

Time: 3hrs **Full Marks:** 100

Answer all

Answers of all sub-parts of a question must be in ***adjacent*** locations

1	(a) *Answer **any six**:* (i)_____ and _____ are the roles of operating system. (ii) _____ and _____ are two states of a process. (iii) Control signal is an attribute of (A) Computer Organization, (B) Computer Architecture, (C) Both, (D) None (*choose the correct one*) (iv) An instruction set is an attribute of: (A) Computer Organization, (B) Computer Architecture, (C) Both, (D) None (*choose the correct one*) (v) A parser generates a set of tokens. (*Say true or false*) (vi) The computer system ENIAC had the facility for storing both program and data of users. (*Say true or false*) (vii) CPU has some internal registers like MQ and AC that sometimes work together to execute a single instruction. (*Say true or false*) (vii) In IAS computer, JUMP instructions get the information from the Accumulator register. (*Say true or false*)	6x1
	(b) (i) Outline the architecture as proposed by Von-Neumann, and give a very brief description about each component. **OR** (ii) Give a brief description of IAS instruction set considering all categories.	6
	(c) (i) Explain **any two** addressing modes – indirect, relative, and auto-indexed. **OR** (ii) Write the **instruction sets** for executing the following expression by considering a 2-address machine architecture (if possible, you can optimize the number of instructions): C = (A - A) * (A - A)* (B - B) * (B –B)	3

2	(a). (i) Design the Carry Lookahead adder. **OR** (ii) Discuss the pros and cons of sign-magnitude, 1's complement and 2's complement numbering systems. (b). Give the flowchart for the restoring **OR** non-restoring type division of 2's complement numbers. Show an example mentioning all steps. For the example, use the last two digits of your examination roll number as the divisor and dividend.	5 3+7
3	(a) *Answer any **seven***: (i) Logical cache access speed is _____ than for a physical cache, because the cache can respond before the _____ performs an address translation. (ii) Hit ratio begins to decrease as the block becomes _____ and the probability of using the newly fetched information becomes _____ than the probability of reusing the information that has to be replaced. (iii) Advantages of unified cache is that it has a _____, and it _____ of instruction and data fetches automatically. (iv) Soft errors can be caused due to _____ and _____. (v) In the write though policy, all write operations are made to _____ as well as to the cache, but its limitation is that it generates _____. (vi) As logic density has increased it has become possible to have a cache _____ as the processor, and the on-chip cache accesses will be faster than would even _____ bus cycles. (vii) About Radom Access Memory which is untrue? 1) Read-write ability, 2) Erasing at block-level, 3) Writing using electrical energy, or 4) Volatile (*Choose the correct one*) (viii) In a SRAM cell, data stored in: 1) CMOS inverter, 2) Access transistor, 3) Both, or 4) None (*Choose the correct one*) (ix) Let's consider an exception case generated during the execution of an instruction – "memory does not exist". This is an exception is related to a) fetch operand, b) fetch instruction, c) both, or d) none. (*Choose the correct one*)	7x1

	(b) (i) Illustrate the implementation issues of direct memory mapping scheme used in cache memory **OR** (ii) Give a block diagram for Pentium 4 cache memory including 3 levels of cache.	5
	(c) With an appropriate example show the LRU **OR** FIFO page replacement algorithm. Consider there are **three** cache lines. Create the reference string using your last five digits of the examination roll number. If your roll is number is 24680, then the reference string would be 2468008642.	3
	(d) Consider there is a data stream of 8 bits (D), which you will get by converting the last two digits of your examination roll number into the binary number. Now find out the check bits (C). Hence, the given word consists of 12 bits (D+C). If your roll number is odd then flip (0 to 1 or 1 to 0) the 2^{nd} data bit, otherwise flip the 3^{rd} data bit. Now this becomes your new data bits. Again find out the check bits. Using the Hamming code, **prove** that the **error** has been occurred in the 2^{nd} or 3^{rd} bit position.	7
	(e) (i) With the circuit diagram, describe the working principle of a SRAM cell. **OR** (ii) Compare data **recoverability** and data **redundancy** issues in RAID levels 1, 4 and 6.	6
	(f) (i) Give the details of the Winchester Disk format. **OR** (ii) With a pictorial diagram briefly describe the SSD architecture.	7
4	(a) Compare **any two** implementation strategies of hardwired control unit.	6
	(b) (i) Design the micro-programmed based control unit. Give a brief description of this design. **OR** (ii) With an example, formulate the **space reduction procedure** of the control memory used in the nano-programmed control unit.	8
	(c) What are the limitations of the mono **OR** poly-phase microinstruction timings?	1

5	(a). (i) Show the pictorial diagram of Intel 82C59A interrupt controller. (ii) What is the key advantage of using DMA? With a pictorial diagram briefly describe the working principle of 8237 DMA controller. **OR** (ii). Write a short note on Thunderbolt including all protocol structures used here. (b). (i) Let's consider the last six digits of your examination roll number. Now, design a reservation table for a 4-stage (Fetch-Decode-Execute-Write) pipeline architecture, and execute at least 6 instructions (I_1 to I_6) except the branch instructions. Scan your roll number from the **left to right**, and add delays using the following rule: *if the digit is an odd number, add **2 clock cycles of delay** for that instruction, otherwise add **1 clock cycle of delay*** (you can add delays at any of the four stages of the pipeline). If the roll number (considering all 6 digits) is an odd number, *I_2 would be a branch instruction, otherwise I_3 would be the branch instruction.* Consider that you have an **instruction pre-fetch queue**, so that any cache miss for the instruction hazard can be handled. Justify (i.e., give reasons) the reservation table you have made. **OR** (ii). Write a short note on PCIe (Peripheral Component Interconnect Express).	3+1 +6 10 10 10