ABSTRACT

Advancements in electronics, wireless communication, and IoT have led to the implementation of Dennard's scaling theory. The need for reduced power matrices in smart gadgets has driven researchers to explore new engineering concepts and novel device structures. Bulk MOSFET technology has been continued with improved structural engineering and finding alternative devices with below 60 mV/decade subthreshold swing has always been on the focus of research endeavour. Silicon-on-Insulator (SOI) and Silicon-on-Nothing (SON) Metal Oxide Semiconductor have gained attention for their higher scalability and reduced parasitic effects. However, SOI/SON-based circuits struggle with power-speed performance, leading to the search for new structures. Junctionless Transistors (JL FET) are another promising solution, but they suffer from degraded subthreshold swing due to thermionic constraints. Therefore, a MOSFET-like structure with alternative energy-efficient technology becomes inevitable to sustain CMOS logic design in future. The Tunnel Field Effect Transistor (TFET), one of the potential contenders, takes the privilege of quantum mechanical tunneling and ballistic transport phenomena driven by low power supply, offering a minimal power-speed product earnestly required for today’s cut-in technological nodes. Moreover, the device is compatible with the latest fabrication technology, favoring ultra-high-density packaging to integrate billions of transistors in a single chip. However, two major constraints include low drive current and ambipolar conduction forbidding the device implementation in VLSI circuits.

VLSI Global routing is a crucial back-end design aspect in industrial VLSI research, aiming to optimize power-delay expenditure. With increasing layout complexity, interconnect routing becomes more complex and tedious. The NP-hard problem involves finding the minimal cost of a Rectilinear Steiner Tree from terminal node graphs. To achieve an acceptable solution, core area and critical path delay must be reduced, based on interconnected wire length and vias. Swarm intelligence, inspired by the intellectual activity of the biotic creators of nature, is one of the emerging and promising optimization tools that may be implemented in this field of optimizing interconnect lengths in achieving the desired performance (speed) of modern ICs.